Supplementary Materials for

"Moiré Synaptic Transistor for Homogeneous-Architecture Reservoir Computing"

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Methods

Device fabrication

We fabricated a h-BN-encapsulated Bernal bilayer graphene (BLG) device with alignment between the straight edges of the BLG flake and the h-BN flakes by using a standard dry-transfer technique (Fig. S1). We first mechanically exfoliated bilayer graphene and h-BN (10-30nm) on 300-nm SiO_2/Si substrate, and selected the flakes of appropriate thickness and high quality with the assistance of optical contrast and atomic force microscopy (AFM). We used a poly (bisphenol A carbonate) (PC)/ polydimethylsiloxane (PDMS) stamp to stack a h-BN flake, a BLG flake, and another h-BN flake sequentially at 80°C. In the stacking process, the BLG sheet was first aligned with both the top and bottom h-BN flakes along the straight edges. The h-BN-encapsulated BLG heterostructure was then released from the PC film to a SiO_2/Si substrate at 140°C. The devices were etched by electron beam lithography and dry etching with a CHF_3/O_2 in an Inductively Coupled Plasma (ICP) system. The metal top gate and the edge contacts were patterned using the standard electron beam lithography method and deposited by the standard electron beam evaporation of Cr(5nm)/Pd(15nm)/Au(30nm).

Electrical measurement

All the electrical measurements were performed at room temperature in a nitrogen atmosphere,

using a semiconductor parameter analyzer (Keysight B1500A) and a probe station (Cascade Summit 11000 M). The input voltage pulses were programmed and generated through a high-voltage pulse generator unit (Keysight B1525A) or a source meter (Keithley 2636B). All measurements were controlled by the instruction implemented with LabVIEW.

Implementation of handwritten digits recognition

To demonstrate the reliability of our proposed moiré physical neural network in implementing homogeneous architecture reservoir computing, we carried out a simulation for the recognition task of the MNIST handwritten digit dataset. The MNIST dataset consists of 60000 handwritten digits for training and another 10000 handwritten digits for testing. Each digit image in the dataset contains 28×28 pixels and has been binarized prior to classification. We first transformed the image into a 196×4 matrix, where each row corresponds to a 4-timeframe sequence. These sequences can be categorized into 16 different distributions, and all the 4-timeframe sequences in the matrix are a subset of these 16 possible sequences. To extract the spatial features of the 4-bit patterns processed by the moiré reservoir, we experimentally measured the read currents under 16 input pulse streams and obtained the reservoir states for each sequence. These measured current values were used to construct a 196×1 reservoir-processed feature vector for each image, where each element of the vector is represented by the read current extracted from the measured data for specific 4-bit input sequences. To achieve digit recognition based on the output results of the reservoir, we further used a fully connected 196×10 moiré-based network as the readout layer to process the 196×1 feature vector. We adopted the sigmoid activation function, which is defined as $f(x) = (1 + e^{-x})^{-1}$, and a typical cross-entropy loss function in network implementation. The neural network was trained by standard error backpropagation and mini-batch gradient descent algorithm with a batch size of 12 for weight updates. Considering the memory characteristics of the moiré synaptic transistor, a differential weight-mapping scheme was employed, where each effective synaptic weight contains a pair of moiré synaptic transistors, which is defined as $W = G^{+}\text{-}G^{-}$. The conductance of the moiré synaptic transistor was experimentally demonstrated to be continuously tunable within the range of 260 μS to 330 μS, and the differential conductance adjust range was limited between -70 μS and 70 μS. In software, the corresponding weights were limited to the range of [-3.5, 3.5]. All the simulation algorithms were implemented using MATLAB.

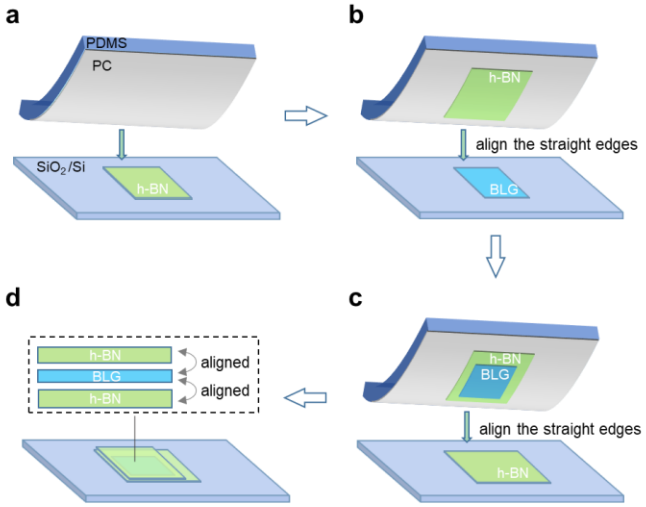

Fig. S1. Dry transfer process for h-BN-encapsulated BLG heterostructure with alignment between the straight edges of BLG and h-BN. (**a**) A h-BN flake with long straight edges was picked up by using a poly (bisphenol A carbonate) (PC)/ polydimethylsiloxane (PDMS) stamp at 80℃. (**b** and **c**) With the aid of a microscope, the straight edges of BLG and h-BN flakes can be precisely aligned. The BLG flake and another h-BN flake were stacked after alignment at 80 ℃. (**d**) The h-BN-encapsulated BLG heterostructure was released from the PC film to a SiO_2/Si substrate at 140℃. The straight edge of the BLG flake was aligned with those of both the top and bottom h-BN flakes.

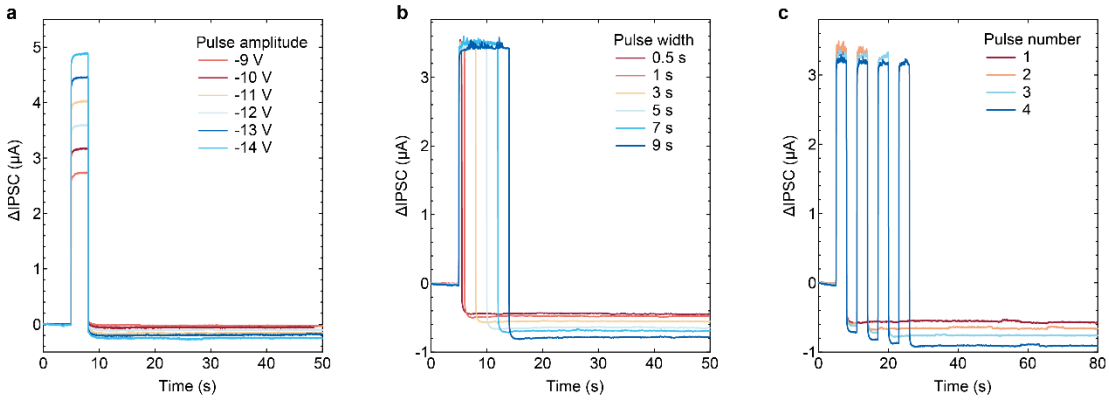

Fig. S2. Dynamic current change of the moiré synaptic transistor in response to various external stimuli of negative V_G. After removing the negative gate voltage pulse, the device current decreases below the initial state, mimicking inhibitory postsynaptic current (IPSC) behavior in biological synapses. (**a**) The IPSC responses to a train of pulse with different pulse amplitude from -9 V to -14 V and an identical width of 4 s. (**b**) The IPSC responses to a train of pulse with different pulse width from 0.5 s to 9 s but a fixed amplitude of -12 V. **(c)** The IPSC responses at different pulse number from 1 to 4, where the pulse amplitude, width, and interval are fixed at -12 V, 3 s, and 3 s, respectively. As the amplitude, width, and number of applied voltage pulses increase, the current change exhibits a gradual increase, indicating a transition from short-term depression to complete long-term depression.

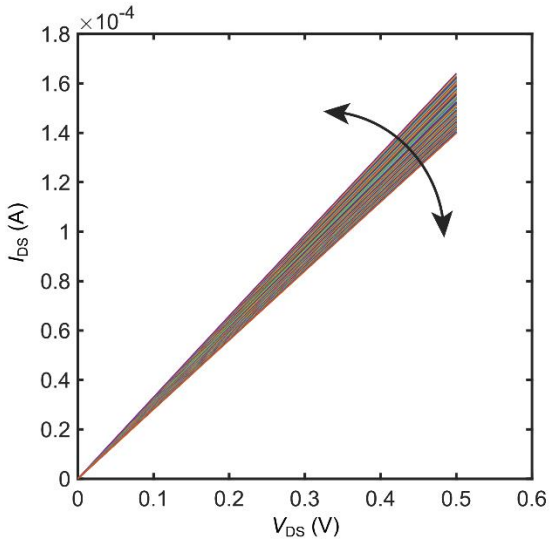

Fig. S3. Linear current-voltage characteristics of the moiré synaptic transistor with different conductance states. Under the precise control of the gate voltage pulse, the conductance of the moiré synaptic transistor can be continuously tuned within a specific range. The device demonstrates excellent linear *I*-*V* characteristics, making it a suitable synaptic unit for the artificial neural network hardware, which can be used to physically perform multiplication through Ohm's law: $I=G\cdot V$.

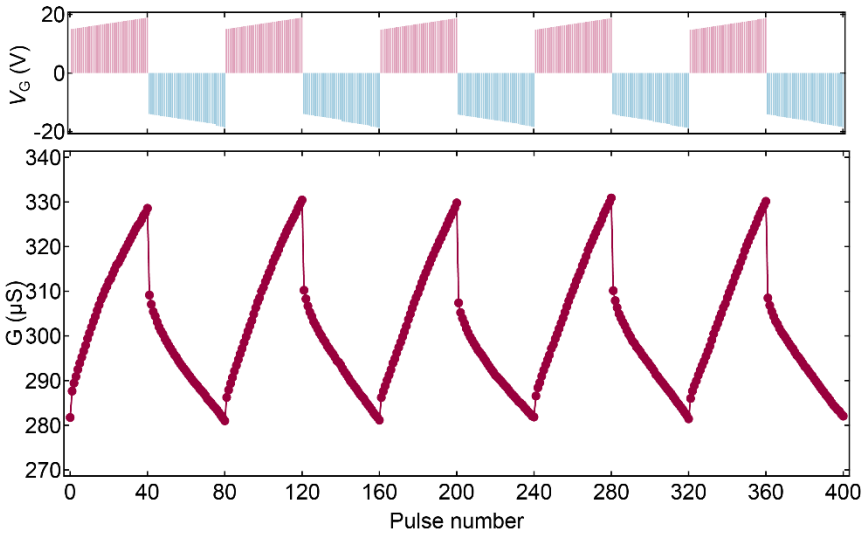

Fig. S4. Reproducibility of long-term potentiation and depression at a moiré synaptic transistor. Top, the device was programmed by a sequence of 40 positive pulses (amplitude: from 15 to 19 V in increments of 0.1V; width: 4 s) followed by 40 negative pulses (amplitude: from -14 to -18 V in increments of -0.1V; width: 4 s). Bottom, the conductance incrementally changes through this sequence of pulses, exhibiting long-term potentiation and depression characteristics. This sequence was repeated five times, and the device demonstrates great repeatability and negligible cycle-to-cycle variation. The conductance values were read out at V_{DS} = 0.1 V after each pulse.

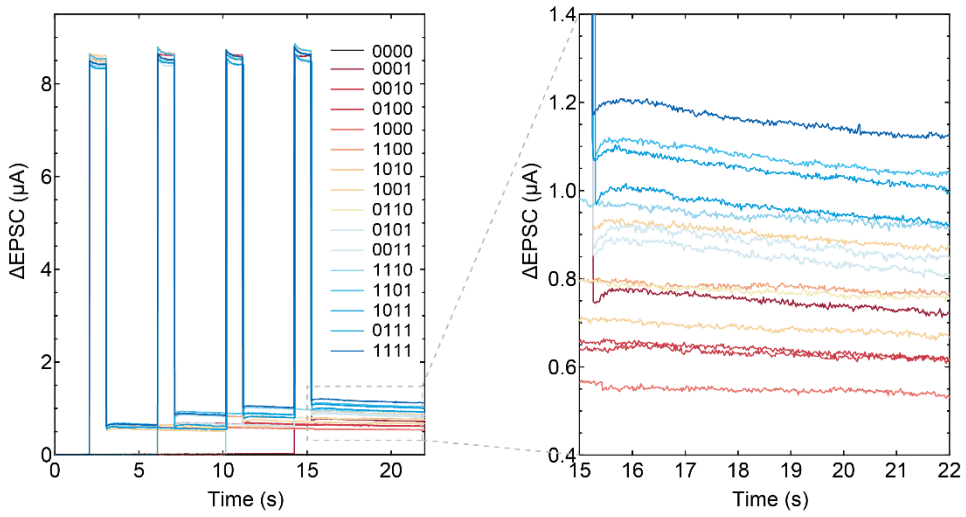

Fig. S5. Dynamic current change in response to 16 different input pulse streams ranging from "0000" to "1111". The bit "1" is represented by a high amplitude pulse (18 V, 1 s), and the bit "0" is represented by a pulse with an amplitude of 0 V (equivalently no pulse). Right, plot of the enlargement for the gray dashed box. Due to the short-term memory effect and nonlinearity of the device, the current response to 16 different input pulse streams can be clearly distinguishable.

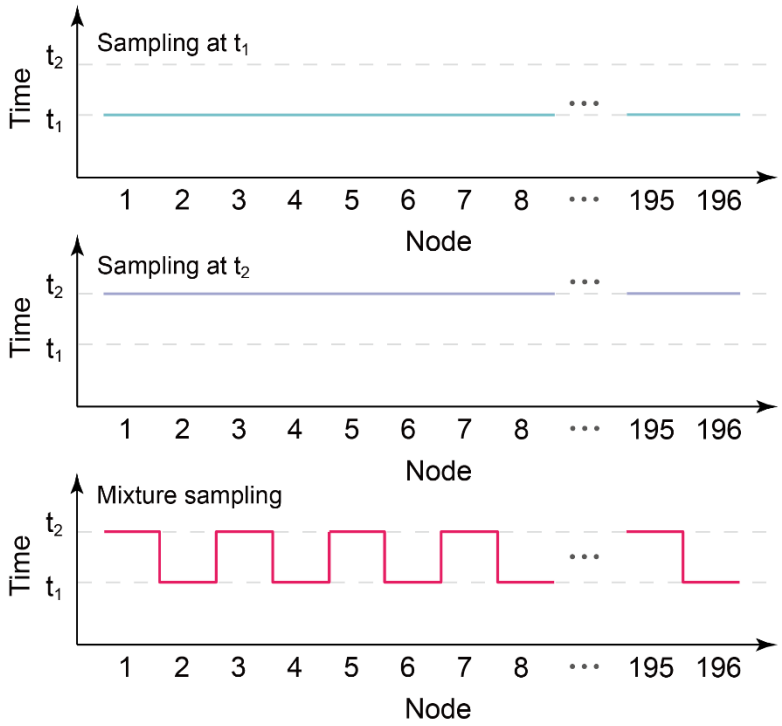

Fig. S6. Three reservoir state sampling modes. The reservoir layer comprises 196 reservoir nodes, where the encoded 196 streams of 4-timeframe pulses are input into the corresponding reservoir nodes respectively. To record the reservoir states, we categorize the sampling modes into three types according to the sampling time for each node: all nodes sampling at t_1, all nodes sampling at t_2, and mixture sampling. In the mixture sampling mode, the sampling time alternates between t_1 and t_2 for each node.