Supplementary Material: *In situ* epitaxy of pure phase ultra-thin InAs-Al nanowires for quantum devices

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Section 1 Methods

A. InAs-Al nanowire growth

InAs nanowires were grown in a solid source MBE system (VG V80H) equipped with standard *Knudsen-cells (including* arsenic cell*)*. Commercial p-type Si (111) wafers were used as the substrates. Before loading the Si substrates into the MBE chamber, they were immersed in a diluted HF (2%) solution for 1 min to remove the surface contamination and native oxide.[1] The Si (111) substrates were initially heated in the preparation chamber to ~200 °C for water desorption. After that, a Ag layer less than 0.5 nm nominal thickness was deposited on the Si substrate in the MBE growth chamber at room temperature and then annealed *in situ* at 550 °C (measured by thermocouples) for 20 min to generate small Ag nano-particles. Ultrathin InAs nanowires with a diameter ranging from ~20 to 30 nm were obtained with these small Ag seed particles (very few nanowires with a diameter smaller than 10 nm or larger than 40 nm also appear on the substrate surface resulting from the Ostwald ripening). According to our previous work,[1] the dimension of InAs grown by MBE using Ag as catalysts can be tuned directly from one-dimensional nanowires to two-dimensional nanosheets and to three-dimensional complex crosses only by increasing the indium flux. Thus, to obtain InAs nanowires, the sample should be grown under an arsenic rich growth condition. In this work, the ultra-thin InAs nanowires were grown for 40-80 min at a temperature of 505 °C with an arsenic/indium beam equivalent pressure ratio of ~ 42 (the beam fluxes of In and As_4 sources are 1.1×10^{-7} mbar and 4.6×10^{-6} mbar, respectively. The indium flux is ~ 9×10^{13} atoms/cm^2/sec). After the growth of nanowires, the sample was transferred from the growth chamber to the preparation chamber at 300 °C to avoid arsenic condensation on the nanowire surface. The sample was then cooled down to low temperatures (~ 1 °C to -40 °C) by natural cooling and liquid nitrogen cooling in the both growth chamber and prep chamber. Al was evaporated from a Knudsen cell at an angle of ~20° from the substrate normal (~70° from substrate surface) and at a temperature of ~1150 °C for 70-360 s (giving approximately 0.083 nm/s). To obtain half Al shells, the substrate rotation was kept disabled during the Al growth. When the growth of nanowires with Al was completed, the sample was rapidly pulled out of the MBE growth chamber and oxidized naturally. We have grown InAs/Al nanowires both with the mounted (mounted on Mo holders by use of melting In) and unmounted manners. We found that InAs/Al nanowires were not damaged even they underwent a temperature cycle (to >156.6 °C) post growth. For TEM analysis, nanowires were removed from the growth substrate via sonication in ethanol and then drop-cast onto the ultrathin carbon support films.

B. Device fabrication and transport measurement

For device fabrication, InAs-Al nanowires were transferred by cleanroom wipes touching and swiping the growth chip, then swiping them onto the chip substrate: highly p-doped Si covered by 285 nm thick silicon dioxide. The aluminum film was selectively etched using Transene Aluminum Etchant Type D at 50 °C for 10 seconds. Ohmic contacts to the InAs nanowire were fabricated by 80 s Argon plasma etching at a power of 50 W and pressure of 0.05 Torr, followed by metal evaporation of Ti/Au (10/70 nm). For transport measurements, the devices were cooled down and measured in a Bluefors dilution refrigerator at a base temperature ~ 20 mK, equipped with a 6-1-1 T vector magnet. Differential conductance was measured using an AC lock-in technique, with excitation voltage of 8 μV. Fridge filter resistance was independently calibrated and subtracted. The measurement circuit was also calibrated with testing resistors. During the measurement of Device A, the lock-in notch filter was on, which underestimates the ZBP height, as reported in this paper, by ~ 3%. The effect of this notch filter for low conductance (e.g. the hard gap near pinched off) is negligible. The nanowire orientation was identified by rotation the magnetic field direction in the substrate plane: the superconducting gap is maximum when the field is aligned with the wire. This is also consistent with the direction estimated based on the device optical/SEM image and chip mounting.

Section 2 Morphology control of the InAs-Al nanostructures

Figures S1(a) and 1(b) show the SEM images of the InAs-Al recorded from different regions on the Si (111) substrates with the Al shell grown at a relatively high temperature of ~ 1 °C. The Al shells are discontinuous and look like 'pearls on a string' on the side walls of all the InAs nanowires. Figures S1(c)-1(e) are a close-up of such a typical InAs-Al where the Al crystalline islands have a length distribution ranging from a few nanometers to about several tens nanometers. These crystals are formed due to a high Al adatom mobility and a long adatom diffusion length since the substrate temperature is relative high during growth. This phenomenon was also observed in the growth of Al on thick InAs nanowires by other groups.[2-4] The interface between InAs nanowire and Al island is relative sharp since the InAs nanowires are pure phase crystals, free of stacking faults and twin defects, which can provide smooth InAs side surfaces for superconductor growth. To obtain continuous Al shells, we further cooled down the substrate to ~ -10 °C for Al growth. Figures S1(f) and 1(g) show the corresponding SEM images from different regions on the Si (111) substrates. Now, the Al shells are continuously formed on the InAs nanowire facets, covering the wire's entire length, see Figs. S1(h)-1(j) for a close-up of a typical InAs-Al wire. We note that all the Al shells have a rough and faceted outer surface. The grain structure and faceted surface are further confirmed by the TEM analysis (Fig. S2). One reason for this rough

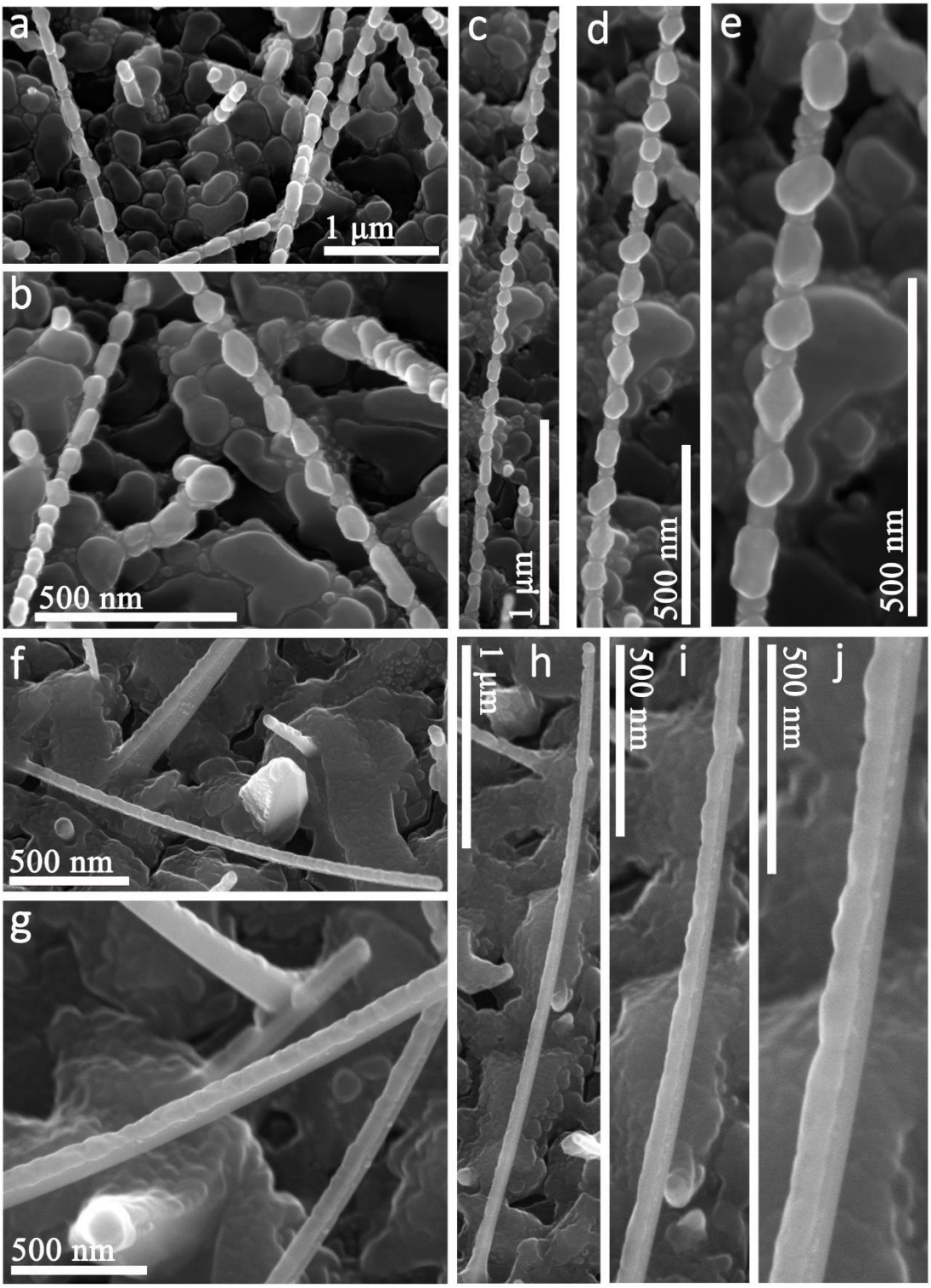

Fig. S1. Morphology control of the InAs-Al nanostructures. [(a) and (b)] SEM images of the InAs-Al recorded from different regions on the Si (111) substrates with the Al shell grown at ~ 1 °C. [(c)-(e)] High magnification SEM images of a typical InAs-Al nanostructure (grown at ~1 °C). Al looks like 'pearls on a string'. [(f) and (g)] SEM images of the InAs-Al nanowires recorded from different regions on the Si (111) substrates with the Al shell grown at ~ -10 °C. [(h)-(j)] High magnification SEM images of a typical InAs-Al nanowire (grown at ~ -10 °C). Continuous half Al shells form on the InAs facets. All the SEM images were taken at a tilt angle of 25°.

surface could be that the -10 °C substrate temperature is still not low enough and the Al growth follows the high temperature dynamics. That is, the large Al grains were initially nucleated and well separated. Then new preferred crystal orientations appeared at a later stage of the growth as the role of the grain boundaries and strain contributions. Thus, polycrystalline Al shells which consist of type-α and -β grains can be observed by TEM (Fig. S3). This phenomenon has also been observed in previous work.[2,3] Another reason could be that the thickness of Al shell measured from high-resolution TEM images is ~ 30 nm, which is beyond the critical thickness of Al layer for smooth shell growth. In short, the substrate temperature is a crucial parameter in enabling the deposition of continuous Al layers on the ultrathin InAs nanowires and the Al thickness directly affects the smoothness of the epitaxial Al layers. Besides growth temperature, the Al flux is also an important factor for the continuous Al layer growth. We find that for Al grown at ~1 °C with a very small Al flux, nano-size Al droplets can form on the InAs nanowire side walls. A higher beam flux and a lower temperature is beneficial for the continuous Al layer growth. In the main text, all the InAs-Al nanowires are grown with a high Al flux (~ 1.1×10^7mbar).

Based on the feedback above, we further lower the substrate temperature during Al growth and reduce the Al film thickness (less than a critical thickness ~ 15 nm in our case). Thin Al shell is in any case necessary for its superconductivity to be maintained at high magnetic field. Figure S4 is the SEM image of an ultra-thin InAs-Al nanowires grown under this 'optimum conditions': the growth temperature and the growth time of the Al shells are ~-40 °C and 3 min, respectively. It is evident from Fig. S4(a) that continuous and smooth Al half-shells are formed on the facets of all the InAs nanowires.

In our work, all the InAs-Al nanowires were grown on p-type Si (111) substrates by MBE using Ag as the catalysts. From the SEM images in the main text (Fig. 1 and Fig. 2), we can see that most InAs nanowires have non-<111> growth directions. The possible reasons for this phenomenon are as follows. It is known that [111] (or [0001]) is the polar direction of III-V semiconductor nanowires with zinc-blende (or wurtzite) structure. Group-III and group-V terminated surfaces are defined as (111)A and (111)B polar surfaces, respectively. However, the non-polar nature of Si substrates indicates that (111)A and (111)B polar surfaces can coexist on the Si substrates surface, which normally leads to random growth directions of III-V nanowires. Meanwhile, we know that the Si substrates are very easy to oxidize in air. As mentioned in the experimental section, the Si substrates used in this work were immersed in a diluted HF (2%) solution for 1 min to remove the surface contamination and native oxide, but a thin oxide layer can form on Si substrates surface within a very short time before loading the Si substrates into the MBE chamber. According to literatures,[5,6] Si substrates are usually annealed to about 900 °C under UHV conditions before MBE growth to completely

remove the thin oxide layer before the growth process. However, this Si surface treatment temperature (~ 900 °C) exceeds the upper limit of the temperature (~ 800 °C) of our substrate heater. That means that the thin natural oxide layer of Si substrates cannot be removed completely before the InAs nanowire growth, which can result in random growth directions of our nanowires. Based on the literatures, the Al shell can be epitaxially grown either on the facets of <111> oriented InAs nanowires[2,4] or <001> oriented InAs nanowires[3]. Our work shows that, besides <111> and <001> orientations, the Al shells can also be epitaxially grown on the facets of InAs nanowires with various non-<111> growth directions due to the random growth directions of our nanowires. From the high magnification SEM image of the nanowires [Figs. S5(a) and 5(b)], we can see that continuous, uniform and thin half Al shells can be successfully grown for all growth directions. It is worth noting that some nanowires with a "worm-like" morphology can also be found on our substrate surface. This kind of nanowires were not discussed in this work. Some kink nanowires also appeared on our substrate surface. The change in growth directions is a common phenomenon in nanowire growth, which happens due to change in growth dynamics. Such changes have been well demonstrated in the previous work[2,7]. The crystal phase of such a kinked nanowire did not change.

Interestingly, for some rare cases, discontinuous Al shells have been found in the samples grown at different temperatures (ranging from ~ 1 °C to ~ -40 °C). As shown in Fig. S6, this discontinuous and rough Al surface is usually accompanied by an obvious enlarged catalyst particle on the top of the InAs-Al nanowire, which can be easily identified by SEM. Figure S7 shows the TEM analysis of such a case. HAADF-STEM image taken from the top of the wire indicates that the catalyst particle has two parts [Fig. S7(e)]. We can see from the false-color EDS elemental maps that the chemical compositions of the two parts are pure Al and Ag-In alloy, respectively. Besides, continuous and smooth Al shells could not be obtained on the facet of the InAs nanowires with a diameter less than or equal 10 nm. The growth mechanism of these kinds of InAs-Al nanowires is unclear and it can be studied for future research.

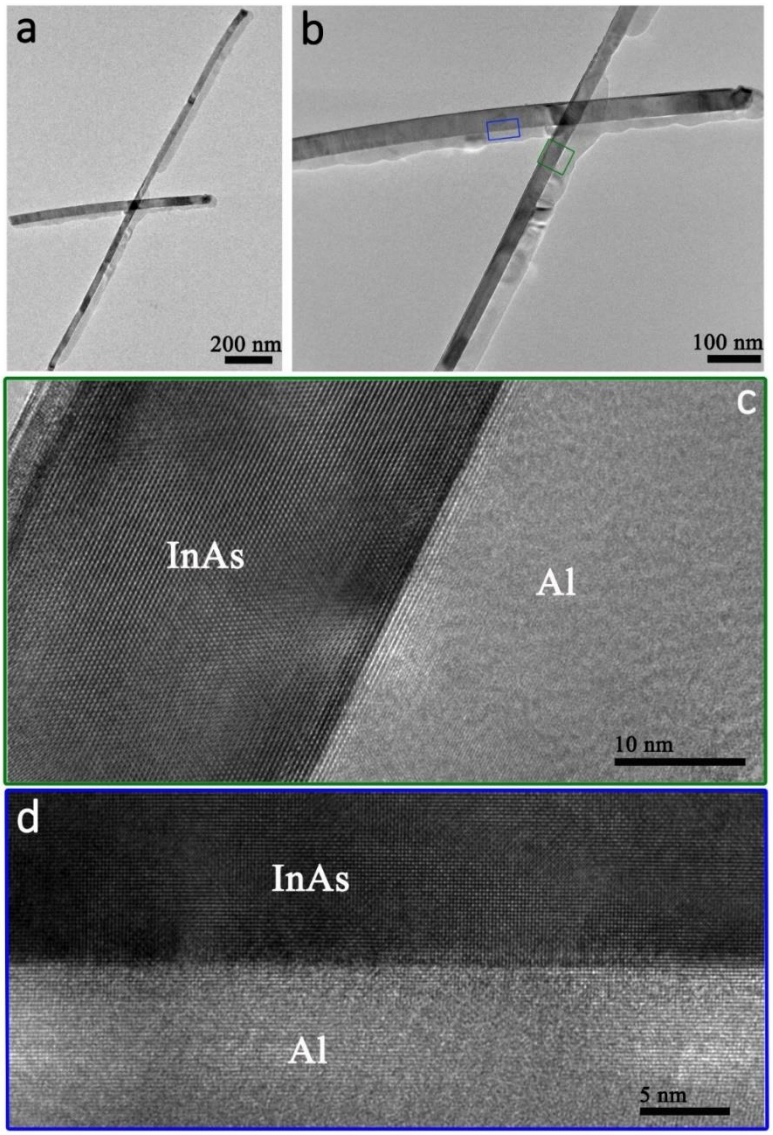

Fig. S2. [(a) and (b)] TEM images of InAs-Al nanowires with the Al shell grown at ~ -10 °C. [(c) and (d)] High-resolution TEM images of the InAs-Al nanowires in (b) indicated by the corresponding color boxes (green and blue). Continuous but rough and faceted outer surface of Al shells can be observed, consistent with the SEM results in Figs.S1(f)-S1(j). The interface between InAs nanowire and Al shell is sharp since the InAs nanowires are pure phase crystals, free of stacking faults and twin defects, which can provide smooth InAs side surfaces for Al growth.

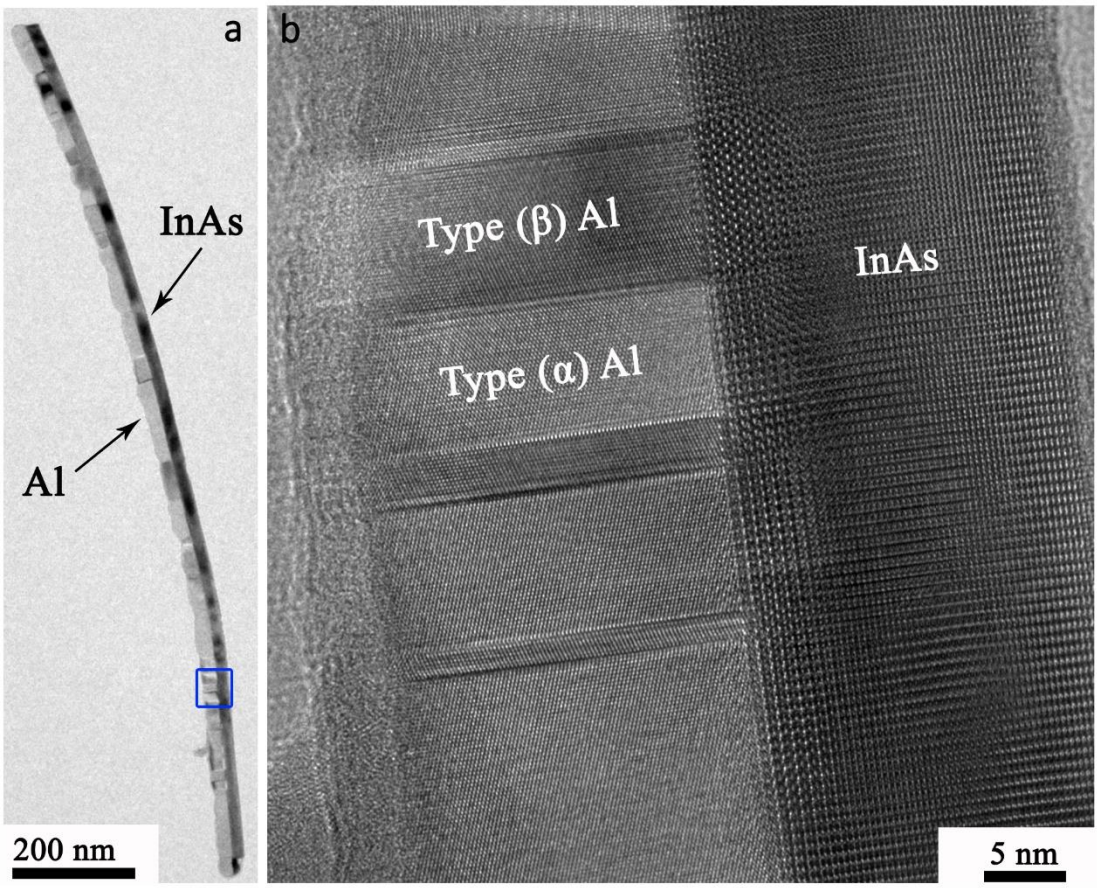

Fig. S3. (a) TEM image of an InAs-Al nanowire with the Al shell grown at ~ -10 °C. (b) High-resolution TEM image of the nanowire in (a) (blue box). Polycrystalline Al shell which consists of type-α and -β grains can be observed.

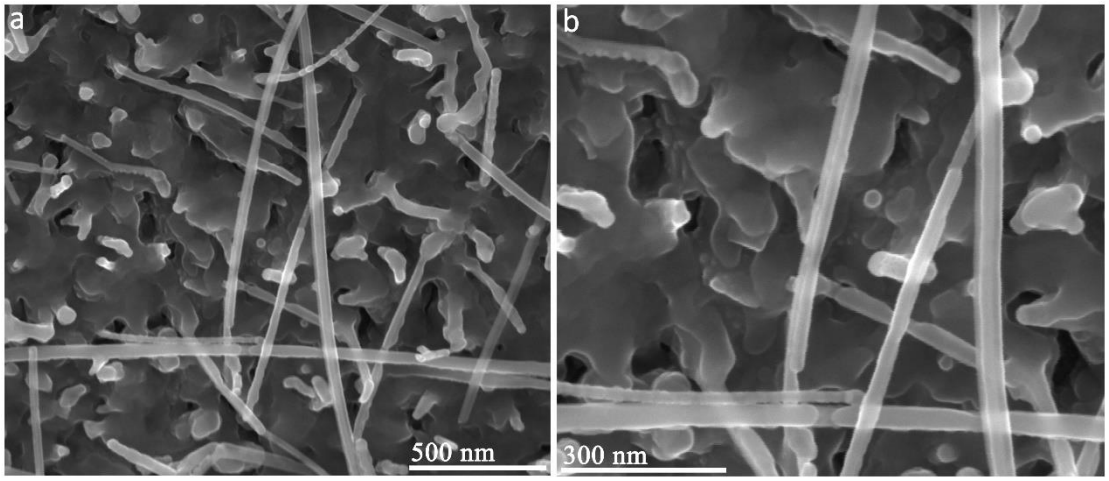

Fig. S4. Ultra-thin InAs-Al nanowires grown under the optimum conditions. (a) SEM image of the ultra-thin InAs-Al nanowires with the Al growth temperature and growth time at ~ -40 °C and 3 min, respectively. (b) Enlarge view of (a). Continuous and smooth half Al shells form on the InAs facets.

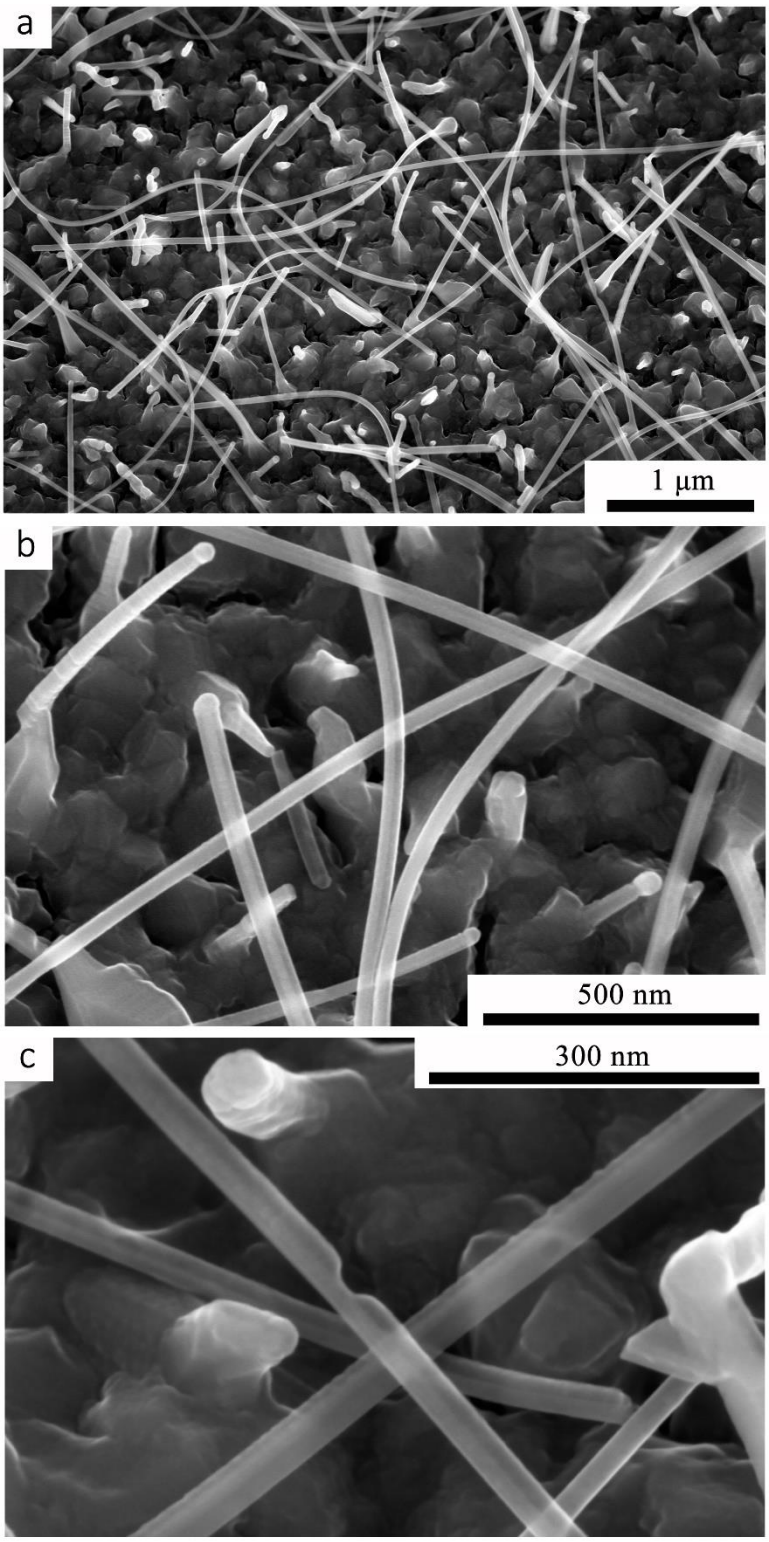

Fig. S5. (a) SEM image of the ultra-thin InAs-Al nanowires grown on Si (111) substrates with the Al shell grown at ~ -40 °C. [(b) and (c)] High magnification SEM images of the ultra-thin InAs-Al nanowires taken from the same sample with (a). All the SEM images were taken at a tilt angle of 25°.

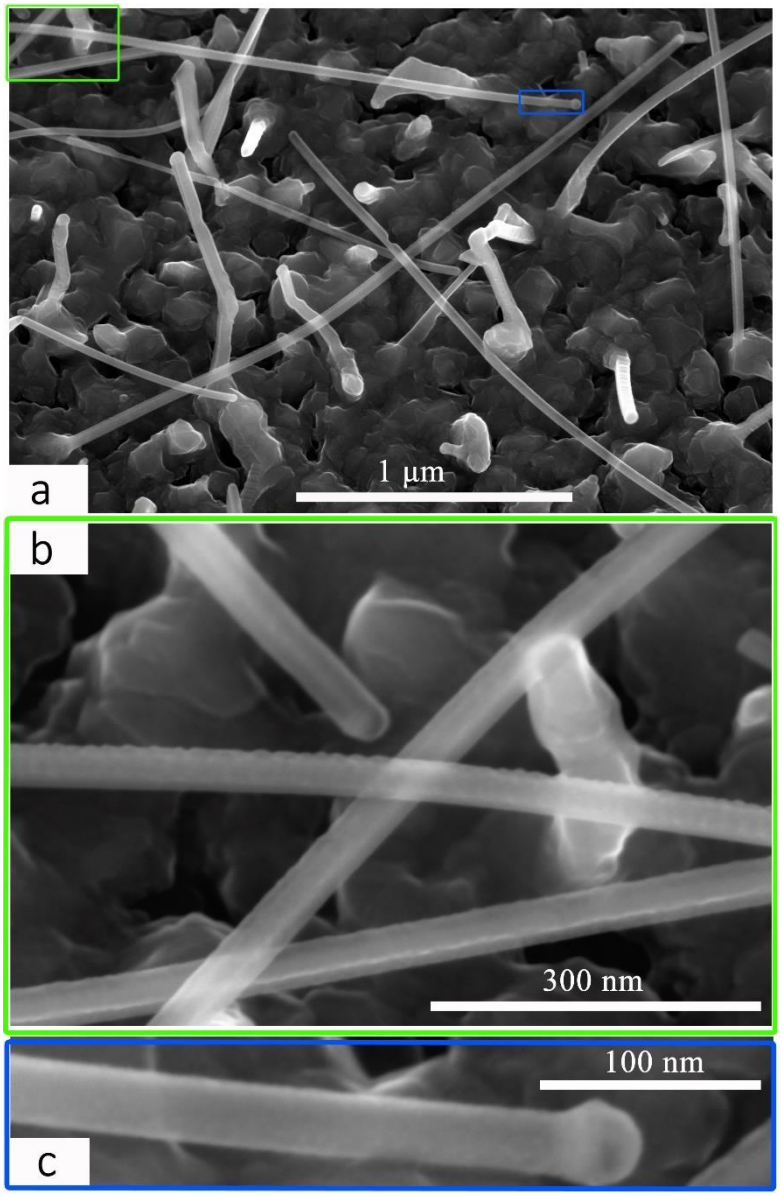

Fig. S6. (a) SEM image of ultra-thin InAs-Al nanowires with the Al shell grown at ~ -40 °C. An InAs-Al nanowire with an obvious enlarged catalyst particle can be observed (blue box). [(b) and (c)] High magnification SEM images of this nanowire indicated by the corresponding color boxes in (a). All the SEM images taken at a tilt angle of 25°.

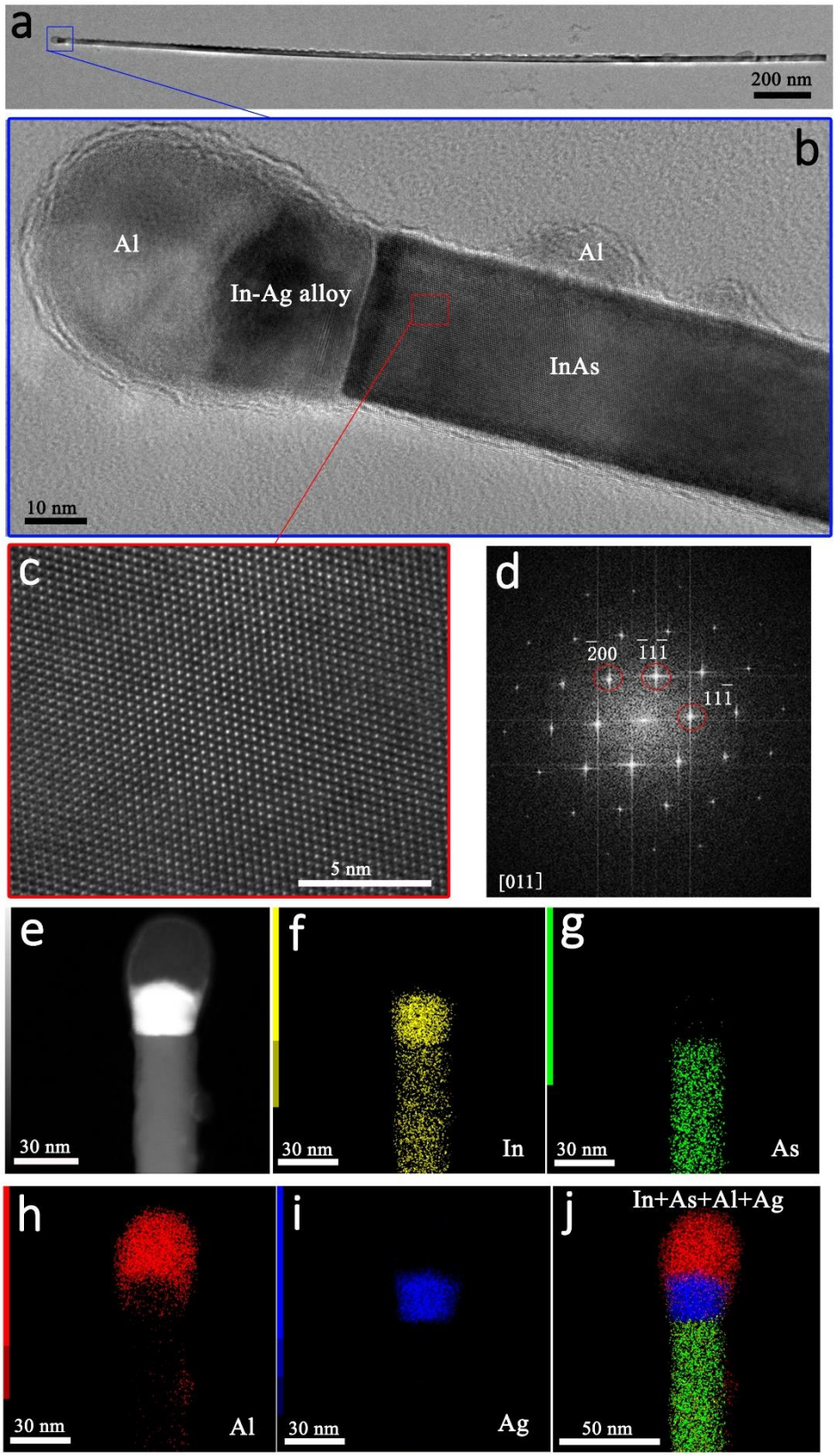

Fig. S7. [(a)-(c)] TEM and high-resolution TEM images of an ultra-thin InAs-Al nanowire with an obvious enlarged catalyst particle. (d) FFT of **c** shows that the InAs nanowire is a pure ZB crystal. (e) HAADF-STEM image taken from the top region of the InAs-Al nanowire. [(f)-(j)] False-color EDS elemental maps of (e).

Section 3 TEM and high-resolution TEM images of the ultra-thin InAs-Al nanowires grown under the optimum conditions

Our work shows that high quality Al shell can be epitaxially grown on the facets of InAs nanowires with all the growth directions we have measured. Figures S8 and S9 show continuous and smooth Al half-shells formed on the facets of ultra-thin InAs nanowires grown along the different directions: <-110> (Fig. S8), <0001> [Fig. S9(a)] and <01-1> [Fig. S9(b)]. All the wires reveal an abrupt and uniform InAs-Al interface and a pure crystal structure, free of stacking faults. It is worth noting that high quality half Al shells can be epitaxially grown on both the pure WZ [Fig. S9(a)] and pure ZB [Fig. S8 and Fig. S9(b)] structured InAs nanowires.

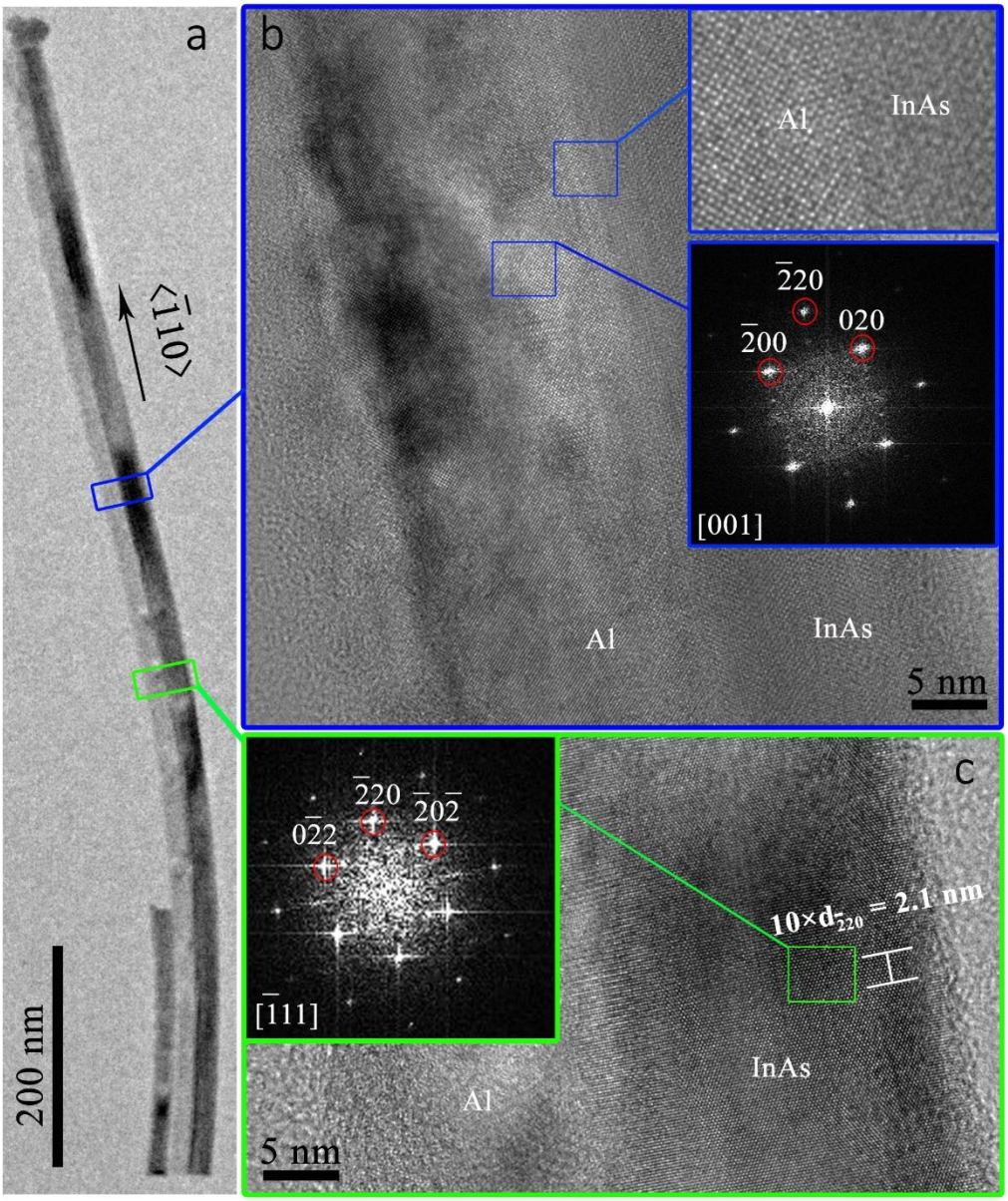

Fig. S8. (a) TEM image of an ultra-thin InAs-Al nanowire with the Al shell grown at ~ -40 °C. (b) and (c) High-resolution TEM images recorded from the blue and green boxes in (a), respectively. The insets in (b) show the InAs-Al interface and the FFT of Al film. The inset in (c) is the FFT of the InAs part. The growth direction of the nanowire is <-110>.

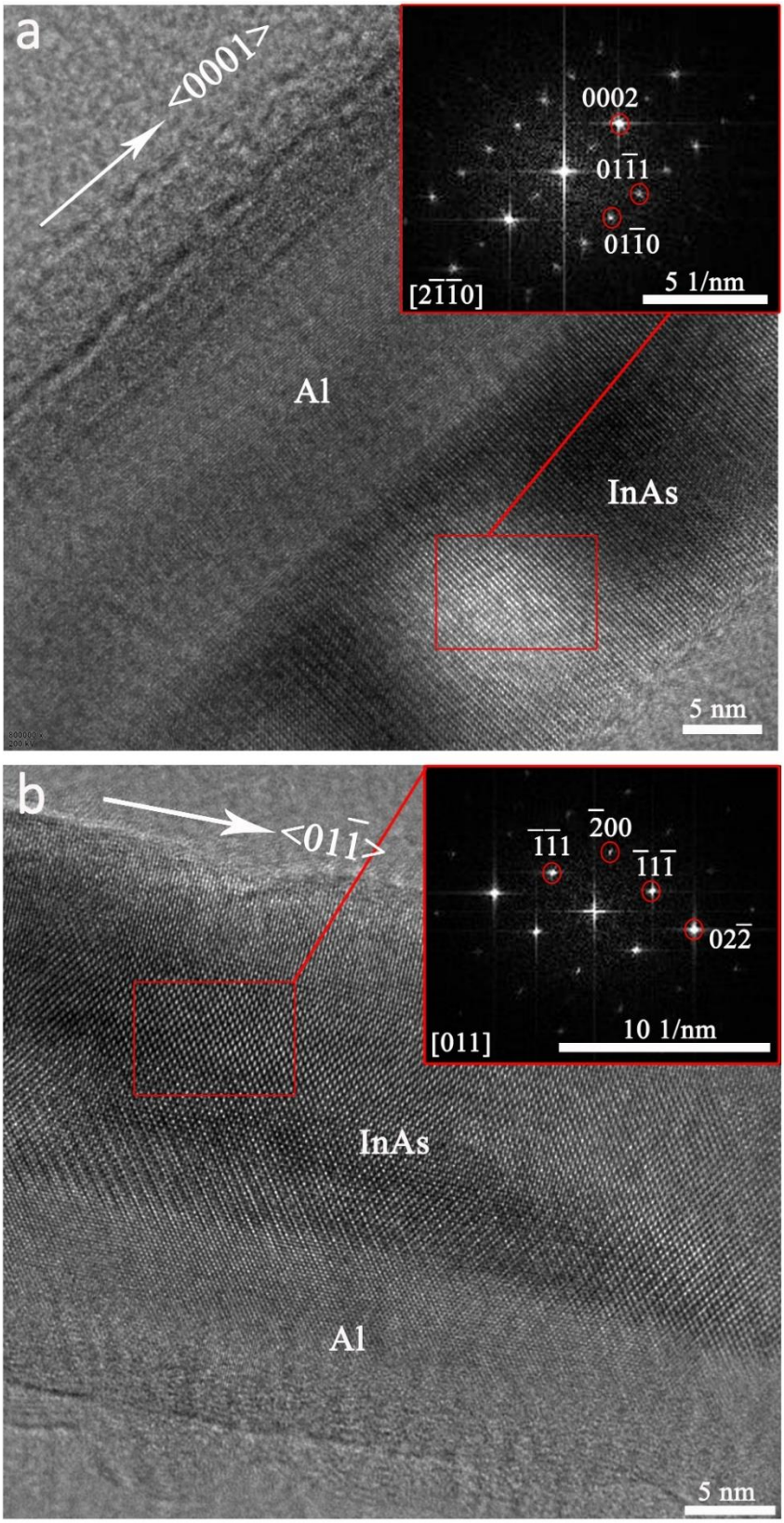

Fig. S9. (a) and (b) High-resolution TEM images of the ultra-thin InAs-Al nanowires with the Al shell grown at ~ -40 °C and along <0001> and <01-1> directions, respectively. The insets in (a) and (b) are the FFT patterns of the corresponding high-resolution TEM images. InAs nanowire in (a) has a pure WZ crystal structure and the nanowire in (b) has a pure ZB crystal structure.

Section 4 ZBP phase diagram of Device A by fixing *B* and scanning gate

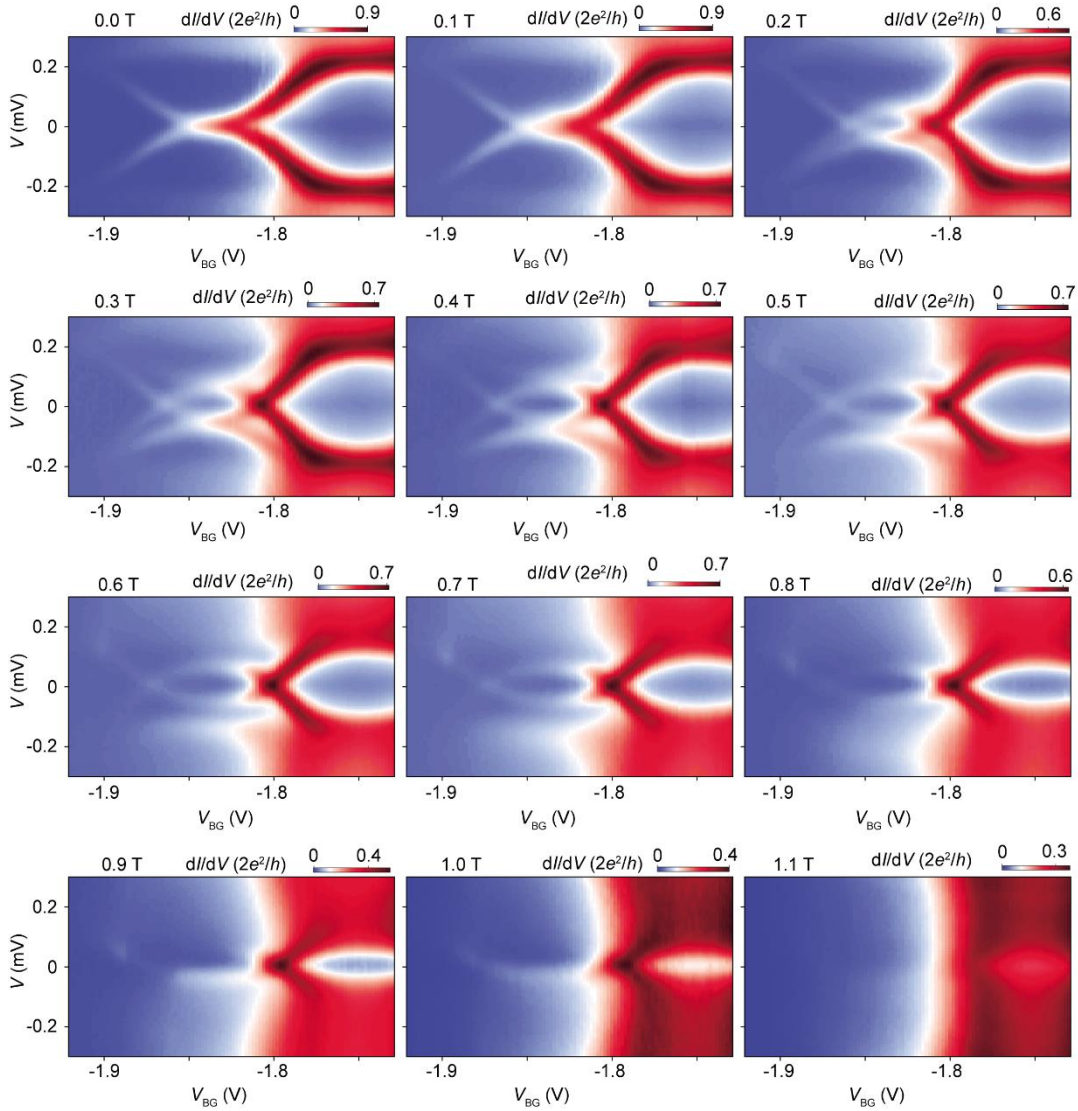

Fig. S10. ZBP phase diagram of Device A by fixing *B* and scanning gate. Each panel represents the V_{BG} dependence of the Andreev bound state at a fixed *B*-field (labeled on the top left, from 0 T to 1.1 T with 0.1 T step). These panels show a continuous evolution of the Andreev bound state. The zero bias peak at finite *B* is due to the Zeeman splitting of the Andreev peak and the peak crossing. The V_{BG} values corresponding to the two crossing points barely change at different *B*-fields. Therefore, by fine-tuning V_{BG} to these two values, we can observe the 'robust' non-split ZBPs in Fig. 4(a) and Fig. 4(e).

Section 5 ZBP phase diagram of Device A by fixing gate and scanning *B*

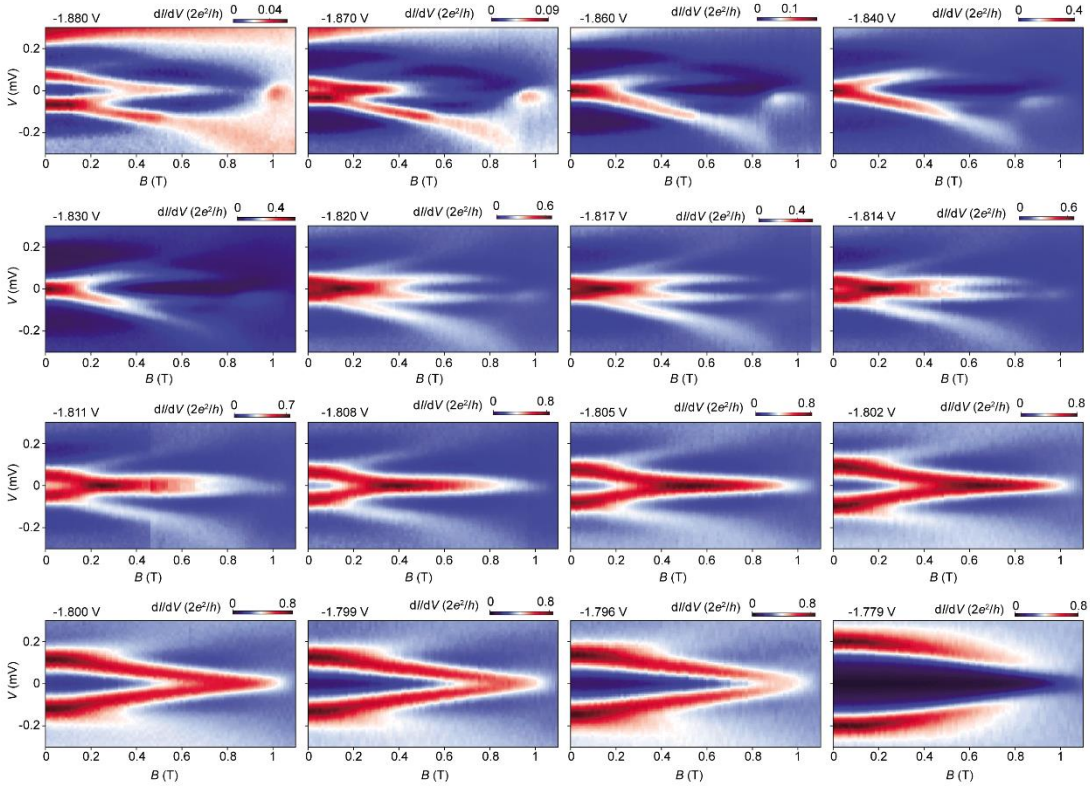

Fig. S11. ZBP phase diagram of Device A by fixing gate and scanning *B*. Each panel represents the *B*-dependence of the Andreev bound state at a fixed V_{BG} (labeled on the top left, from -1.88 V to -1.779 V). These panels show a continuous evolution from one fine-tuned ZBP (-1.88 V) to the other one (-1.808 V), and finally no ZBP observed (-1.779 V) during *B*-sweep.

Section 6 2*e*-Coulomb oscillations in a second island device

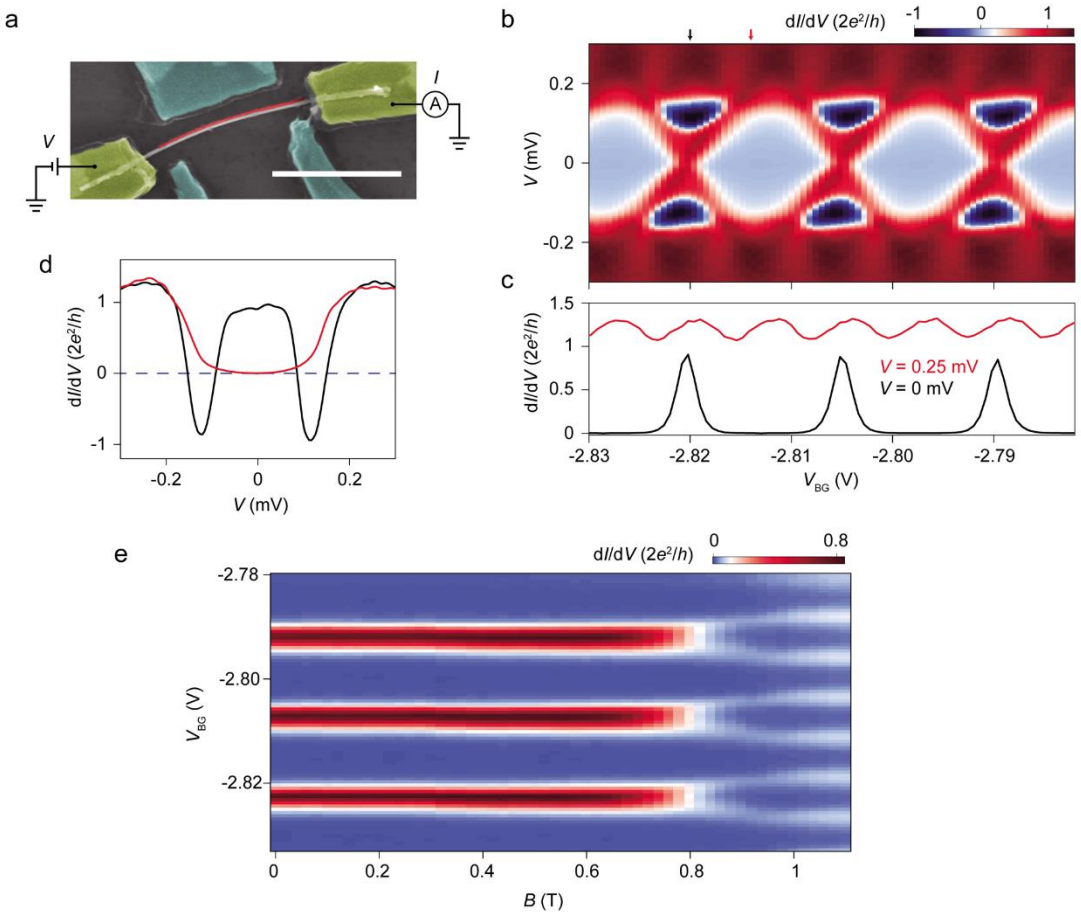

Fig. S12. A second island device (Device C) showing 2*e*- Coulomb oscillations. (a) Device SEM (false-color) and measurement set up. Scale bar is 1 μm. (b) d*I*/d*V* as a function of bias (*V*) and back gate voltage (V_{BG}) resolves the 2*e*- Coulomb diamond. The side gates were kept grounded during the measurement. The diamond size ($V \sim 0.25$ mV) corresponds to a charging energy of ~ 31 μeV. (c) Horizontal line-cuts at $V = 0$ mV (black) and $V = 0.25$ mV (red) resolves the 2*e*- (Cooper pair) and 1*e*- (quasi-particle) oscillations. (d) Vertical line-cuts at Coulomb valley (red) and Coulomb peak degeneracy point (black) with V_{BG} labeled by the arrows in panel (b) with corresponding colors. The onset bias (~ 88 μeV) of the negative differential conductance gives an estimation of $E_O \sim 75$ μeV. (e) d*I*/d*V* at zero bias as a function of V_{BG} and *B* (direction along the nanowire) shows a 2*e*-periodic to 1*e*-periodic transition.

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