

# Supplementary Materials: Giant-capacitance-induced wide quantum Hall plateaus in graphene on LaAlO<sub>3</sub>/SrTiO<sub>3</sub> heterostructures

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## Supplementary notes:

**Note 1: Detail forms of the potential equilibrium equation (Eq. (1) in the main text) under a quantizing magnetic field.**

As mentioned in the main text, Eq. (1) remains valid while under a quantizing magnetic field, but varies in detail form depending on the location of the Fermi level (Fig. 3(b)).

A. When the Fermi level is inside the gap between the neighboring  $N$ th and  $(N+1)$ th LLs of graphene (e.g. region I in Fig. 3(b)), the  $N$ th LL is fully filled,  $E_N \leq E_F \leq E_{N+1}$ , where Eq. (1) can be rewritten as:

$$e(V_g - V_d) = E_F - \frac{e^2}{C_{\text{LAO}}} \frac{-(4N+2)eB}{h} \quad (\text{S1})$$

B. When the Fermi level is in the  $N$ th LL (e.g. region II), the  $N$ th LL is partly filled,  $-(4N+2)eB/h \leq n \leq -(4N-2)eB/h$ , where Eq. (1) can be rewritten as:

$$e(V_g - V_d) = \text{sgn}(N)v_F\sqrt{2e\hbar B|N|} - \frac{e^2}{C_{\text{LAO}}}n \quad (\text{S2})$$

**Note 2: Determination of the upper/lower critical magnetic field of the quantum Hall plateau**

Taking  $\nu=-2$  Hall plateau as an example, the upper critical field  $B_{\text{IU}}$  corresponding to the lower edge of  $N=0$  LL (right plane in Fig. 3(c)) fulfills the following equation:

$$e(V_g - V_d) = -\frac{e^2}{C_{\text{LAO}}}\frac{2eB_{\text{IU}}}{h} \quad (\text{S3})$$

That is,

$$B_{\text{IU}} = -\frac{h}{2e^2}(V_g - V_d)C_{\text{LAO}} = -\frac{h}{2e^2}D = \frac{h}{2e}n_\infty \quad (\text{S4})$$

Here  $n_\infty$  represents the final carrier density of graphene (as indicated in Fig. 3(e)), and  $D = (V_g - V_d)C_{\text{LAO}}$  is the electric displacement.

The lower critical field  $B_{\text{IL}}$  corresponding to the upper edge of  $N=-1$  LL (middle plane in Fig. 3(c)) fulfills the following equation:

$$e(V_g - V_d) = -v_F\sqrt{2e\hbar B_{\text{IL}}} - \frac{e^2}{C_{\text{LAO}}}\frac{2eB_{\text{IL}}}{h} \quad (\text{S5})$$

That is,

$$B_{\text{IL}} = \left[ \frac{hC_{\text{LAO}}}{4e^3} \left( \sqrt{2e\hbar v_F^2 + \frac{-8e^4(V_g - V_d)}{hC_{\text{LAO}}}} - \sqrt{2e\hbar v_F^2} \right) \right]^2 = \left( \frac{-2\pi e h D}{\sqrt{\pi e \hbar^3 v_F^2 C_{\text{LAO}}^2 - 8\pi^2 e^4 h D} + \sqrt{\pi e \hbar^3 v_F^2 C_{\text{LAO}}^2}} \right)^2 \quad (\text{S6})$$

**Note 3: Analysis of the effect of interface states on the quantum Hall plateau**

When there are interface states with constant density of states  $\gamma$  locating between graphene and the gate electrode, both the Fermi levels of the interface states and graphene will vary while applying a gate-voltage. That is, a portion of charges induced by the gate-voltage will be accommodated by the interface states, which acts as an interfacial trap capacitance.<sup>[1]</sup> Figures S4(a,b) show the schematic

band diagram and the corresponding equivalent capacitive circuit, where  $C_Q = e^2(dn/dE_F)$  represents the equivalent quantum capacitance of graphene;  $C_{it} = e^2\gamma$  represents the interfacial trap capacitance;  $C_1$  represents the capacitance between the gate electrode and the interface states, which normally approaches the value of gate capacitance;  $C_2$  represents the capacitance between the interface states and graphene, which normally is quite large.

According to the principle of charge conservation, the equilibrium between the electrochemical potentials of the interface states and graphene can be expressed as:

$$E_F - \frac{e^2}{C_2}n = -\frac{e^2}{C_{it}}n_{it} \quad (S7)$$

Here  $n_{it}$  represents the change of the carrier density of the interface states.

Analogously, the equilibrium between the electrochemical potentials of the interface states and the gate electrode can be expressed as:

$$-\frac{e^2}{C_{it}}n_{it} - \frac{e^2}{C_1}(n + n_{it}) = e(V_g - V_d) \quad (S8)$$

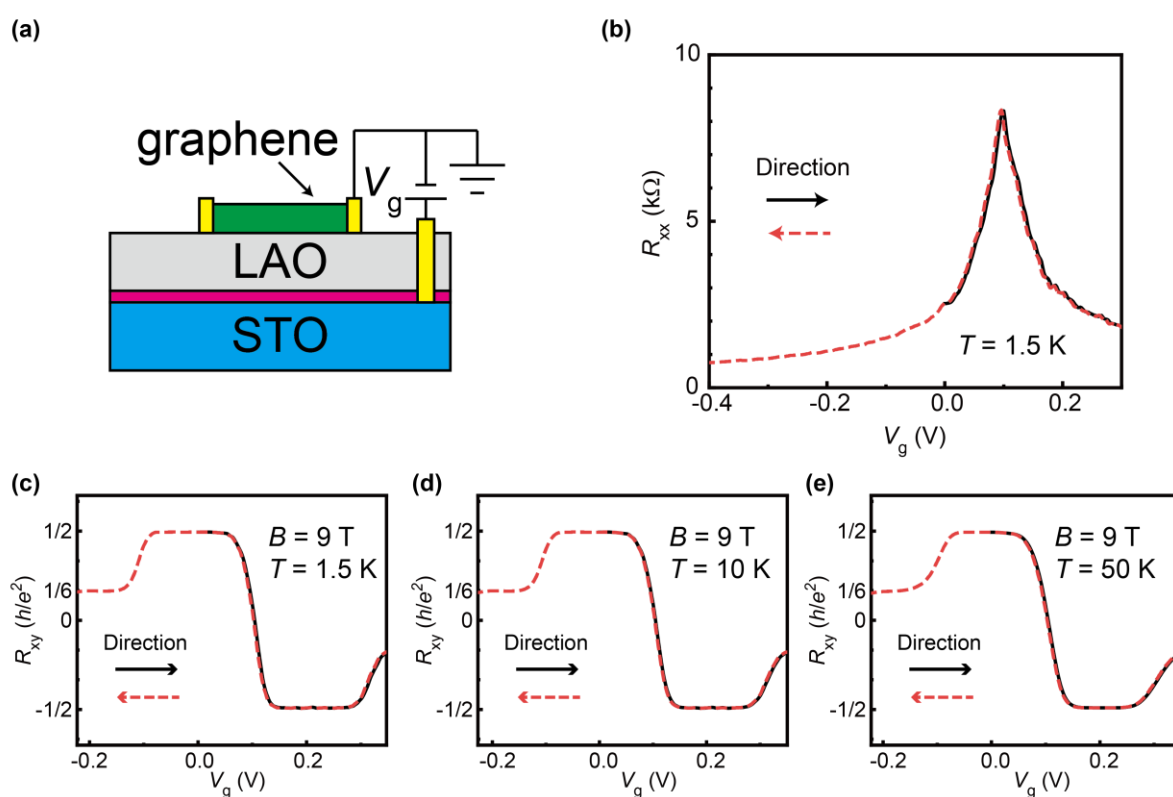
By combining Eqs. (S7) and (S8), we can obtain the following equation:

$$e(V_g - V_d) = \frac{C_1 + C_{it}}{C_1}E_F - \frac{e^2}{\left(\frac{C_1 C_2}{C_1 + C_2 + C_{it}}\right)}n \quad (S9)$$

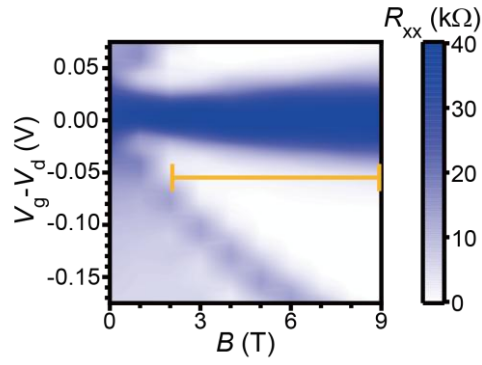
This equation is quite similar to Eq. (1), while the only differences are the coefficients of the terms on the right side. Following the analysis procedures analogous to those described above, the dependence of  $n$  on  $V_g/B$  after involving the effect of the interface states can also be obtained. Especially,  $\Delta V_I$  can be depicted as  $\Delta V_I \sim [(C_1 + C_{it})/C_1] v_F(2\hbar B/e)^{1/2}$ . Compared to the calculated value without interface states, i.e.  $v_F(2\hbar B/e)^{1/2}$ ,  $\Delta V_I$  would be enlarged by  $(C_1 + C_{it})/C_1$  times. However, as shown in Figs. 3(d) and S4(c), the experimental obtained  $\Delta V_I$  are nearly identical with  $v_F(2\hbar B/e)^{1/2}$ ,

implying the negligible effect of interface states on the widening of the quantum Hall plateau in G-LAO-STO.

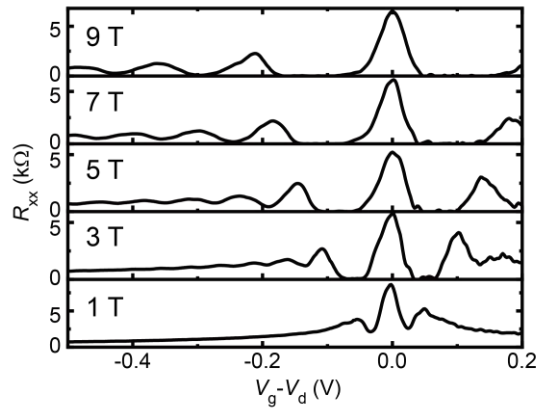
**Supplementary figures:**



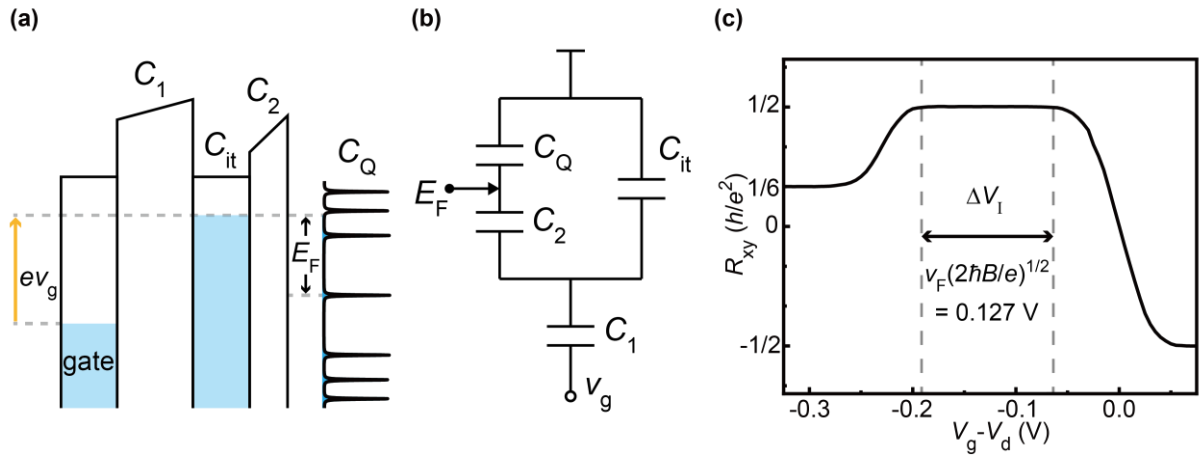
**Fig. S1.** (a) Schematic illustration of the G-LAO-STO device, in which the LAO layer and the conducting LAO/STO interface are utilized as the dielectric layer and the gate electrode, respectively. (b)  $R_{xx}$  vs  $V_g$  curves for G-LAO-STO-#2 obtained at 1.5 K under zero magnetic field. (c-e)  $R_{xy}$  vs  $V_g$  curves for G-LAO-STO-#2 under 9 T magnetic field obtained at 1.5 K, 10 K and 50 K, respectively. The arrows indicate the directions of  $V_g$  sweeping.



**Fig. S2.**  $R_{xx}$  as a function of  $B$  and  $(V_g - V_d)$  measured at 1.5 K for G-LAO-STO-#1.  $V_d$  is the gate-voltage corresponding to the Dirac point of graphene. These data were taken simultaneously with Fig. 1(e) in the main text.



**Fig. S3.**  $(V_g - V_d)$  dependent  $R_{xx}$  at 1.5 K under different magnetic fields in G-LAO-STO-#2.



**Fig. S4.** (a) The schematic band diagram of the G-LAO-STO while involving the effect of interface states. (b) Equivalent capacitive circuit of (a). (c)  $(V_g - V_d)$  dependent  $R_{xy}$  under measured at  $B=9 \text{ T}$  and  $T=1.5 \text{ K}$  for G-LAO-STO-#1. The dashed range represents the simulated gate-voltage range of region I ( $\Delta V_I$ ) without interface states.

### Supplementary references:

- [1] Takase K, Tanabe S, Sasaki S, Hibino H and Muraki K 2012 *Phys. Rev. B* **86** 165435