CHIN.PHYS.LETT. Vol. 25, No. 5 (2008) 1908

Memory Effect of Metal–Insulator–Silicon Capacitors with $SiO_2/HfO_2/Al_2O_3$ Dielectrics *

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(Received 13 December 2007)

Charge trapping characteristics of the metal–insulator–silicon (MIS) capacitors with $SiO_2/HfO_2/Al_2O_3$ stacked dielectrics are investigated for memory applications. A capacitance-voltage hysteresis memory window as large as 7.3 V is achieved for the gate voltage sweeping of ±12 V, and a flat-band voltage shift of 1.5 V is observed in terms of programming under 5 V and 1 ms. Furthermore, the time- and voltage-dependent charge trapping characteristics are also demonstrated, the former is related to charge trapping saturation and the latter is ascribed to variable tunnelling barriers for electron injecting and discharging under different voltages.

PACS: 85.25.Hv, 77.55.+f

Recently, poly-silicon-oxide–nitride-oxide–silicon (SONOS) memory structures have drawn great attention as a promising candidate to replace the conventional poly-silicon floating gate memory.[1−8] This is ascribed to the reason that the charges stored in the poly-silicon floating gate (like a continuous conducting plate) can easily discharge through a single defect in the tunnel oxide,[9] hereby leading to inferior data retention characteristics. Therefore, to improve the data retention of memory device, a floating gate composed of discrete charge storage nodes (for example, silicon nitride) is much preferred. Further, to achieve an increased programming speed and a lower voltage operation, it is of practice to reduce the tunnel oxide thickness. However, this seriously degrades the charge retention capability. Lee *et al.*[10] have reported that lower program/erase voltages and faster erase speed can be achieved by using high-dielectric-constant (high-k) Al_2O_3 to replace the blocking SiO_2 in the SONOS structure, which is attributed to an enhanced electric field across the tunnel layer under a program/erase mode. It is well known that for multi-stacked insulators under a constant gate voltage, the electric field across each insulator is dependant on its dielectric constant. As a result, it is anticipated that the programme speed can be increased further if both silicon nitride layer and the blocking SiO_2 layer are replaced by other high-k dielectrics. It is reported that HfO_2 has a high dielectric constant of about 25 and appropriate conduction band offset to Si (about 1.5 eV),[11,12] moreover, its typical polycrystalline texture ensures sufficient defects present in the HfO_2 film, which is thus a potential charge trapping layer. Al_2O_3 has a large band-gap (about 8 eV) as well as amorphous and dense texture in the temperature range of interest,[12,13] and thus is a promising blocking layer to prevent carriers from tunnelling though it.

In this Letter, we use atomic-layer-deposited HfO_2 as a charge trapping layer and Al_2O_3 as a blocking layer. Charge trapping characteristics of the metal-insulator-silicon (MIS) capacitor with $SiO_2/HfO_2/Al_2O_3$ dielectrics are investigated, and a larger capacitance-voltage hysteresis memory window is demonstrated in comparison with that with SiO_2/Al_2O_3 dielectrics. Moreover, time- and voltage-dependent programme properties of the memory capacitor are characterized and the underlying mechanisms are addressed as well.

In this study, (100)-orientated p-type silicon wafers with a resistivity of 4–8 Ωcm were used as the starting substrates. After cleaning by the method of Standard Radio Corporation of America, the remnant chemical oxide was removed by diluted hydrofluoric acid rinse. Then a film of about 2.7 nm SiO_2 was grown by dry oxidation in a furnace at 800°C. Subsequently, an 8 nm layer of HfO_2 was deposited from tetrakis(ethylmethylamino)-hafnium (TEMAH) and water at 300°C by atomic layer deposition (ALD), followed by a 10 nm Al_2O_3 film that was deposited from trimethylaluminium (TMA) and water at 300°C using ALD technique. Finally, around 1 μm aluminium film was evaporated on top of the dielectric as the electrode plate, and the Si substrate backside was also coated with a layer of aluminium for ohmic contact after the native oxide removal. The capacitor size with a gate area of 6.28×10^{-6} cm^2 was obtained after photolithography and wet etching. The resulting MIS capacitor with $SiO_2/HfO_2/Al_2O_3$ dielectrics

*Supported by the National High-Technology Research and Development Programme of China under Grant No 2006AA03Z307, the Key Project of Ministry of Education of China under Grant No 108052, the National Basic Research Programme of China under Grant No 2006CB302703, and the National Natural Science Foundation of China under Grant No 90607023.

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is represented by MAHOS. For comparison, the MIS capacitor with SiO_2/Al_2O_3 dielectrics was also fabricated and defined as MAOS.

The thickness of SiO_2 was measured by an ellipsometer. The thicknesses of HfO_2 and Al_2O_3 were controlled by reaction cycles based on the measured growth rates (i.e., about 0.1 nm per cycle in the present experiments), which were deduced from the thickness measurements by an ellipsometer and high-resolution transmission electron microcopy. The capacitance-voltage (C–V) measurements were performed on an Agilent 4284A precision LCR meter at room temperature. The programme pulses were generated by an Agilent 81110A pulse pattern generator.

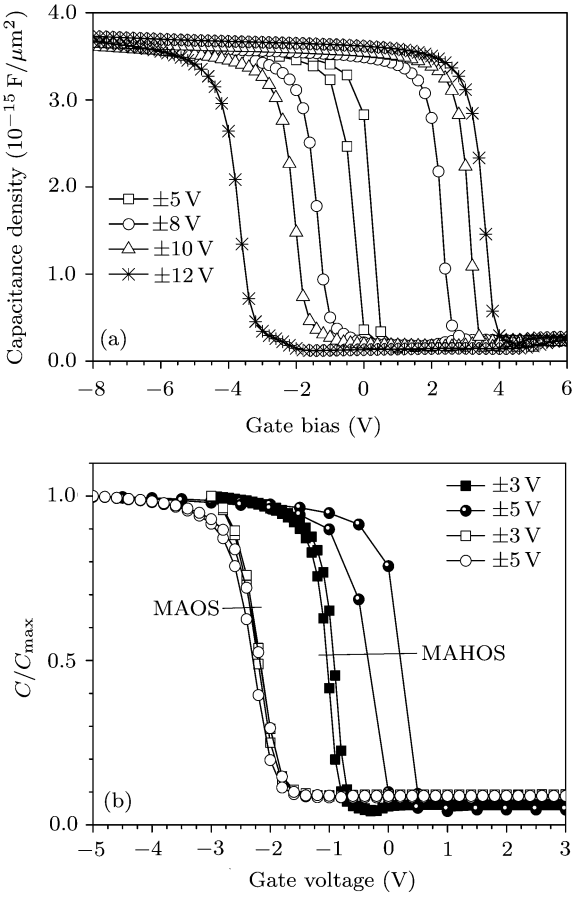


Fig. 1. (a) High-frequency (1 MHz) C–V hysteresis curves corresponding to different gate voltage sweeping ranges for the MAHOS capacitor. (b) Comparison of high-frequency (1 MHz) C–V hysteresis curves for the MAHOS and MAOS capacitors.

Figure 1(a) presents the high-frequency (1 MHz) C–V curves of the MAHOS capacitor by bidirectional voltage sweeping. It is found that the C–V hysteresis window increases obviously with increment of the maximum sweeping gate voltage. This reveals an obvious memory effect of the MAHOS capacitor. In terms of the sweeping gate voltage of ±12 V, a hysteresis memory window as large as 7.3 V is achieved. For comparison, high-frequency (1 MHz) C–V hysteresis curves of the MAOS and MAHOS capacitors are shown in Fig. 1(b). It is observed that the MAOS capacitor exhibits a much smaller hysteresis window than the MAHOS capacitor for a sweeping gate voltage of ±5 V. Our previous experiments also show that the MIS capacitor with a single ALD Al_2O_3 dielectric presents a negligible hysteresis about 5 mV.[14] Therefore, it can be concluded that the marked charge trapping effect of the MAHOS capacitor should be attributed to the embedded HfO_2 layer, which provides enough defects (or traps) for charge trapping.

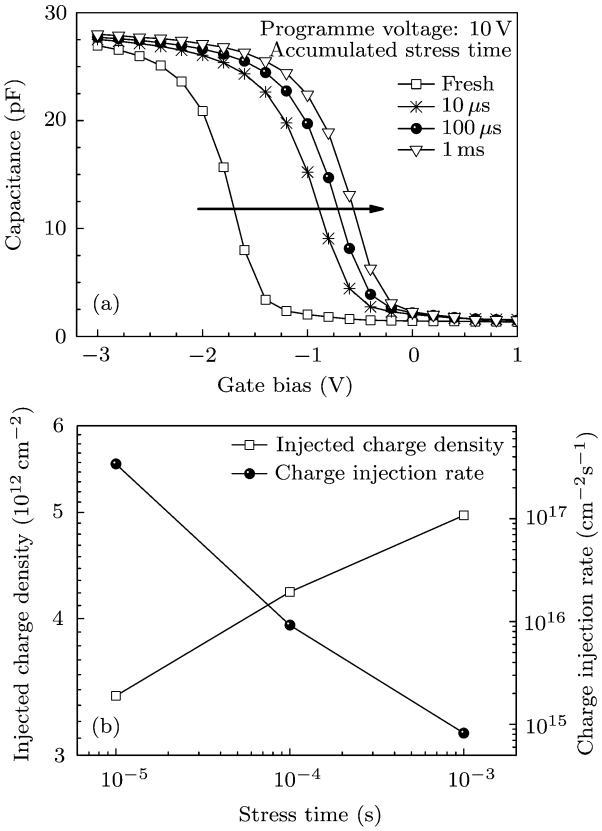


Fig. 2. (a) Dependence of C-V curves on the accumulated stress time (10 μs–1 ms) under 10 V in terms of the MAHOS capacitor. (b) Trapped charge density and average charge injection rate versus the accumulated stress time under 10 V.

To observe the charge trapping characteristics as a function of stress (programme) time under a constant gate voltage, the MAHOS capacitor is stressed at +10 V for different durations, and the resulting C–V curves are shown in Fig. 2(a). It is found that the resultant C–V curve exhibits a flat-band voltage shift (ΔV_{fb}) of 0.78 V for the initial stress time of 10 μs. When the accumulated stress time is increased to 100 μs and even 1 ms, the resulting C–V curve presents a small ΔV_{fb} increase by 0.19 V and 0.17 V, respectively, which is likely due to charge trap-

ping saturation. This indicates that charge trapping occurs principally at the beginning of electrical stress, followed by slow charge trapping. On the assumption that all the trapped charges are located in the middle of the HfO_2 layer, the trapped charge density N_t can be calculated in the case of different stress time from the equation[15]

$$N_t = \frac{\Delta V_{fb}}{q\left(\frac{T_{HfO_2}}{2\varepsilon_0 k_{HfO_2}} + \frac{T_{BL}}{\varepsilon_0 k_{Al_2O_3}}\right)},$$

where T_{HfO_2} and T_{BL} represent the thickness of the HfO_2 layer and Al_2O_3 layer, respectively; ε_0 is the permittivity in vacuum; q is the elementary charge; k is the relative dielectric constant. As illustrated in Fig. 2(b), the injected charge density increases from $3.4 \times 10^{12}\,\mathrm{cm}^{-2}$ to $4.97 \times 10^{12}\,\mathrm{cm}^{-2}$ when prolonging the accumulated stress time from $10\,\mu$s to 1 ms. The average charge injection rate is about $3.4 \times 10^{17}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ during the initial programme time of $10\,\mu$s, and declines dramatically to 9.22×10^{15} and $8.22 \times 10^{14}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ corresponding to the following stress times of 90 and 900 μs, respectively.

Figure 3 shows the programming characteristics of the memory capacitor as a function of stress voltage in the case of a constant stress time (1 ms). Regarding a stress voltage of 3 V, we cannot observe any ΔV_{fb}. When the stress voltage is increased to 5 V, the resulting C–V curve demonstrates a significant shift in the direction of positive voltage, and the obtained ΔV_{fb} is close to 1.5 V. However, when the stress voltage is raised to 10 V, the resultant C–V curve does not exhibit a further shift towards a positive voltage but an obvious movement towards a negative voltage. This means the negative charges trapped in the HfO_2 film are reduced. As the stress voltage increases to 12 V, a more shift towards a negative voltage is observed. The above phenomena can be explained according to the energy band diagram in Fig. 4. When the gate is biased under a positive voltage, the electrons can inject into the HfO_2 layer from the p-type substrate (defined as J_b), meanwhile some of the trapped electrons in the HfO_2 layer can also tunnel through the Al_2O_3 layer into the gate (defined as J_g). Therefore, the magnitude of ΔV_{fb} is determined by the two competitive processes of J_b and J_g. In the case of the stress voltage of 3 V, the inversion layer electron density in the substrate is quite small, and the amount of electrons tunnelling through SiO_2 is negligible, i.e., J_b is negligible and J_g as well. Therefore, ΔV_{fb} approaches zero due to very limited electrons trapped in the HfO_2 layer. As the gate bias is increased to 5 V, see Fig. 4(b), the inversion layer electron density increases large enough, the electric field drop across the SiO_2 layer becomes larger, hereby leading to a significant increase in J_b due to the Fowler–Nordheim (F-N) tunnelling mechanism. However, a small quantity of electrons trapped in the HfO_2 layer can tunnel directly to the gate because of a large tunnel thickness of the Al_2O_3 layer. Therefore, J_b is dominant in the case of 5 V stressing, i.e., the injected electrons from the substrate can be effectively trapped in the HfO_2

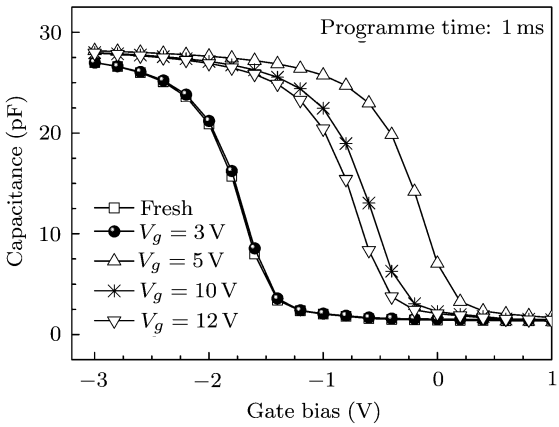


Fig. 3. Evolution of C–V curves as a function of the programme voltage V_g in the case of a constant programme time 1 ms.

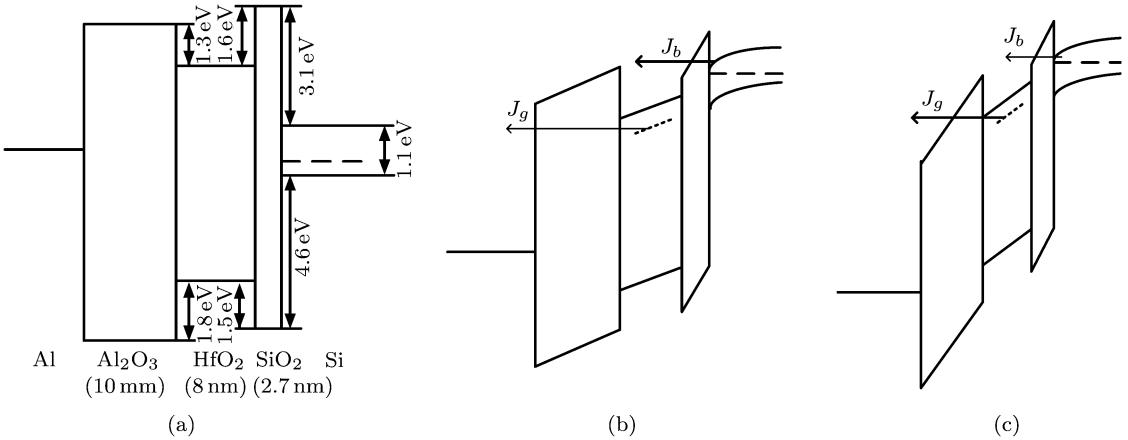


Fig. 4. Schematic energy band diagrams of the MAHOS capacitor: (a) without external electric field, (b) 5 V programme voltage, (c) 10 V programme voltage.

layer. When the programme voltage is further increased to 10 V, see Fig. 4(c), the electric field dropped on the Al_2O_3 layer becomes so large that the trapped electrons in the HfO_2 layer can tunnel to the gate through a small triangle barrier by F-N tunnelling, i.e., J_g increases significantly compared to the programme voltage of 5 V. Therefore, the net electrons trapped in the HfO_2 layer reduce, hereby resulting in a decrease of ΔV_{fb}.

In conclusion, the charge trapping characteristics of the MIS capacitor with a dielectric structure of $SiO_2/HfO_2/Al_2O_3$ have been investigated. The obtained results reveal that the MAHOS capacitor exhibits obvious memory effects such as a large hysteresis memory window and a fast electron injection rate in the initial programme time. The time- and voltage-dependent charge trapping characteristics are discussed according to charge trapping saturation and variable electron tunnelling barriers under different voltages.

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