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Epitaxial Growth of High-Quality Silicon Films on Double-Layer Porous Silicon *

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The epitaxial growth of a high-quality silicon layer on double-layer porous silicon by ultra-high vacuum/chemical vapour deposition has been reported. The two-step anodization process results in a double-layer porous silicon structure with a different porosity. This double-layer porous silicon structure and an extended low-temperature annealing in a vacuum system was found to be helpful in subsequent silicon epitaxial growth. X-ray diffraction, cross-sectional transmission electron microscopy and spreading resistance testing were used in this work to study the properties of epitaxial silicon layers grown on the double-layer porous silicon. The results show that the epitaxial silicon layer is of good crystallinity and the same orientation with the silicon substrate and the porous silicon layer.

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Silicon epitaxial layer growth on porous silicon (PS) can be applied to form silicon-based solar cells[1] and silicon-on-insulator (SOI) wafers, i.e. full isolation by porous oxidized silicon (FIPOS) [2−4] and epitaxial layer transfer (ELTRAN).[5,6] ELTRAN technology allows the thickness of the top silicon layer in SOI to be easily controlled and to be made quite uniform.

Silicon epitaxial layer growth on PS is a key process in ELTRAN technology. A number of different methods, such as molecular beam epitaxy (MBE)[2−4] and conventional chemical vapour deposition,[5] have been reported. In this work, the silicon epitaxial growth on PS employs ultra-high vacuum/chemical vapour deposition (UHV/CVD) technology. UHV/CVD exhibits some advantages over other methods. Silicon MBE has received little attention until very recently, because of its complexity and noncompatibility with device fabrication requirements.[7] Conventional CVD is usually performed in a temperature range of 800−1040°C.[5] The high temperature may be harmful to the PS microstructure. However, in the UHV/CVD process, the growth temperature can be reduced to about 740°C.

In this letter, it has been found that the PS microstructure and the surface treatment of PS prior to the silicon epitaxial growth are the key steps in a successful UHV/CVD technology. Using PS with a smaller pore size as a substrate can result in higher quality epitaxial Si (epi-Si) since it is better in terms of supplying enough nucleation sites during subsequent UHV/CVD silicon epitaxy. On the other hand, the PS layer will be used as a sacrificial layer in the ELTRA–SOI process. The larger pore size of the PS is easier to etch away. To fulfil both requirements, a double-layer PS system with a different porosity was fabricated on a heavy doped p-type silicon wafer using a two-step anodization process and was used as the substrate for silicon epitaxy. The top layer of the PS has a smaller pore size while the underlying PS layer has a larger pore size.

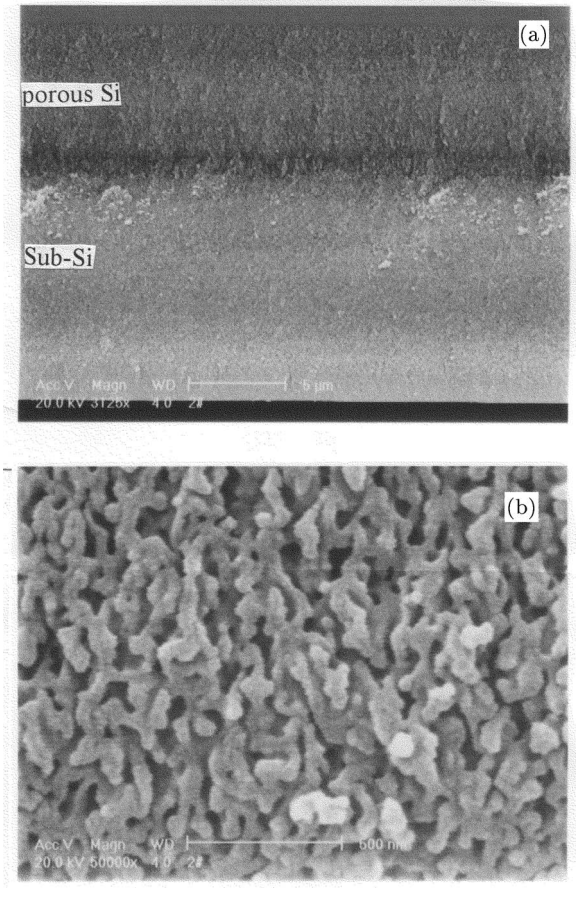


Fig. 1. Cross-sectional SEM images of PS: (a) PS/Si structure; (b) enlarged image of the PS layer.

UHV/CVD silicon growth techniques rely strongly on the treatment of an ultra-clean surface of PS. Prior

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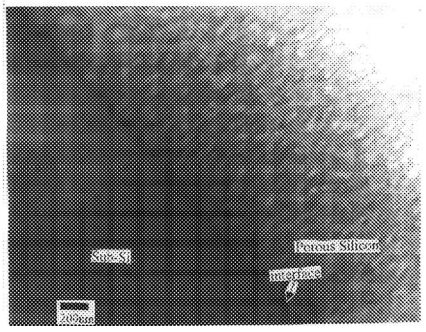


Fig. 2 XTEM image of the PS/sub-Si structure near the interface.

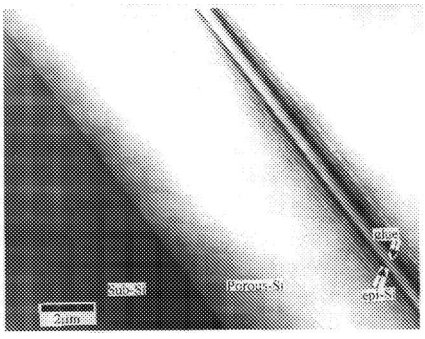


Fig. 3. XTEM image of the epi-Si/PS/sub-Si structure.

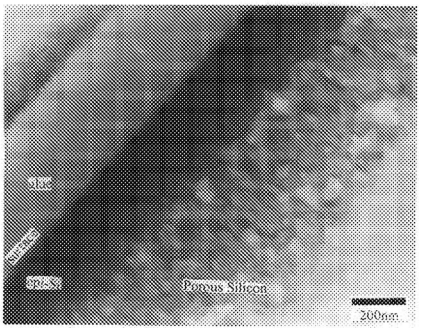


Fig. 4. XTEM image of the epi-Si/PS.

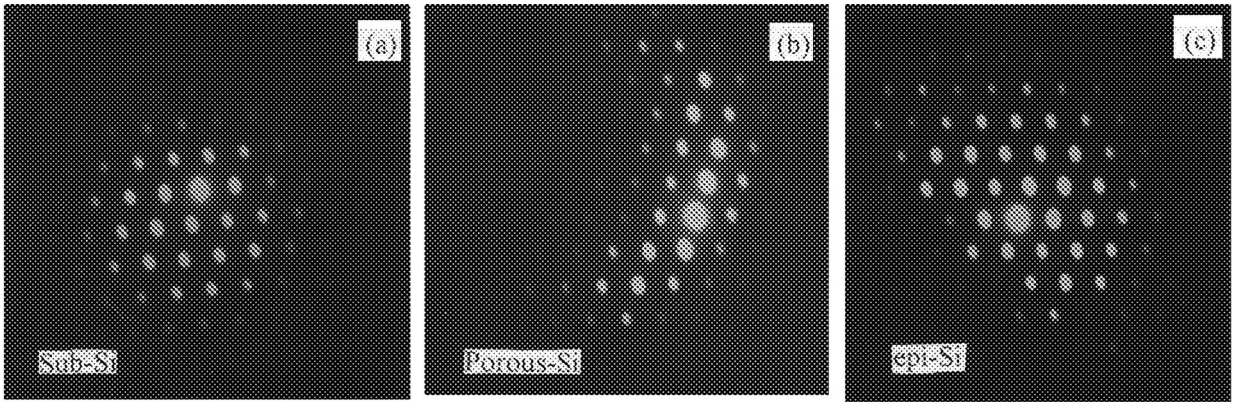


Fig. 5. Electron diffraction patterns of (a) sub-Si, (b) porous Si and (c) epi-Si.

to epitaxial growth, an extended low-temperature annealing in a vacuum system was proposed to stabilize the PS and clean the surface of the PS.

Boron-doped p-type wafers with a resistivity of $0.003-0.007\,\Omega\cdot$ cm were anodized in an HF electrolyte with a composition of HF(42 wt.%):C_2H_5OH = 4:1. Wafers were first anodized at $10\,mA/cm^2$ for 40 s, followed by an anodization at $30\,mA/cm^2$ for 15 min without changing the electrolyte. The change of current density was gradual to avoid any abrupt change in the PS microstructure. Such a PS formation condition results in a double-layer PS structure with a different porosity. In order to stabilize the PS layer and clean the surface of the wafers with PS, the surface treatment of wafers with a double-layer PS was adopted. The wafers were kept at 300°C in 1.33×10 Pa vacuum system for 8 h after anodization. Then the wafers were loaded into the UHV/CVD chamber immediately after it was taken out of a 10:1 H_2O/HF dip and rinsed with de-ionized (DI) water. The wafer was introduced into the growth chamber together with hydrogen. At first, the growth chamber was kept a constant temperature of 800°C and was pumped down to a base pressure of below 10 Torr. The native oxide can be removed by heating the wafer to 800°C to vaporize the oxide. After 800°C thermal cleaning, the temperature of the growth chamber decreased to 740°C and the source gases (silane) for silicon epi-layer growth were subsequently fed into the growth chamber. The operated growth pressure was maintained at 10 Torr.

The crystallographic quality and configuration of epi-Si films grown on double-layer PS were investigated by x-ray diffraction (XRD), cross-sectional transmission electron microscopy (XTEM) and spreading resistance analysis. The results show that good a Si epi-layer with low doping was obtained.

Figure 1 shows cross-sectional scanning electron microscopy (SEM) images of a double-layer PS formed on a P^+-type substrate. The top layer of the PS has lower porosity and the underlying PS layer has higher porosity. The interface between the PS and silicon substrate is investigated by XTEM using a Philips EM430 TEM system. As shown in Fig. 2, the interface between the porous layer and silicon substrate is quite rough and the thickness of the porous layer is about $6.2\,\mu$m.

Figure 3 shows an XTEM image of an epitaxial Si-film/PS/Si-substrate structure. The epi-Si film and

PS layer have thicknesses of 260 nm and 6.2 μm, respectively. Figure 4 shows an XTEM micrograph of an epi-Si layer over a PS layer. The top layer above the epi-Si layer is a glue layer. The epi-Si layer is uniform and the surface of the epi-Si layer is flat. Defects such as dislocation and stacking faults are not observed in the epi-Si layer during XTEM observation. A transmission electron diffraction pattern analysis of the Si/PS/Si structure has been made to estimate the crystallographic property of top epi-Si layer. The diameter of the selected area is 0.6 μm. Figures 5(a)–5(c) show the electron diffraction patterns for the substrate, PS layer and epi-Si layer, respectively. It indicates that all three electron diffraction patterns are the patterns along the $\langle 110 \rangle$ axes. Results show that the crystalline skeletons of the epi-Si and PS layers have the same orientation as the silicon substrate. Figure 5 also indicates that the epi-Si layer has good crystalline property and quality.

Fig. 6(a) shows the XRD spectra of the epi-Si film grown on PS, and Fig. 6(b) shows the XRD spectra of the silicon substrate. XRD results show that (a) and (b) have the same diffraction peaks along the Si(111) substrate orientation, indicating a single-crystalline structure of the epi-Si layer. It also indicates that the epi-Si layer has the same orientation as the silicon substrate, in agreement with the XTEM results. The peak of (a) is slightly narrower than (b). It is considered that there is a PS layer between the epi-Si layer and the substrate.

A spreading resistance testing (Fig. 7) shows the impurity profile of the epi-Si film and the PS layer after silicon epitaxial growth. The results indicate that the resistivity of the epi-Si layer is higher than $10^2\Omega\cdot$cm and the resistivity of the PS layer is 500 times higher than $10^2\Omega\cdot$cm. The $10^2\Omega\cdot$cm impurity level meets the requirement for direct device fabrication.

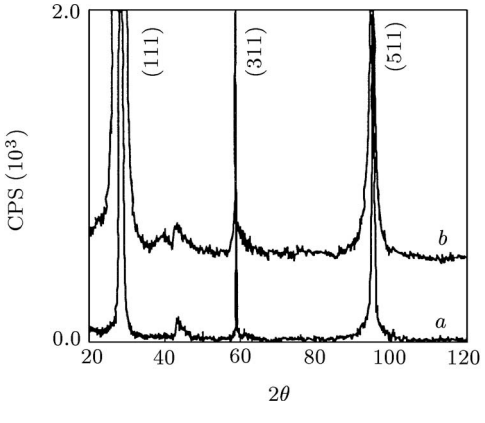


Fig. 6. XRD spectra of sub-Si (a) and epi-Si (b).

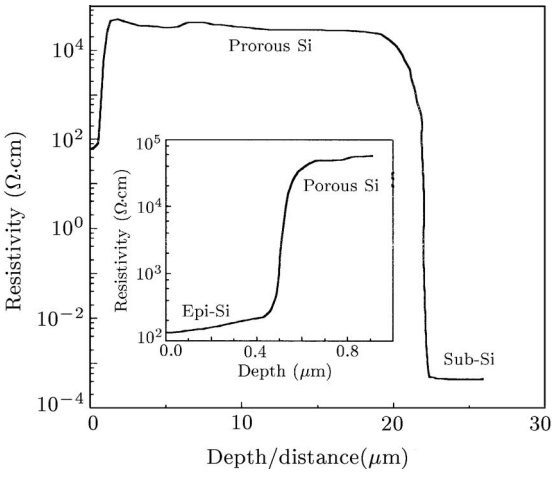


Fig. 7. Spreading resistance profile of the epi-Si/porous-Si/sub-Si structure. The inset shows the detailed profile near the epi-Si/PS interface.

In conclusion, a double-layer porous silicon structure with a lower porosity layer and an underlying higher porosity layer was fabricated on a p-type silicon wafer using a two-step anodization process, and was used as the substrate for silicon epitaxy. It was found that the top porous silicon layer has lower porosity which is better for subsequent epitaxy and the underlying porous silicon layer has higher porosity, which is easier to etch away for ELTRAN technology requirements. It was also found that the extended annealing at low temperature in a vacuum system prior to epitaxial growth was helpful in stabilizing the porous silicon and eliminating contamination. XRD, SEM, XTEM and spreading resistance testing were used to characterize the films. The results show that a good silicon epitaxial layer grown on porous silicon with low doping using UHV/CVD has been obtained.

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