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Microstructural and Electrical Properties of ZrO_2 Thin Films Prepared on silicon on Insulator with Thin Top silicon *

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Amorphous zirconia thin films were deposited directly on silicon-on-insulator (SOI) substrates with thin top silicon by ultra-high vacuum electron beam evaporation. Spreading resistance profile and scanning transmission–electron microscopy (TEM) were used to detect the interface quality and microstructure, revealing that the interface between the zirconium oxide films and top silicon was abrupt and clear. The films kept to be amorphous up to the rapid thermal temperature of 700° C for 300 s, but arriving at 700° C an unknown interfacial product appeared, which was probably $ZrSi_xO_y$. High frequency capacitance-voltage ($C-V$) characteristics at 1 MHz performed on metal–oxide–SOI structure revealed that this interfacial product exhibited good electrical properties of zirconia thin films. When the annealing temperature increased from 600° C to 700° C, flat voltage V_{FB} changed from -2.451 to -1.741 eV, showing the improvement in the quality of the films. The cumulative region capacitance decreased from $3.058 \times 10^{-11} F$ to $3.012 \times 10^{-11} F$, indicating increasing equivalent oxide thickness, which is in agreement with the result of high-resolution cross-sectional TEM.

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silicon-on-insulator (SOI) technology has attracted much attention due to its inherent advantages over bulk counterpart such as radiation hardness, high speed/low power operation, low parasitic capacitance, absence of latch-up, lower off-state leakage and reduced gate delays, as well as possibility to achieve three-dimensional devices.[1,2] For partially depleted SOI metal–oxide–semiconductor field effect transistors (MOSFETs), the depletion charge could hardly be transported timely and completely due to lack of body contact, and then the float-body effect arises.[3] Fully depleted SOI MOSFETs, however, could avoid the float body effect because the region above the buried oxide layer is very thin and could not collect charge during transistor operation. They also have low junction capacitance, which allows the transistor run faster. Therefore, the SOI substrate with thin top silicon attracts more interests.[4]

At the same time, the continual scaling of semiconductor devices result in excessive direct tunnelling current through traditional SiO_2 gate oxide, especially when the thickness is now approaching 10–15 Å on bulk silicon.[5] This is not a sharp physical limit, but rather the point beyond which the leakage current due to tunnelling (about 1–10 A/cm^2) becomes the dominant leakage mechanism in current device designs.[6,7] Also, the drive current and transconductance of scaled MOSFETs tend to saturate or decline with decreasing the gate oxide thickness. Furthermore, ultrathin gate oxides have several inherent scattering mechanisms, such as poly gate/oxide interface roughness scattering, remote impurity scattering, interface plasmon scattering and scattering associated with wavefunction penetration.[8] Thus, one of the best solutions is to overcome this difficulty and use a physically thicker gate dielectric with a higher value of dielectric constant (K). ZrO_2 is one of the best candidates of high K gate dielectric due to its excellent properties.[9,10] In this study, we deposited ZrO_2 thin films directly on thin top silicon SOI substrates and studied the their microstructural and electrical properties.

The evaporation apparatus was a UMS 500 P ultra-high vacuum film plating apparatus made in Germany by Balzers Company, which included three parts: vacuum system, control system and chambers. The SOI substrates were provided by SOITEC Company. The SOI substrate was fabricated by the following process: the p-type Si (100) substrate was implanted by H ions with an energy of 90 keV and a dose of $1.79 \times 10^{18}\,cm^{-3}$, and then using the Smart-Cut technology and chemical mechanical polishing to prepare the final SOI materials. They were cleaned by supersonic vibration in high purity acetone and alcohol (100%) for 10 min, respectively, followed by rinsing in deionized water. The final step was to quickly immerse the SOI substrates in 5 vol% HF solution to remove native oxide on the surface. To reduce the negative influence of huge pressure difference between inner and outer chamber, the SOI substrates was first introduced into the pre-vacuum chamber and then transferred to the main chamber. The background pressure of the main chamber was evacu-

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ated to 10^{-6}–10^{-7} Pa. High purity (99.9%) solid sintered ZrO_2 pellet was used as the evaporation source. The substrate could be rotated to make sure the uniformity of thin films evaporated. The substrate temperature was kept at room temperature during the deposition process. The distance between evaporation source and substrate was 50–60 cm and the substrates can be rotated to ensure the uniformity of the deposited materials. The evaporation rate was controlled by quartz crystal monitor and set at 1 Å·s^{-1}. Some as-deposited samples were rapidly thermal annealed (RTA) in O_2 ambient at 300–700°C for 300 s and the flow rate of O_2 was controlled at 5 L/min. The samples were examined by various characterization techniques, such as spreading resistance profile (SRP), x-ray photoelectron spectroscopy (XPS), atomic force microscope (AFM) and high-resolution cross-sectional transmission–electron microscopy (HR-XTEM). High frequency $C-V$ characteristics at 1 MHz were performed using an HP 4194 A analyser. Metal-oxide SOI capacitors were formed by electron beam evaporation of Al on ZrO_2 thin films to form the top electrode. Al contact was also made to the backside surface of SOI substrates.

The SRP is mainly used to generate resistivity depth profiles. The spreading resistance probe consists of two carefully aligned probes that are stepped along the semiconductor surface. The voltage between the probes during measurement is kept at around 5 mV to reduce the effect of contact resistance.[11] Fig. 1 exhibits the information of both thickness and resistivity distributions of the 600°C-annealed sample. Interfaces of ZrO_2/Si, Top Si/SiO_2, SiO_2/Si substrate were very clear and abrupt. The resistivity of the films was much more than $10^8\Omega$·cm, which is the upper limit of apparatus. The thickness of the films was estimated to be 50 nm.

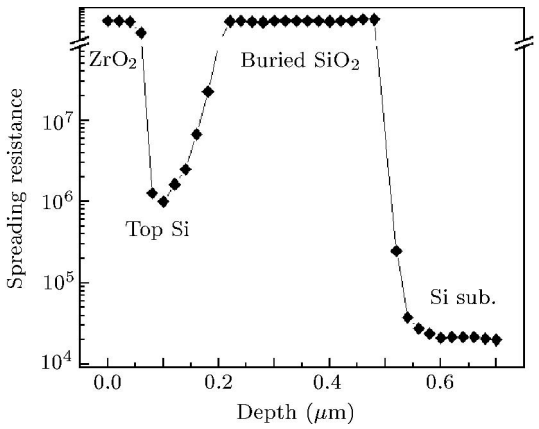

Fig. 1. Spreading resistance profile of ZrO_2 thin films on silicon on insulator substrates rapid thermal annealed in O_2 at 600°C for 300 s.

XPS, also known as electron spectroscopy for chemical analysis (ESCA), is the high-energy version of the photoelectric effect discovered by Hertz in 1887.[11] Electrons can be emitted from any orbital with photoemission occurring for x-ray energies exceeding the binding energy. C 1*s* at 284.6 eV was used as the reference binding energy. The results not shown here proved zirconium was fully oxidized in its +4 state. The atomic ratio of Zr and O was calculated to be Zr:O=1:2.2. This value is higher than that in the case of ZrO_2, i.e., Zr:O=1:2. This is probably due to the absorption of the impurities from ambient to which the annealed samples was exposed, such as CO_2, O_2, water vapour and so on.

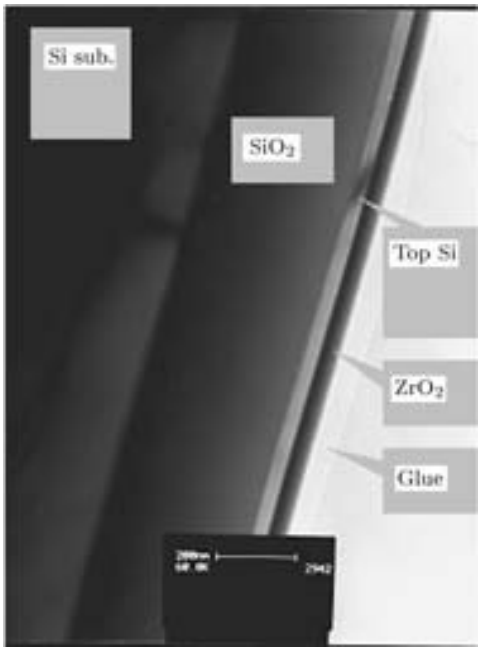

Fig. 2. Cross-sectional transmission–electron microscopy of the 600°C-annealed sample.

HR-TEM can give structural information on the atomic size level, known as lattice imaging, and has become very important for interface analysis. For example, oxide–semiconductor, metal–semiconductor and semiconductor–semiconductor interfaces have benefited a great deal from HR-TEM images.[11] The microstructure and the quality of the interface between ZrO_2 thin films and top Si were analysed by the HR-XTEM, as shown in Figs. 2 and 3. The images were taken in the annular dark field (ADF) to image directly the film chemical composition. The high-angle ADF signal is dominated by Rutherford-like scattering to large angles, resulting in a signal that is strongly dependent on density ρ and atomic number Z, scaling roughly as $\rho Z^{1.7}$. Consequently, SiO_2 will appear darker than Si in an ADF image, while zirconium oxide or silicate will appear brighter than Si. As we could find that high quality of the interface was achieved when the annealing temperatures was 600°C, as shown in Fig. 2, and the

ZrO_2 thin films were amorphous, and uniform, as appeared in Fig. 3. Because polycrystalline dielectrics have a non-uniform leakage distribution and can give rise to large statistical variation for nanometre devices across the chip, and the grain boundaries tend to be easy pathways of leakage.[12] Furthermore, the crystallization of an oxide causes a significant increase in surface roughness.[13] Therefore, replacement gate strategies have been proposed to prevent crystallization and deleterious effect of mass and electrical transport along grain boundaries.[14]

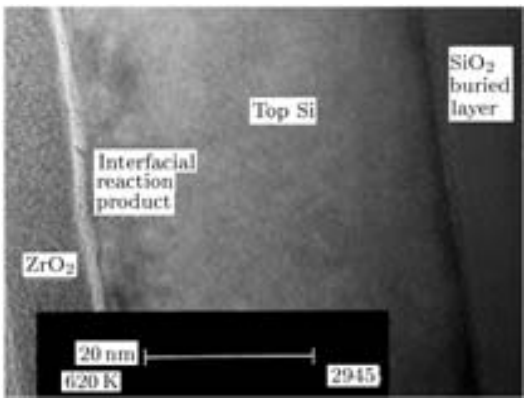

Fig. 3. High resolution cross-sectional transmission–electron microscopy of the 700°C-annealed sample.

The chemical compositions of the thin films were corroborated by the elements weight and atomic ratio that they were nearly stoichiometric (Zr:O=1:2.28, atomic%). Whereas an unknown thin oxide product layer was also detected when the annealing temperature was raised to 700°C, as shown in Fig. 3, the thickness of which is about 1 nm. The component of the oxide product is not exactly known yet, which may be $ZrSi_xO_y$.[15,16] Both the upper interface with ZrO_2 and the lower interface with Si were almost atomically flat. This is reasonable because our annealing treatments had an excess of oxygen, with the O_2 flow rate of 5L/min, and it is known that oxygen has a high diffusivity in ZrO_2. Thus, it is not the product of chemical reaction between ZrO_2 and Si, but the product of the reaction between oxygen, diffused from annealing environment, and Si substrate. In fact, this layer has been proved to be of great importance to reduce the interface state density.[15] The thickness of the zirconia thin films elicited was about 47 nm, which was nearly in agreement with the results of SRP.

High frequency $C-V$ characteristics were performed at 1 MHz. Figure 4 shows the high frequency $C-V$ curves of 600 and 700°C RTA samples. With increasing the rapid thermal temperature, the cumulative region capacitance decreased from 3.058×10^{-11} F to 3.012×10^{-11} F. According to $C_{\max}=\dfrac{\varepsilon A}{d}$ and $EOT=3.9\div\dfrac{\varepsilon}{d}$, the EOT of ZrO_2 thin films on thin top silicon SOI substrate decreased with increasing rapid thermal temperature, which is due to growth of a thin layer of interfacial product. This is in agreement with the results of the HR-XTEM. The dielectric constants of Zirconia thin films were calculated according to the formula $C_{\max}=\varepsilon_0\varepsilon_r A/d$, where $\varepsilon_0=8.85\times10^{-12}\,\mathrm{F\cdot m^{-1}}$, the thickness of the films was taken to be 47 nm from the result of XTEM and the area of the Al electrode was calculated with the diameter of 0.3 mm. The dielectric constants of the 600°C and 700°C annealed samples were 23.0 and 22.7, respectively, which corroborated further the formation of interfacial reaction product when the annealing temperature was raised to 700°C. The flat band of the annealed samples was elicited using the method in Ref. [11]. The results revealed that when the rapid thermal temperature was raised from 600 to 700°C, V_{FB} changed from -2.451–-1.741 eV. As is known to all, there are two reasons for V_{FB} to deviate from the ideal value 0 eV: one is the work function difference between gate electrode and gate dielectrics; the other is the charges existed in the gate dielectric or on the interface. Because the O ions have high diffusion speed in ZrO_2 thin films, when the O ions moved, there were some more cavities with positive charge left, which led to the negative deviation of flat band voltages. Therefore, we could safely say that increasing the annealing temperature was well performed to reduce the charges, and the interfacial product was helpful to improve the electrical properties of ZrO_2 thin films, which are consistent with other reports.[15,16]

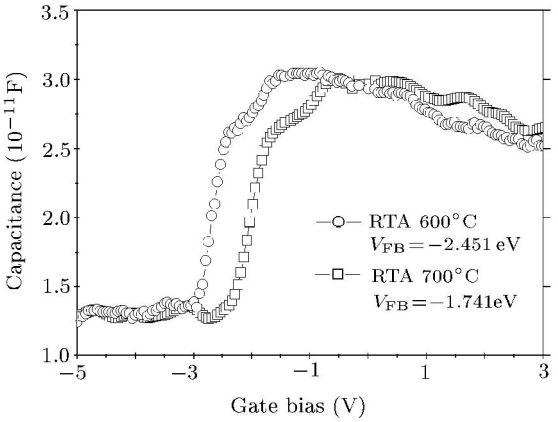

Fig. 4. High frequency capacitance voltage curves of the 600 and 700°C rapid thermal annealed samples.

In summary, we have investigated the ZrO_2 thin films on thin top silicon SOI. The result shows that the films have high quality interfaces between ZrO_2 thin films and the top silicon layer of SOI substrates. Thermal stability of the nanoscale amorphous films have been studied by RTA experiment, and the films remain in its amorphous state after RTA in O_2 environment at 300–700°C for 300 s. An oxide product layer between

ZrO_2 thin films and the top silicon layer was detected, which is probably due to the reaction between oxygen, diffused from annealing environment, and Si substrate. High frequency $C-V$ characteristics displayed that this interfacial product is helpful to improve the electrical properties of the ZrO_2 thin films on thin top silicon SOI substrates. Therefore, it is promising to use ZrO_2 as high K gate dielectrics in fully depleted SOI MOSFET, although further work is needed.

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