In-Memory Probabilistic Computing Using Gate-Tunable Layer Pseudospins in van der Waals Heterostructures

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Layer pseudospins, exhibiting quantum coherence and precise multistate controllability, present significant potential for the advancement of future computing technologies. In this work, we propose an in-memory probabilistic computing scheme based on the electrical manipulation of layer pseudospins in layered materials, by exploiting the interaction between real spins and layer pseudospins. This approach demonstrates near-linear time complexity, achieving computation speeds approximately five times faster than conventional probabilistic computing schemes for the Maximum Cut (MAXCUT) optimization problem. Moreover, we demonstrate that our proposed scheme can realize a computation speed comparable to quantum computing when the MAXCUT problem with a large number of nodes is considered. Our results highlight the potential of layer degree of freedom as a new information carrier for building up advanced computational systems.

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1. Introduction. Probabilistic computing[1–6] is a computational paradigm that utilizes probabilistic bits (p-bits), which stochastically fluctuate between 0 and 1, to address combinatorial optimization problems efficiently. This approach is expected to overcome challenges that conventional computers face, such as inference,[7–9] invertible logic,[5,10,11] sampling,[12–15] and optimization,[12,16–20] drawing on principles from neural networks.[21–23] P-bits have been demonstrated in systems including magnetic tunnel junctions,[5,16,24] volatile memristors,[25–27] and bistable resistors,[28] utilizing their inherent bistability and stochastic nature. However, inherent stochasticity can lead to oscillations around the global minimum, impeding convergence and causing entrapment in local minima. To reach the global optimum, statistical analysis of multiple outcomes is required. Note that the Boltzmann distribution, which has been used to model system states in probabilistic computing, inherently favors the global minimum, yet it also increases computational complexity.

Layertronics, a parallel development to spintronics, is grounded in insights from its extensive study.[29–31] At the core of this concept lies layer pseudospin, a quantum degree of freedom that captures the behavior of electronic states across layers in layered materials like graphene and transition metal dichalcogenides (TMDs), facilitating the exploration of interlayer coupling,[32,33] quantum coherence,[34,35] and electronic interactions.[36–38] Electronic states localized in the upper or lower layer are represented by pseudospin up or down, respectively, corresponding to electrical polarization. This polarization ($\boldsymbol{P}$) couples directly to an external electric field ($\boldsymbol{E}$), enabling dynamic control of layer pseudospin and electrically tunable randomness. Data can also be stored by using the layer pseudospin degree of freedom in van der Waals heterostructures, enabling in-memory probabilistic computing. Layer pseudospins enable gate-controlled, nonvolatile multistate programmability—distinct from spin/valley systems that rely on magnetic fields or optical stimuli—while offering enhanced robustness against disorder in van der Waals (vdW) heterostructures. Their vertical 3D integration and inherent analog stochasticity uniquely bridge probabilistic computing and quantum-inspired algorithms, surpassing planar spin/valley platforms in scalability and efficiency for combinatorial optimization.[39–41]

In this work, we propose a theoretical framework for in-memory probabilistic computing based on layertronics in a dual-gated vdW heterostructure. This framework enables gate-controlled p-bits, which are organized into an asynchronous network to solve a four-node Maximum Cut (MAXCUT) optimization problem. Our results indicate near-linear time complexity, with computational efficiency superior to that of conventional probabilistic computing and comparable to quantum computing. This work provides a scalable hardware solution for exploiting the layer

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pseudospin degree of freedom as a new information carrier to address complex optimization and sampling problems.

2. Effective Model. We model a two-dimensional vdW heterostructure under gate control using a tight-binding approach.[42–44] The p-bit building block consists of a layered ferromagnet (FM) stacked with an AB-stacked bilayer of TMDs [Fig. 1(a)]. The effective Hamiltonian for this gated bilayer TMDs/FM heterostructure is given by

$$H(\boldsymbol{k}) = \begin{pmatrix} h_1(\boldsymbol{k}) & T \\ T^\dagger & h_2(\boldsymbol{k}) \end{pmatrix}, \tag{1}$$

where $h_l(\boldsymbol{k})$ denotes the intralayer Hamiltonian for each layer l ($l = 1, 2$) and T is the interlayer coupling. The intralayer Hamiltonians are expressed as

$$h_l(\boldsymbol{k}) = \epsilon(\boldsymbol{k}) + h_l^{\mathrm{R}}(\boldsymbol{k}) + h_l^{\mathrm{I}}(\boldsymbol{k}) + h_l^{\mathrm{E}},$$

where $\epsilon(\boldsymbol{k})$ is the kinetic energy, h_l^{E} is the onsite potential from the out-of-plane electric field controlled by gate voltages, and $T = t_\perp \mathrm{I}_{2\times 2}$ is the interlayer hopping matrix. The stacking of chalcogen atoms breaks inversion symmetry within each TMD layer, resulting in an Ising spin-orbit coupling (SOC) term, $h_l^{\mathrm{I}}(\boldsymbol{k})$. The Rashba SOC term, $h_l^{\mathrm{R}}(\boldsymbol{k})$, originates from the interface-induced SOC and inversion asymmetry at the TMDs/FM interface (see details in the Supplementary Material[45]).

The coupling of multiple degrees of freedom is central to our framework. We consider a layered FM with perpendicular magnetic anisotropy, coupled to bilayer TMDs with strong intralayer SOC (λ_{SO}) and interlayer coupling ($t_\perp$). In our vdW heterostructure, spin and valley are coupled to the layer pseudospin. Due to the 180° in-plane rotation of the lower layer, out-of-plane spin splitting depends on both valley and layer pseudospins, as shown in Fig. 1(a). The interlayer hopping incurs an energy cost of $2\lambda_{\mathrm{SO}}$. When $2\lambda_{\mathrm{SO}} > t_\perp$, the charge carrier localizes in either the upper or lower layer, determined by its valley and spin state. In this regime, spin is locked to layer pseudospin within a given valley, enabling electrical control of spin via gate-controlled layer polarization and spin accumulation.

We then discuss the role of Rashba SOC at the FM-bilayer TMDs interface in generating spin polarization and manipulating the layertronic p-bit. By applying an in-plane charge current, we can induce spin polarization along the y-direction at the interface, which diffuses into the FM layer, generating an in-plane spin-orbit torque. This torque switches the perpendicular magnetization between stable (UP or DOWN, corresponding to the 1 and 0 states of the p-bit, respectively) and unstable states aligned along the y-axis [Fig. 1(a)]. Thermal fluctuations cause random switching between UP and DOWN states with equal probability [Fig. 1(b)]. This switching probability can be modulated by electrically controlled spin polarization [Figs. 1(c)–1(h)]. In the absence of an electric field, the net z-spin is zero, resulting in equal probabilities for the UP and DOWN states [Figs. 1(e)–1(f)]. A negative field induces upward spin accumulation in the TMD bilayer, generating an out-of-plane spin-orbit torque in the FM layer [Figs. 1(c)–1(d)], favoring the UP state and driving the p-bit to the 1 state with nearly 100% probability. Conversely, a positive electric field induces downward spin polarization, favoring the DOWN state [Figs. 1(g)–1(h)], causing the p-bit to favor the 0 state with a probability approaching 100%. These electrically tunable probabilities provide a flexible mechanism for designing stochastic behavior, crucial for in-memory p-bits capable of processing and storing information.

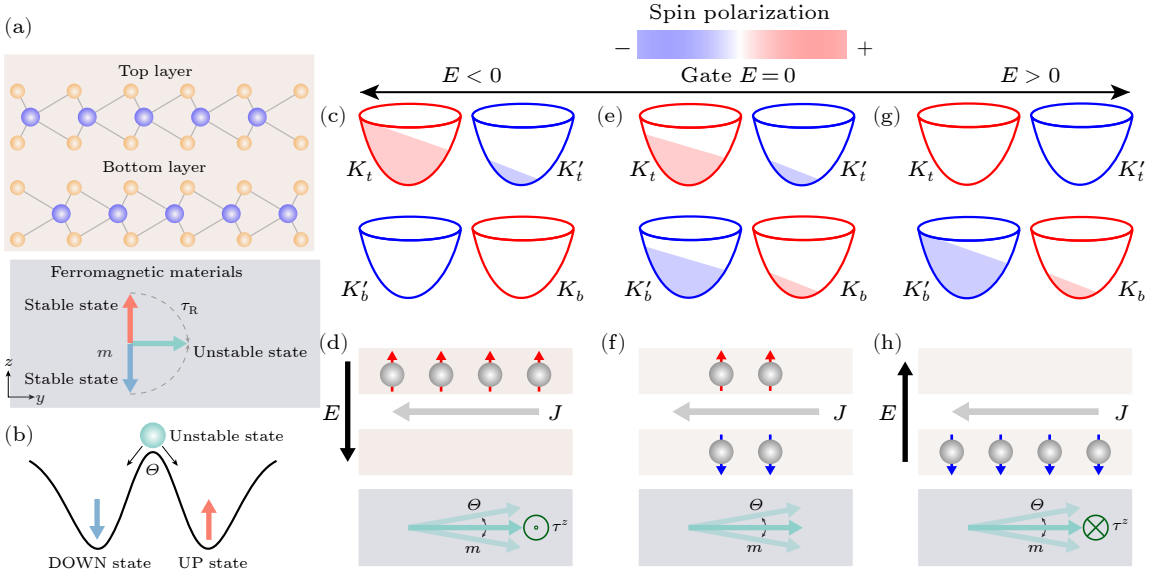

Fig. 1. (a) Schematic illustrations of the AB stacking bilayer TMDs/FM heterojunction. (b) Schematic of a double potential well characterizes the stable states (UP and DOWN) and the unstable state of the FM layer. Due to thermal perturbation, the unstable state randomly fluctuates to the UP state or the DOWN state with the same probability. (c)–(d), (e)–(f), and (g)–(h) represent the electrically controlled net spin accumulation and its corresponding magnetization dynamics at $E < 0$, $E = 0$, and $E > 0$, respectively, where E is the out-of-plane electric field pulse. Θ represents the thermal perturbation.

3. Implementation of an In-Memory p-Bit. To elucidate the in-memory p-bit implementation, we examine the stochastic magnetization dynamics in the gated vdW heterostructure by using the stochastic Landau–Lifshitz-Gilbert–Slonczewski (s-LLGS) equation,

$$\frac{\mathrm{d}\boldsymbol{m}(t)}{\mathrm{d}t} = -\boldsymbol{m}(t) \times \boldsymbol{\Theta}(t) + \boldsymbol{\tau}_{\mathrm{Rashba}} + \boldsymbol{\tau}_{\mathrm{Ising}}, \tag{2}$$

where $\boldsymbol{m}(t)$ is the time-dependent unit magnetization vector of the FM layer, and $\boldsymbol{\Theta}(t)$ represents thermal perturbations. The in-plane torque $\boldsymbol{\tau}_{\mathrm{Rashba}}$ and out-of-plane torque $\boldsymbol{\tau}_{\mathrm{Ising}}$ are induced by Rashba and Ising SOC, respectively, in response to an applied current. The input-output characteristics are shown in Fig. 2(a), based on simulations of the FM layer's magnetization evolution. In the first step (left panel), an electric current pulse generates the Rashba torque $\boldsymbol{\tau}_{\mathrm{Rashba}}$, causing the magnetization to precess around the y-axis and deviate from the UP state (see inset). In the second step (right panel), the magnetization is stabilized under an electric field, settling into either the UP or DOWN state, corresponding to 0 and 1, respectively. The probabilities P_0 and P_1 are controlled by the electric field pulse E_i. When $E_i = 0$, the probabilities are equal ($P_0 = P_1 = 0.5$). A large positive field (i.e., $+0.2\,\mathrm{V/nm}$) pins the output m_i to 1 ($P_0 = 0$, $P_1 = 1$), while a large negative field (i.e., $-0.2\,\mathrm{V/nm}$) pins it to 0 ($P_0 = 1$, $P_1 = 0$). The output state for the ith p-bit can be expressed as a function of the input electric field, in a manner similar to the ideal binary stochastic neuron, which exhibits an input-output relation,

$$m_i = \theta\left[\sigma(E_i) - r\right], \tag{3}$$

where θ is the unit step function, σ is the sigmoidal function, and r is a random number uniformly distributed between 0 and 1. The average output state as a function of E_i is shown in Fig. 2(b), with each data point representing an average over 1000 pulse cycles. Figure 2(c) shows cycle-varying outputs for a specific input field. We find that stochastic switching behavior can be observed near $E_i = 0\,\mathrm{V/nm}$, while the stochastic behavior can be transformed into the deterministic behavior as E_i increases to approximately $\pm 0.1\,\mathrm{V/nm}$.

These p-bits can be interconnected to perform useful functions. The ith p-bit is driven by a synaptic input E_i (i.e., an electric field pulse), which depends on the outputs $\{m_1, \ldots, m_N\}$. This setup is inspired by the concept of Boltzmann machines pioneered by Hinton and colleagues [21] for machine learning applications, where the synaptic input E_i is derived from the energy function $\mathcal{E}$ via the following relation,

$$E_i = -\frac{\partial \mathcal{E}(m_1, \ldots, m_N)}{\partial m_i}. \tag{4}$$

These networks explore configurations with probabilities given by the Boltzmann distribution $P(m_1, \ldots, m_N)$, which are proportional to $\exp[-\mathcal{E}(m_1, \ldots, m_N)]$. As such, configurations with the lowest energy have the highest probability, making the network well-suited for optimization problems, where the correct solution minimizes a cost function $\mathcal{E}$, which is used to calculate the synaptic inputs E_i.

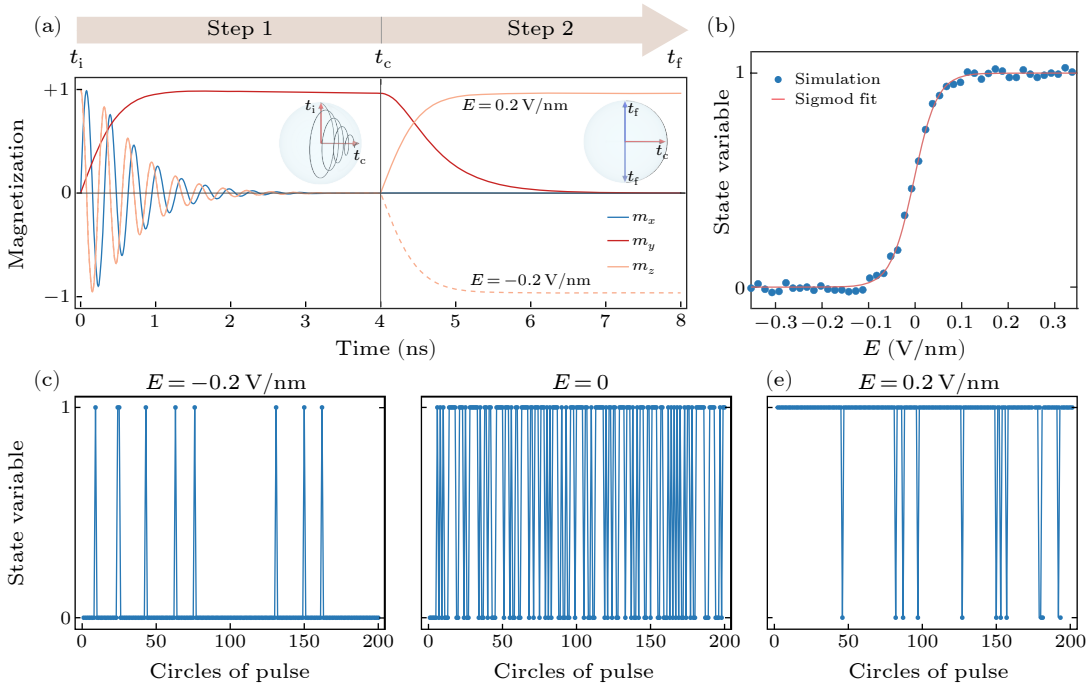

Fig. 2. (a) The magnetization dynamics are driven by the combined effects of spin-orbit torque. (b) The cycle-averaged state variable, as a function of the applied input electric field, is fitted to a sigmoidal function. Each point is averaged over 1000 cycles of pulses, with 5000 or more sampling points for each data point shown. (c)–(e) Cycle snapshots of the state variable for three different input electric field pulses, showing the preferred state of an in-memory p-bit (high or low) as a function of the input electric field.

4. Benchmarking of In-Memory p-Bits with the MAXCUT Problem. We then proceed to benchmark our proposed computing scheme with the MAXCUT problem,[46] which is a classic and well-known nondeterministic polynomial time hard (NP-hard) optimization task that partitions the nodes of an undirected graph to maximize the number of edges between the two subsets. It is pivotal in statistical mechanics and quantum computing, serving as a benchmark for evaluating the performance of classical and quantum algorithms in modeling complex systems and optimization tasks.[47–49] Moreover, our in-memory probabilistic computing has emerged as a unified framework for modeling and solving a wide variety of combinatorial optimization problems.[45] The MAXCUT problem can be defined as follows. Let $G(N, P)$ be a weighted undirected graph with n nodes in N and edges in P. This problem consists of finding a partition $N = N_0 \cup N_1$ with $N_0 \cap N_1 = \emptyset$ that maximizes the number of edges $(i, j) \in P$ connecting the two subsets of nodes, namely $i \in N_0$ and $j \in N_1$. This problem can be equivalently formulated as the task of finding the global minimum energy state of the Ising energy function:

$$\mathcal{E} = -\sum_{i,j} w_{ij} s_i s_j, \tag{5}$$

where w_{ij} are the edge weights, $s_i \equiv 2m_i - 1$ is the discrete variable of the system referred to as the spin state, which can take on the values $+1$ or -1. The MAXCUT problem can then be restated as finding the n-bit number s that maximizes the payoff, which is a function of the cut defined by s and is expressed as

$$P(s) = \frac{1}{2}\sum_{i,j}(1 - s_i s_j) w_{ij}. \tag{6}$$

The smallest meaningful MAXCUT problem involves at least three nodes, as graphs with fewer nodes lack sufficient complexity. Here, we examine a four-node MAXCUT problem with edge weights of $+1$ and -1, as shown in Fig. 3(a). By setting $m_1 = 0$ (i.e., $s_1 = -1$), the problem reduces to three nodes. The goal is to partition the graph into two subsets, $N_0 = \{\text{A, C}\}$ and $N_1 = \{\text{B, D}\}$, such that the total edge weight sums to 2. The payoff function for these weights is $P(s) = \{-1, 0, 1, 2\}$, where $s = \{000, 001, 010, 011, 100, 101, 110, 111\}$. The global maximum occurs at $s = 101$, so the probabilistic computer output is $\{m_2, m_3, m_4\} = \{1, 0, 1\}$, as illustrated in Fig. 3(c). To maximize $P(s)$, we construct a network of binary stochastic neurons driven by inputs E_i, calculated from Eq. (4), where m_i is the output of the i-th neuron. This approach is conceptually similar to adiabatic quantum computing (AQC),[50] with substantial effort invested in identifying suitable payoff functions for optimization problems, many of which can be adapted for p-bit networks. The corresponding function for each graph cut is encoded in the synaptic input E_i, as detailed in the Supplementary Material.[45]

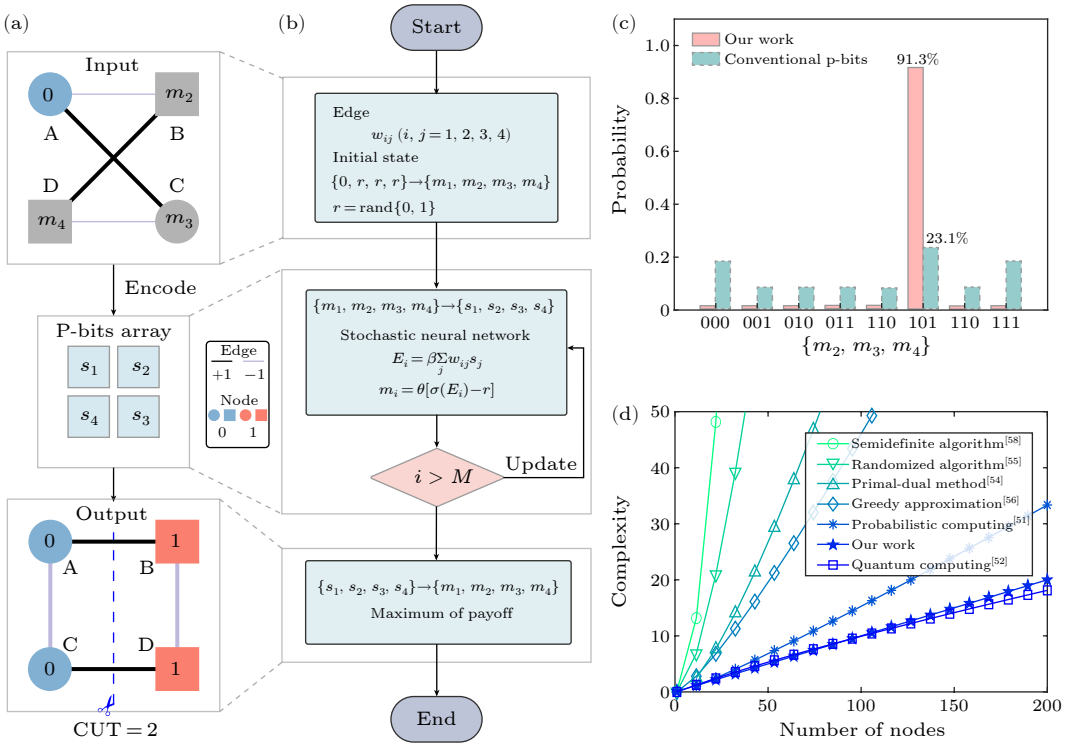

Fig. 3. (a) Illustration of a graph consisting of four nodes and four edges. The edges are assigned weights with values of either $+1$ or -1. When m_1 is fixed at 0 ($s_1 = -1$), the solution is $s = 101$, and the MAXCUT corresponds to the drawn cut. (b) Flowchart detailing the solution for the four-node MAXCUT problem. (c) The output state of the system when four in-memory p-bits are used to cut four interconnecting nodes with the first one fixed to 0. Here, the number of iterations for both is 10. (d) Computational complexity estimation for solving the MAXCUT problem using various algorithms and our design.

The methodology for solving the MAXCUT problem is depicted in Fig. 3(b). Starting from a randomly initialized state, the system is iteratively updated according to Eqs. (3) and (4), and the state flips are determined based on interconnection strengths. The synaptic input is given by $E_i = \beta \sum_j w_{ij} s_j$, where β is the inverse temperature, controlling the iteration step size in the annealing process. The system discretizes the range into steps, with each iteration result stored and used as the initial state for the next, continuing until a predefined number of iterations, M, is reached. Annealing occurs within an optimal range of β values, leveraging the electric field controllability of in-memory p-bits while maintaining dominant randomness as E_i approaches zero. This ensures convergence to the ground state, yielding the optimal MAXCUT solution.

To compare the performance of different computational approaches for solving the MAXCUT problem in Fig. 3(a), we set $M = 10$ and analyzed the results from two schemes. Our proposed scheme achieves an accuracy of 91.3%, significantly outperforming the conventional probabilistic computing approach, which reaches only 23.1%. Compared to conventional probabilistic computing approach, our approach demonstrates a substantially higher accuracy. Increasing the number of iterations could improve the convergence, but would also increase the computation time. To benchmark the time complexity, we fix M and plot the time complexity as a function of node count [Fig. 3(d); see Supplementary Material [45] for details]. Our approach exhibits a near-linear computational complexity, making the computation speed approximately five times faster than the conventional probabilistic computing, [51] with the advantage further magnified with the increasing graph size. For graphs with fewer than 50 nodes, our model showed a slight edge over quantum computing. [52,53] For larger node counts, our p-bit-based scheme maintains performance comparable to quantum computing while significantly outperforming both the classical algorithms [54–58] and the conventional probabilistic computing.

Our proposed scheme is experimentally feasible, with previously reported material systems and mature microfabrication techniques. As discussed, our theoretical framework builds upon the observation of layer pseudospins in materials such as graphene and TMDs. [29–31,37,59] Recent experiments have demonstrated electrical and magnetic control of layer pseudospins in vdW heterostructures via spin-filtered interlayer charge transfer, [60] gate-tunable exchange bias engineering, [61] and twist-angle-modulated spin-momentum locking. [62] These advances establish viable pathways for implementing programmable spin textures and quantum state manipulation using standard heterostructure fabrication techniques, directly supporting the proposed pseudospin-based probabilistic computing framework. In bilayer TMDs/FM heterostructures, p-bits based on layertronics can be controlled with high precision via electrically tunable spin-orbit torques, [63–66] and the readout is easily accessible. [67–69] Unlike conventional probabilistic computing, which is typically constrained by local minima, our approach demonstrates higher accuracy and significantly reduced time complexity. In contrast to quantum computing requiring ultra-low operating temperatures, [70] our proposed computing scheme can be implemented at room temperature and can effectively address complex optimization problems, offering similar reductions in time complexity. These advantages indicate that the proposed in-memory probabilistic computing approach is not only experimentally feasible but also exhibits advantage over previously reported computing technologies. Furthermore, the scalability of the system is supported by the large-area growth of TMDs and ferromagnetic van der Waals materials, combined with mature microfabrication technologies that are compatible with CMOS processes, enabling large-scale integration. [71–78] By combining quantum coherence with the scalability of classical systems, and compatibility with established microfabrication technologies, our scheme represents a promising direction for next-generation computational technologies, bridging the classical and quantum computing paradigms.

5. Conclusions. In this work, we present an in-memory probabilistic computing paradigm based on layer pseudospins, utilizing their electronic control in van der Waals heterostructures. This approach enables parallel, asynchronous p-bit operation, improving computational efficiency and enhancing the probability of storing optimal solutions. Our proposed computing scheme demonstrates near-linear time complexity and allows for a five-fold efficiency improvement over conventional probabilistic computing, while maintaining performance comparable to quantum computing for larger node counts. The findings of this work underscore the transformative potential of layertronics in quantum electronics, highlighting the pivotal role of layer pseudospins in advancing in-memory probabilistic computing.

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