h-BN-assisted Metal Contact Transfer to InSe for Two-Dimensional Multifunctional Electronic Devices

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Metal contacts to two-dimensional (2D) semiconductors are crucial for determining the electrical performance of electronic devices. However, traditional three-dimensional metal deposition processes cause damage to 2D semiconductors and considerable Fermi-level-pinning effects. In this study, a hexagonal boron nitride (h-BN)-assisted transfer method was proposed for transferring metal contacts to few-layered InSe for fabricating 2D functional electronic devices. Using the transferred Pt electrodes as the contact, p-type dominated ambipolar conduction behavior with the hole Schottky barrier height (SBH) approaching 0 meV was observed in field-effect transistors (FETs) comprising multilayered InSe. Based on this phenomenon, several InSe homojunctions were fabricated using a dual-gate modulating method such as p–p, n–n, p–n, and n–p. For InSe p–n homojunctions, a current rectification ratio of over 10^4 and optoelectronic detection capabilities were achieved. Furthermore, a complementary metal–oxide–semiconductor (CMOS) inverter with an ultra-high voltage gain exceeding 60 at $V_{\rm DD} = -1$ V was fabricated. The proposed h-BN-assisted metal contact transfer method can be easily extended to other 2D semiconductors for fabricating complementary electronic and optoelectronic devices.

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Introduction. Traditional Si transistors are continuously scaled down to enhance their performance and lower the associated cost. However, minimized channel length causes a series of issues such as high off-state current and static power consumption, which limit the further development of Si transistors.[1–4] Two-dimensional (2D) semiconductor materials are atomically thin and do not have dangling bonds, thereby enabling the effective electrostatic control of the channel by the gate. They also prevent short-channel effects and are a potential route to continue Moore's law.[5,6] In the past decade, 2D semiconductor materials such as black phosphorus and 2D transition metal dichalcogenides have garnered considerable attention owing to their outstanding performance in multifunctional electronic devices.[7] Their high conductivity and excellent carrier mobility make them suitable for applications such as logic gates,[8] detectors,[9] and memory devices.[10] Their appropriate bandgaps and optoelectronic properties are also promising for energy conversion and storage devices such as batteries.[11]

InSe, a typical 2D metal chalcogenide semiconductor, has a relatively low electron mass ($m^* = 0.143\,m_0$) and layer-tunable moderate bandgaps; thus, its transistors exhibited high electron mobility that exceeded 1000 $\rm cm^2/Vs$ and a high on/off ratio at room temperature.[12–15] Due to the atomically sharp interface formed between InSe and h-BN, ultrafast non-volatile memory devices based on InSe/h-BN/graphite van der Waals (vdWs) heterostructures can be grown on SiO_2/Si substrates.[16,17] By inducing phase transition via Y doping in the contact region, a room-temperature ballistic ratio of up to 83% and a high transconductance of 6 $\rm mS{\cdot}\mu m^{-1}$ can be achieved for ballistic transistors.[18] Furthermore, its layer-dependent and moderate direct bandgap endows it with excellent optoelectronic properties.[19–22] However, due to the strong Fermi-level-pinning effect at the metal–semiconductor contact interface, InSe field-effect transistors (FETs) typically exhibit n-type conduction with electrons as the majority carriers;[23–25] this limits their application in complementary electronic devices. Kis *et al.* observed n-type dominated ambipolar transport behavior in InSe with graphite contacts.[26] The Se vacancy in InSe can generate a peak in the density of states near the valance band, thereby enabling access to the hole conduction branch. Several strategies have been proposed to overcome the Fermi-level-pinning effect, including using 1D edge contact[27] or metallic 2D materials as the contact.[28] Metal electrode transfer has garnered considerable attention as a nondestructive method for modulating the Schottky barrier height.[29–32] By pre-depositing metal electrodes on a

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sacrificial substrate and then transferring them onto the target 2D material using the dry transfer method, vdWs contacts can be formed.[30] These contacts can avoid damage to the 2D material by high-energy particles in traditional metal evaporation, thereby enabling the modulation of the type of carrier in FETs by selecting metals with different work functions.

In this study, an h-BN-assisted metal contact transfer method was proposed for constructing multifunctional electronic devices. Using transferred Pt electrodes as the metal contact for few-layered InSe, p-type dominated ambipolar conduction behavior was observed in InSe FETs. The on/off current ratio for hole conduction reached $\sim 10^9$ with a hole mobility of $\sim 11.64\,\mathrm{cm}^2/\mathrm{Vs}$ and a near-ideal subthreshold swing as low as 72.68 mV/dec was achieved. By determining the temperature-dependent transfer characteristics of InSe FETs, a hole Schottky barrier height (SBH) of ~ 0 meV was obtained. By accessing the hole conduction regime of the InSe channel, multiple types of homojunctions were created, including p–p, n–n, p–n, and n–p, using a dual-gate modulation method. The InSe p-n homojunction exhibited a current rectification ratio of over 10^4 with an ideality factor of ~ 3.02 and optoelectronic detection capabilities. Moreover, a complementary metal-oxide-semiconductor (CMOS) inverter with the voltage gain of over 60 at $V_{\mathrm{DD}} = -1\,\mathrm{V}$ was constructed. These results demonstrated that the h-BN-assisted metal contact transfer method could be used for fabricating metal contact electrodes of 2D semiconductor materials for developing multifunctional CMOS electronic and optoelectronic devices.

Results and Discussion. Figure 1(a) shows the fabrication process of h-BN-assisted transferred metal contact. A 2D h-BN sheet was first mechanically exfoliated onto a sacrificial substrate (heavily doped p-silicon wafer) (I). Using electron beam lithography (EBL) and reactive ion etching (RIE), patterns were predefined and etched on the h-BN sheet for developing contact electrode areas (Ⅱ). Then, metal electrodes were deposited via electron beam deposition (EBD), ensuring that they were tightly connected to the h-BN layer (Ⅲ). After functionalizing the wafer with hexamethyldisilazane (HMDS) vapor, a layer of polymethyl methacrylate (PMMA) was spin-coated on the h-BN layer (Ⅳ). Using a polydimethylsiloxane (PDMS) sheet, the h-BN and metal electrodes were picked up from the Si sacrificial substrate and then aligned and transferred to the target material using a dry transfer method (Ⅴ and Ⅵ). The PDMS sheet was heated to separate it from the PMMA layer (Ⅶ). The top PMMA layer was then removed using acetone (Ⅷ). Finally, EBL and EBD were used again to define and deposit the other parts of the contact electrodes (Ⅸ). Figures 1(b), 1(c), and 1(d) show the optical images of the device after steps Ⅱ, Ⅵ, and Ⅶ, respectively.

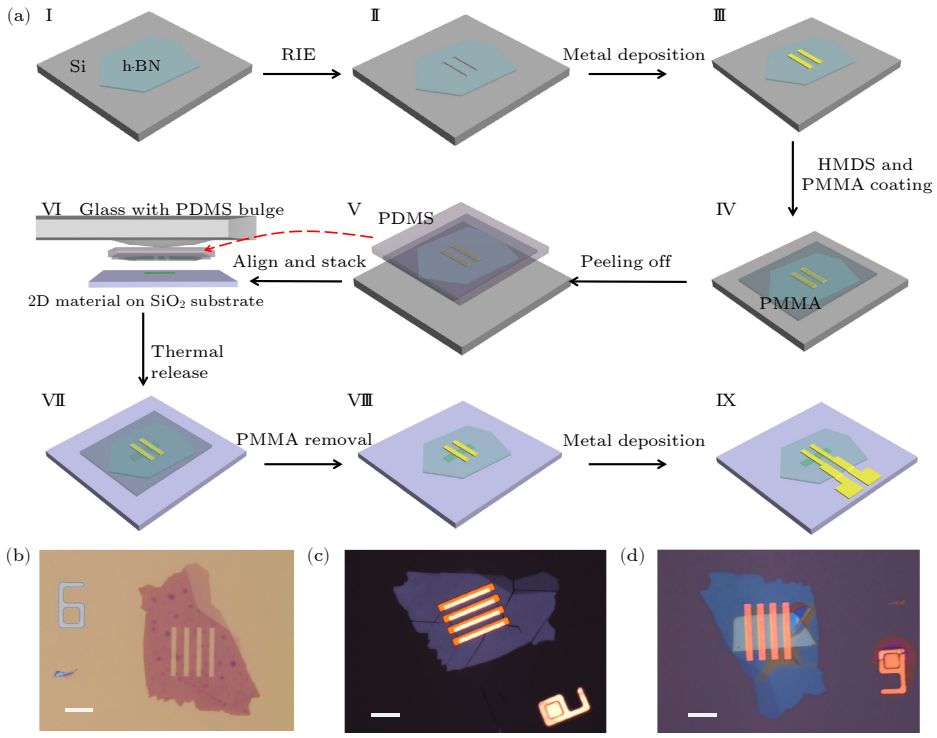


Fig. 1. Fabrication process of h-BN-assisted transferred metal contact. (a) Fabrication flow of h-BN-assisted transferred metal contact. I) Exfoliation of the h-BN layer on the silicon sacrificial substrate; Ⅱ) contact pattern fabrication via RIE; Ⅲ) metal deposition for contact area; Ⅳ) HMDS functionalization and PMMA coating; Ⅴ) PMMA peeling off from the sacrificial substrate using the PDMS flake; Ⅵ) aligning and stacking the electrode to the target material on the SiO_2 substrate; Ⅶ) separation of the PMMA layer from the PDMS layer via heating; Ⅷ) PMMA layer removal; Ⅸ) metal deposition for circuit area. (b) Optical image of the h-BN layer deposited on the silicon sacrificial substrate after RIE (step Ⅱ). (c) Optical image of the h-BN layer and contact metal on the PDMS flake after peeling off (step Ⅵ). (d) Optical image of the device after dry transfer (step Ⅶ). The scale bars in Figs. 1(b), 1(c), 1(d) are 10 μm.

Unlike the traditional method of directly depositing metal electrodes, transferred metal electrodes form vdWs contacts with the target material; thus, they prevent damages caused by high-energy deposition and are free from the shortcomings of Fermi-level-pinning effect.[30] The h-BN layer is vital because the metal electrodes are prepared separately on the sacrificial substrate and are tightly connected with it. The h-BN layer encapsulates the target material and effectively prevents the performance degradation of the target material caused by exposure to air during traditional metal deposition.[31–33] The h-BN layer serves as the encapsulation layer and ensures that the metal electrodes are fixed in place. This process prevents detachment due to the strong vdWs force with 2D materials and the silicon wafer. The h-BN layer also serves as the top-gate dielectric layer. Compared with the traditional electrode transfer method, the h-BN layer-assisted method improves the success rate of device fabrication and enables the removal of thick PMMA layers. It also reduces the risk of electrode detachment, making it more flexible for subsequent vertical processing such as 3D integration.

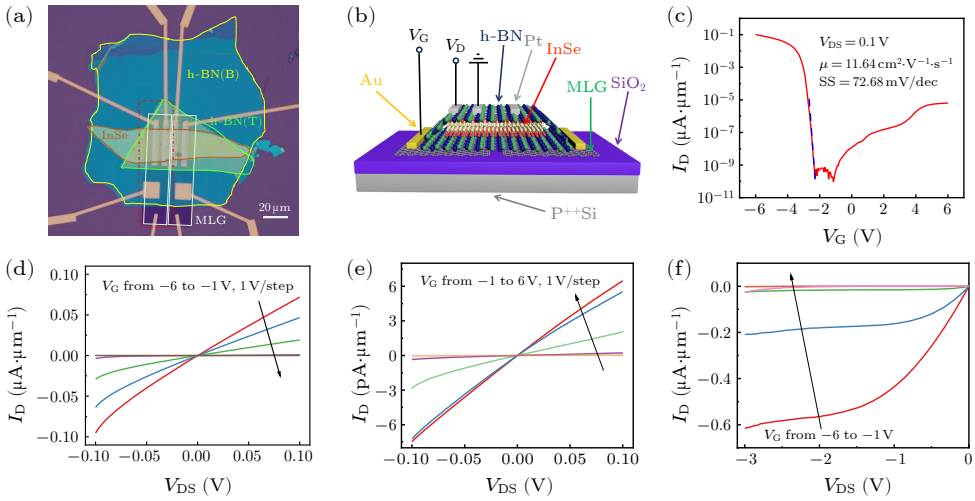


Fig. 2. Electrical characteristics of InSe FETs based on h-BN-assisted transferred Pt contact electrodes. (a, b) Optical image (a) and schematic (b) of transferred-Pt-contact InSe FET device. The channel is marked by the red dash box. (c) Transfer curve of the InSe FET at $V_{DS} = 0.1$ V, showing a p-type dominant ambipolar conduction behavior with a near ideal SS of ∼72.68 mV/dec. (d, e) Output curves of the InSe transistor under p-type (d) and n-type (e) conduction. (f) Saturation behavior at large V_{DS} from 0 to 3 V and negative V_G.

The feasibility of the proposed h-BN-assisted metal contact transfer method was tested by fabricating InSe FETs using h-BNassisted transferred Pt electrodes. The details of device fabrication are given in the Methods section. Figures 2(a) and 2(b) show the optical image and structural diagram of the transistor, respectively, in which multilayered graphite (MLG), h-BN (B), InSe, h-BN (T), and Pt serve as the gate electrode, back gate dielectric, channel material, top encapsulation layer, and contact electrodes, respectively. The thickness of h-BN (B), InSe, and h-BN (T) layers is shown in Fig. S1 in Supporting Information, where the channel region is marked by a red dashed box. Figure 2(c) shows the transfer curve of the transistor via back-gate sweeping from −6 to +6 V at $V_{DS} = 0.1$ V, indicating p-type dominated ambipolar conduction. The channel current (I_D) was well modulated by the bottom gate, with a high on/off current ratio of 10^9 and 10^5 for the hole and electron conduction branches, respectively. The carrier mobility was determined as follows:[14]

$$\mu = \frac{L}{W}\frac{1}{C_i}\frac{1}{V_{DS}}\frac{dI_D}{dV_G}, \tag{1}$$

where L, W, C_i, I_D, and V_G denote the channel length, channel width, gate dielectric capacitance, drain-source current, and gate voltage, respectively. The hole current reached 0.1 μA·μm^{-1} at $V_G = -6$ V, with a high hole mobility (μ) of 11.64 cm^2·V^{-1}·s^{-1}; this value is higher than that previously reported for 2D material p-type transistors.[34–36] The subthreshold swing (SS) was calculated as follows:

$$\mathrm{SS} = \frac{dV_G}{d(\log I_D)}. \tag{2}$$

Notably, the hole conduction branch showed a near ideal SS of 72.68 mV/dec, indicating good interface quality between the h-BN and InSe layers. Figures 2(d) and 2(e) show the output curves under hole conduction ($V_G = -6$ V to −1 V) and electron conduction ($V_G = -1$ V to 6 V). The I_D was linear and symmetric for both high positive or negative V_G at V_{DS} ranging from −0.1 V to +0.1 V. When V_{DS} increased to 1 V, the hole conduction branch output curve remained linear and the electron conduction branch was nonlinear. This indicated good p-type ohmic contact at $V_G = -6$ V and n-type Schottky contact at $V_G = 6$ V (Fig. S2, Supporting Information). As shown in Fig. 2(f), under high V_{DS} conditions, I_D exhibited stable saturation behavior. The contact resistance (R_C) was determined using the Y-function method at a low R_C of ∼22.9 kΩ·μm (Fig. S3, Supporting Information).

To further investigate the hole conduction characteristics of the transistor, temperature-dependent measure-

ment was performed on the transfer characteristics. Figure 3(a) shows the transfer curves of the InSe transistor at 100–300 K with a step of 50 K. As the negative gate voltage increased in the hole conduction branch region, the current exhibited a metal–insulator transition behavior; this suggested a negligible hole barrier. The effective SBH was determined based on the thermionic emission theory:[37,38]

$$I_{\mathrm{D}} = AA^{*}T^{1.5}\exp\left(-\frac{\mathrm{SBH}}{k_{\mathrm{B}}T}\right), \tag{3}$$

where A is the Schottky junction area, $A*$ is the Richardson constant, k_{B} is the Boltzmann constant, and T is the temperature. Figure 3(c) shows the extracted SBH values at different gate voltages. Under flat band voltage conditions, the extracted SBH was close to 0 meV. This indicated the good p-type ohmic contact characteristics of the InSe transistor fabricated using the transferred Pt contact electrodes.

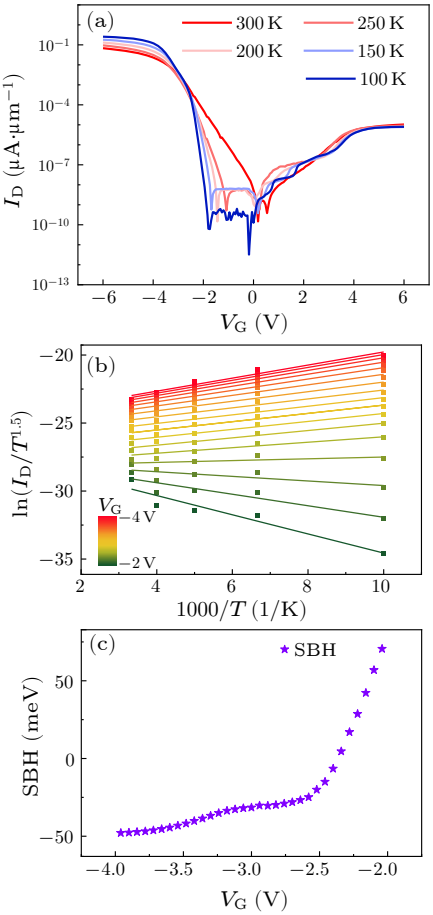


Fig. 3. Extraction of Schottky barrier height for the InSe FET comprising the transferred Pt contact electrode. (a) Temperature-dependent transfer curves from 100 to 300 K with a step of 50 K. (b) Arrhenius plots used to extract the Schottky barrier height at the p-type branch. (c) The extracted p-type Schottky barrier heights at various gate voltages.

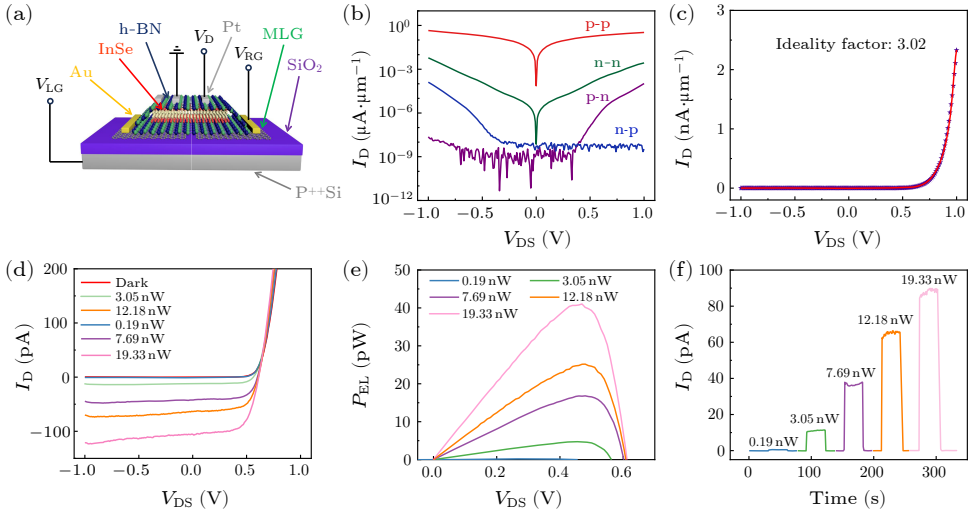
The transferred metal Pt electrodes with a high work function did not damage the 2D InSe channel, thereby forming a vdWs gap between the contact Pt electrode and the InSe channel. This also prevented Fermi-level pinning effect at the metal–semiconductor contact interface, which is observed in traditional high-energy deposition. For comparison, an InSe FET was fabricated using transferred Au contact electrodes (Fig. S4, Supporting Information). The band alignment between InSe and Pt and Au is shown in Fig. S4(d) in Supporting Information. The work function of the Pt electrode was close to the valence band of InSe, whereas that of the Au electrode was close to the midpoint of the bandgap. The transfer characteristic curves showed that the device with transferred Pt contact electrode exhibited a p-type dominated ambipolar conduction behavior, whereas that with the transferred Au contact electrode exhibited an n-type dominated ambipolar conduction behavior, consistent with the band alignment theory.

Based on the p-type dominated ambipolar conduction behavior in InSe FETs fabricated using the transferred Pt contact electrodes, multiple InSe homojunctions were fabricated [Fig. 4(a)]. By applying voltages to the bottom Si gate (V_{LG}) and the right graphite gate (V_{RG}), the carrier type in the InSe channel was modulated. When V_{LG} and V_{RG} were simultaneously applied, the carrier type in the left half of the InSe channel depended on the magnitude of V_{LG}. In contrast, the carrier type in the right half of the InSe channel was determined based on V_{RG} because of the electric field generated by V_{LG}. Figure 4(b) shows the output curves of the InSe homojunction under four gate voltages. When a negative bias was simultaneously applied to V_{LG} (−60 V) and V_{RG} (−6 V) (red line), the carrier type of the entire channel was modulated to be holes; this indicated the formation of a p–p junction and exhibited the highest and symmetric channel current under four conditions. In contrast, when a positive bias was applied to V_{LG} (60 V) and V_{RG} (6 V) (green line), the channel was dominated by electrons and formed an n–n junction. A symmetric channel current slightly lower than the p–p junction was formed because the contact region was more beneficial for hole injection. When V_{LG} and V_{RG} were applied with different polarity biases, the channel was modulated into a p–n (purple line) or n–p (blue line) junction. The output curve showed a clear rectification behavior and the rectification ratio exceeded 10^4 at V_{DS} ranging from −1 to 1 V. The channel current of the p–n junction [purple stars in Fig. 4(c)] was fitted with the Shockley equation [red curve in Fig. 4(c)]:[39,40]

$$I_{\mathrm{D}} = \frac{\eta V_{\mathrm{T}}}{R_{\mathrm{S}}} W\left[\frac{I_0 R_{\mathrm{S}}}{\eta V_{\mathrm{T}}}\exp\left(\frac{V_{\mathrm{DS}} + I_0 R_{\mathrm{S}}}{\eta V_{\mathrm{T}}}\right)\right] - I_0, \tag{4}$$

where η is the ideality factor; $V_{\mathrm{T}} = k_{\mathrm{B}}T/e$ is the thermal voltage; R_{s} is the equivalent resistance of the contact and doped region; and k_{B}, T, e, W, and I_0 are the Boltzmann constant, temperature, electron charge, Lambert W function, and reverse saturation current, respectively. The large ideality factor (∼3.02) obtained from the fitting curve indicated that the electron transport was mainly dominated by the recombination process that may be related to the traps and defects in the InSe channel that served as the recombination centers.[17] The photoelectric and photovoltaic characteristics of the p–n homojunction were

measured as the intrinsic properties. Figure 4(d) shows the channel current in the dark and under 633 nm laser irradiation with different laser powers. In the dark atmosphere, the channel current was suppressed when a negative voltage was applied on V_{DS}. Under laser irradiation, significant amounts of photocurrent were generated. The positive open-circuit voltage (V_{OC}) and negative short-circuit current (I_{SC}) indicated that the p–n junction effectively separated the generated charge carrier and produced a self-driven photocurrent related to the laser power. Figure 4(e) shows the relation between the output electrical power (P_{EL}) and V_{DS} under different laser power irradiations, where $P_{EL} = I_{SC} \times V_{OC}$. At V_{DS} of ∼0.48 V, P_{EL} reached its maximum value, which is the optimal working voltage for the device as a photovoltaic cell. Figure 4(f) shows the photocurrent under different laser power levels at $V_{DS} = 0$ V. The current switching behavior was observed even under the weakest laser irradiation (∼0.19 nW), indicating the potential for weak light detection. Figure 4(g) shows some typical parameters such as V_{OC}, I_{SC}, fill factor, electrical power conversion efficiency, and responsivity (fill factor $= P_{EL}^{max}/I_{sc} \times V_{OC}$, efficiency $= P_{EL}^{max}/P_{laser}$, and responsivity $= V_{OC}/P_{laser}$). The maximum electrical power conversion efficiency reached ∼0.22% at a power level of 7.69 nW, and the maximum photodetection responsivity reached 2.39×10^9 V/W at the weakest power level of 0.19 nW.



(g)

Laser power (nW)	0.19	3.05	7.69	12.18	19.33
V_{OC} (V)	0.45	0.56	0.6	0.6	0.61
I_{SC} (pA)	0.66	12.22	42.27	63.53	105.37
Fill factor	0.63	0.69	0.66	0.66	0.64
Efficiency (%)	0.10	0.16	0.22	0.21	0.21
Responsivity (10^9 V/W)	2.37	0.18	0.08	0.05	0.03

Fig. 4. InSe homojunctions based on h-BN-assisted transferred Pt contact electrode. (a) Schematic of the InSe homojunction. (b) Output curves of the InSe homojunctions with different V_{LG} and V_{RG} values, red ($V_{LG} = -60$ V, $V_{RG} = -6$ V), green ($V_{LG} = 60$ V, $V_{RG} = 6$ V), blue ($V_{LG} = -60$ V, $V_{RG} = 6$ V), and purple ($V_{LG} = 60$ V, $V_{RG} = -6$ V). (c) Linear plot of the output curve (purple stars) across the InSe p–n homojunction. The red curve is the fitting curve drawn using the modified Shockley equation. (d) I_D–V_{DS} curves of InSe p–n homojunction in the dark and under light illumination with different powers of a 633-nm laser. (e) Output electrical power (P_{EL}) as a function of V_{DS} with different laser powers. (f) Photocurrent of the InSe p–n homojunction under light illumination with different laser powers ($V_{DS} = 0$ V). (g) List of the key figures of merit characterizing the optoelectronic properties of the InSe p–n homojunction such as the open-circuit voltage (V_{OC}), short-circuit current (I_{SC}), fill factor, electrical power conversion efficiency (η_{EPCE}), and responsivity.

The high-performance p-type InSe FETs fabricated using the transferred Pt contact electrodes can be used in 2D logic circuits. Figures 5(a)–5(c) shows a digital p-type metal–oxide–semiconductor (PMOS) inverter based on the InSe FETs comprising the transferred Pt contact electrode. By connecting a fixed resistor in series with the transistor, the inverter function can be realized [Fig. 5(a)]. Supply voltage (V_{DD}) was applied on the resistor side, and the outer contact electrode of the FET was grounded. The input voltage (V_{In}) was applied on the gate of the FET, and the output voltage (V_{Out}) was measured between the FET and resistor. Figure 5(b) shows the relation between V_{Out} and V_{In} when $V_{DD} = -1$ V. When V_{In} was above −3 V, V_{Out} was close to V_{DD} (logic "1"). When V_{In} was below −4 V, V_{Out} was close to 0 V (logic "0"). The voltage gain of the inverter is an important parameter for characterizing the sensitivity of V_{Out} to the changes in V_{In}. Figure 5(c) shows the variation in the voltage gain with V_{In} at a V_{DD} of −1 V, with its peak value reaching 1.58. Using the directly deposited Cr/Au contacts, a high-performance n-type metal–oxide–semiconductor (NMOS) FET can be fabricated. By integrating PMOS and NMOS, a CMOS

inverter with lower power consumption and better switching characteristics can be fabricated. The optical image of the CMOS inverter is shown in Figure S5 (Supporting Information). Figure 5(d) schematizes the CMOS inverter fabricated using the same InSe flake. The resistor of the PMOS inverter was replaced by an n-type metal-oxide-semiconductor field-effect transisor (NMOSFET), and the V_{In} was applied on both gates of the two FETs simultaneously. The input and output characteristics of the inverter [Fig. 5(e)] exhibited a considerably higher voltage gain than that of the PMOS inverter, reaching up to 68.73 at $V_{DD} = -1$ V [Fig. 5(f)]. The ultra-high voltage gain indicated their potential use in digital logic applications.

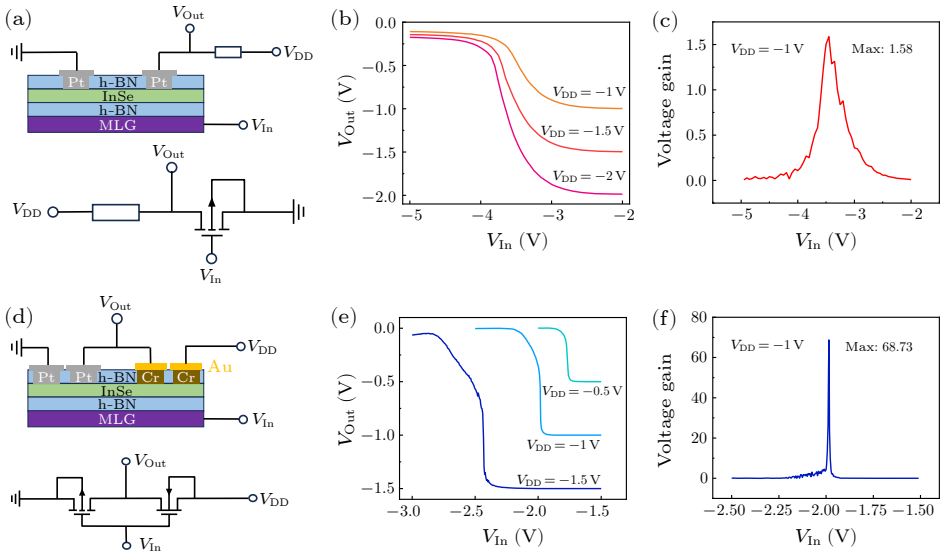


Fig. 5. PMOS and CMOS inverters based on the InSe transistor with transferred Pt contact electrodes and evaporated Cr/Au contact electrodes. (a) Schematic of the PMOS inverter. (b) V_{Out} as a function of V_{In} of the PMOS inverter at $V_{DD} = -1$ V. (c) Voltage gain of the PMOS inverter as a function of V_{In}. (d) Schematic of the CMOS inverter. (e) V_{Out} as a function of V_{In} of the CMOS inverter at $V_{DD} = -1$ V. (f) Voltage gain of the CMOS inverter as a function of V_{In}.

Conclusion. In conclusion, we developed an h-BN-assisted metal electrode transfer method for establishing a metal contact to few-layered InSe. Using this damage-free contact method and highworkfunction Pt as the contact electrode, a p-type dominant ambipolar conduction behavior was observed in InSe FETs with a high on/off current ratio up to 10^9, a hole mobility of $\sim$11.64 cm^2/Vs, and a near ideal SS of $\sim$72.68 mV/dec for the hole conduction regime. A Schottky barrier height of $\sim$0 meV for hole conduction was determined from the temperature-dependent transfer characteristics. To demonstrate the application of this contact method for multifunctional electronic devices, multiple homojunctions such as p–p, n–n, n–p, and p–n as well as InSe-based logic inverters were fabricated. The p–n homojunction exhibited a current rectification ratio over 10^4 and optoelectronic detection capabilities when the laser power was reduced to 0.19 nW. A CMOS inverter could be fabricated on an InSe flake, with an ultra-high gain of >60 under a V_{DD} of -1 V. The proposed method can be easily extended to other 2D materials, thereby providing a new approach for designing CMOS electronic and optoelectronic devices in the future.

Methods.

Device Fabrication and Electrical Characterization: InSe, graphite bulk crystals, and h-BN were purchased from 2D semiconductors, NGS Naturgraphit, and HQ graphene, respectively. First, MLG was exfoliated onto a silicon wafer containing 300 nm SiO_2 and patterned using EBL and RIE (O_2 100 sccm, 100 W, and 100 mTorr). Then, h-BN and InSe layers were sequentially exfoliated and dry transferred onto the MLG. Another h-BN layer was exfoliated onto a silicon wafer as the sacrificial substrate, and EBL was used to define the contact areas in the h-BN region. RIE (SF_6 30 sccm, O_2 10 sccm, 20 W, and 30 mTorr) was used to fully etch the h-BN layer in the contact areas. EBL and EBD were used to deposit Pt onto the contact areas, ensuring some overlap with the h-BN layer. The prepared electrodes were then placed in an HMDS vapor environment (120 °C and 25 min) and immediately coated with PMMA 950 A11 (4000 RPM). PDMS flake was bonded to the PMMA and quickly peeled off to separate the electrode from the sacrificial substrate. Then, the electrodes were aligned and laminated onto the prepared MLG/h-BN/InSe heterostructure. The device was heated to 50 °C, and PDMS was slowly lifted to separate PMMA from it. All processes involving the InSe heterostructure and electrode transfer were performed in an argon glovebox with O_2 and H_2O concentrations below 0.1 ppm to prevent InSe degradation. Finally, acetone was used to remove the PMMA film from the device surface, and EBL and EBD were performed to define and deposit the external circuit for measurements. Based on this device fabrication method, the contact areas were predefined and etched for directly evaporating Cr/Au electrodes on the h-

BN(T) layer to fabricate the CMOS inverter. In the final step, EBL and EBD were performed to define and deposit 5/50nm Cr/Au layer into directly evaporated contacts and the external circuit. Electrical measurements were conducted using a Keithley 4200 semiconductor characterization system (4200-SCS) and a Lakeshore probe station.

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