High-Performance Indium-Gallium-Zinc-Oxide Thin-Film Transistors with Stacked Al_2O_3/HfO_2 Dielectrics

Yue Li(李玥), Li Zhu(朱力), Chunsheng Chen(陈春生), Ying Zhu(祝影), Changjin Wan(万昌锦)*, and Qing Wan(万青)*

School of Electronic Science and Engineering, Nanjing University, Nanjing 210093, China

(Received 4 September 2022; accepted manuscript online 17 October 2022)

High-performance amorphous indium-gallium-zinc-oxide thin-film transistors (a-IGZO TFTs) gated by Al_2O_3/HfO_2 stacked dielectric films are investigated. The optimized TFTs with Al_2O_3 (2.0 nm)/HfO_2 (13 nm) stacked gate dielectrics demonstrate the best performance, including low total trap density N_t, low subthreshold swing voltage, large switching ratio $I_{ON/OFF}$, high mobility μ_{FE}, and low operating voltage, equal to $1.35 \times 10^{12}\,cm^{-2}$, 88 mV/dec, 5.24×10^8, 14.2 cm^2/V·s, and 2.0 V, respectively. Furthermore, a low-voltage-operated resistor-loaded inverter has been fabricated based on such an a-IGZO TFT, showing ideal full swing characteristics and high gain of ∼27 at 3.0 V. These results indicate a-IGZO TFTs gated by optimized Al_2O_3/HfO_2 stacked dielectrics are of great interests for low-power, high performance, and large-area display and emerging electronics.

DOI: 10.1088/0256-307X/39/11/118501

Recently, applications of amorphous indium gallium zinc oxide thin-film transistors (a-IGZO TFTs) in large-area display, emerging electronics and neuromorphic devices have attracted a great deal of attention, because of their superior electronical and physical properties, including high carrier mobility (> 10 cm^2/V·s), high transparency, and good uniformity.[1–6] However, a-IGZO TFTs with traditional silicon dioxide gate dielectric exhibit a high operation voltage. In this case, TFTs gated by high-κ dielectrics (such as HfO_2, ZrO_2, Al_2O_3) are featured with lower operating voltage as well as better performance, in comparison to SiO_2 or Si_3N_4 gate dielectric.[7–9]

Among these high-κ materials, HfO_2 has been widely investigated, due to its high dielectric constant and high transmittance. However, the large leakage current and small energy band gap make the practical use of HfO_2 suffer some critical issues, such as mobility reduction and device instability.[10–12] Hence, gate dielectric with stacked structure is adopted to make up the drawbacks existing in each of the stacked materials.[12–14] For instance, although dielectric constant of Al_2O_3 is moderate, it exhibits low leakage current and good stability.[15–18] Therefore, a-IGZO TFTs gated by Al_2O_3/HfO_2 may exhibit low operating voltage as well as low leakage current.

In this work, we investigate a-IGZO TFTs gated by different combinations of Al_2O_3/HfO_2. The optimal a-IGZO TFTs with Al_2O_3 (2.0 nm)/HfO_2 (13 nm) stacked dielectric show the best performance with a low subthreshold swing voltage (SS) of 88 mV/dec, a large $I_{ON/OFF}$ of 5.24×10^8, and a high mobility of 14.2 cm^2/V·s. Furthermore, small ΔV_{TH} of +0.25 V is obtained under a positive bias stress (PBS) at 2.0 V for 1000 s. Finally, a resistor-loaded inverter with a voltage gain of 27 at 3.0 V and an ideal swing characteristics was demonstrated.

Typical bottom-gate-type IGZO TFTs were made in this work. Firstly, gate dielectric films with different stacked thicknesses were deposited on the glass with 100-nm-thick ITO at a temperature of 150 ℃. Then, through radio frequency (RF) sputtering, 30-nm IGZO semiconducting channel layers were deposited at room temperature, cavity pressure and plasma power were set to 0.3 Pa and 100 W, respectively. Finally, thermal evaporation was employed to deposited 100 nm Al metal source and drain electrodes with help of a shadow mask, the channel width W and length L are 1000 μm and 100 μm, respectively. Figure 1(a) shows the schematic of the finished device. Finally, five types of TFTs with five kinds of gate dielectrics were fabricated, including HfO_2 (15 nm), Al_2O_3 (1.0 nm)/HfO_2 (14 nm), Al_2O_3 (2.0 nm)/HfO_2 (13 nm), Al_2O_3 (3.0 nm)/HfO_2 (12 nm), and Al_2O_3 (4.0 nm)/HfO_2 (11 nm), simplified as H, HA1, HA2, HA3 and HA4, respectively. The dielectric properties of TFTs were analyzed by using a semiconductor analyzer (Keithley 2636B) and an impedance analyzer (HIOKI IM 3533–01 LCR meter), and the electrical characteristics were analyzed by the semiconductor parameter analyzer at room temperature.

Figure 1(b) shows the surface roughness of five kinds of TFTs. The root-mean-square (RMS) roughness are 999, 796, 646, 594, and 615 pm, respectively. With the increase of alumina thickness, the surface roughness tends to be stable. Smooth surface can lead to fewer interface defects, making the interface contact between IGZO and electrolyte better.[19,20]

In order to measure leakage current density of thin films, Al/dielectric/ITO sandwich capacitors were prepared. It can be seen from Fig. 2(a) that the leakage cur-

*Corresponding authors. Email: wanqing@nju.edu.cn; cjwan@nju.edu.cn
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rent density of device HA2 is greatly reduced in comparison with device H. The reason for the high leakage current density of device H is the low band gap energy and relatively rough surface of HfO_2.[10–12] Al_2O_3 has better insulation which is attributed to its larger energy band gap.[15–17] Figure 2(b) illustrates the areal capacitance of the gate dielectric which is another important parameter of the transistor. According to the measured areal capacitance of the thin film, we find that the areal capacitance decreases with the increasing thickness of Al_2O_3, because the dielectric constant of Al_2O_3 is smaller than that of HfO_2.[21,22]

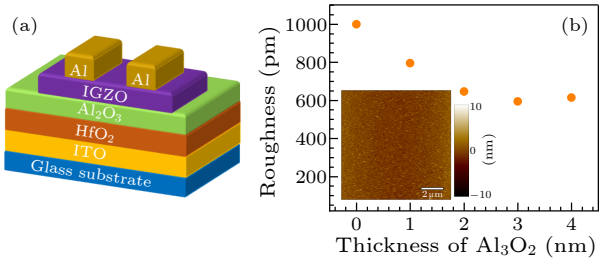

Fig. 1. (a) The schematic diagram of IGZO-based transistors with a structure of Al/IGZO/Al_2O_3/HfO_2/ITO/glass. (b) RMS roughness of different gate dielectrics.

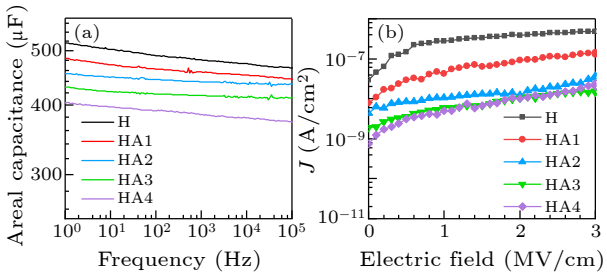

Fig. 2. (a) Areal capacitance of different gate dielectrics. (b) Leakage current density of different gate dielectrics.

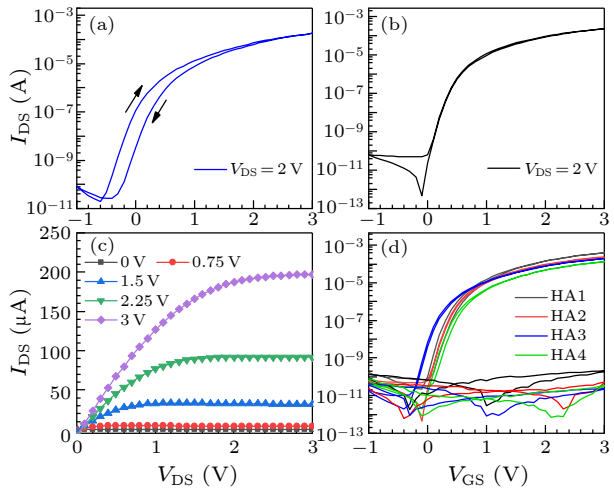

Fig. 3. (a) Transfer curve of device H. (b) Transfer curve of device HA2. (c) Output curve of device HA2. (d) Transfer characteristics of TFTs with different gate dielectrics.

The transfer characteristics of the TFTs with 15 nm HfO_2 measured at V_{DS} = 2.0 V are shown in Fig. 3(a). Moreover, it can also be observed that a large clockwise hysteresis window is 0.26 V, which can be interpreted as the charge traps at the interface between IGZO layer and gate dielectric.[23] In the process of gate voltage (V_{GS}) scanning, the charge traps at the dielectric/channel interface continuously capture charge and make contribution to the localized state charge, which leads to reduction of the density of free charge in the channel layer. Hence, with V_{GS} sweeping back from 3.0 V to −1.0 V, the reduction of I_{DS} leads to the clockwise hysteresis.

Figure 3(b) shows the transfer characteristic curve of the device HA2, almost no hysteresis can be seen, which can be attributed to few charge traps at the Al_2O_3/IGZO interface.[23] The output characteristic curve of device HA2 is shown in Fig. 3(c). V_{DS} is swept from 0 to 3.0 V and a saturation current of 200 μA is obtained. Figure 3(d) shows the transfer characteristic curves of other three samples with no obvious hysteresis. Then the following formula can be used to calculate the SS and saturation mobility:

$$\mathrm{SS} = \left(\frac{d\log(I_D)}{dV_{GS}}\right)^{-1},$$
$$I_{DS} = \left(\frac{W}{2L}C_i\mu\right)(V_{GS} - V_{TH})^2.$$

The trap density N_t affects the value of SS. A small trap density can increase the output current of the transistor, and improve the carrier mobility and switching ratio. N_t can be calculated by

$$N_t = \left[\frac{\mathrm{SS}\log e}{kT/q} - 1\right]\frac{C_i}{q}.$$

According to the above formula, the key electrical properties can be calculated. The electrical performance parameters of five samples are compared. In Fig. 4(a), the $I_{ON/OFF}$ of device HA2 is 5.24×10^8, much larger than that of device H (8.99×10^6), which can be attributed to the high leakage current of HfO_2.

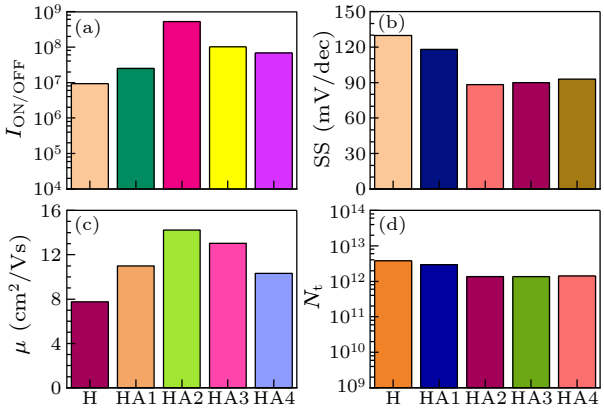

Fig. 4. (a) $I_{ON/OFF}$ of TFTs with different gate dielectrics, (b) SS of TFTs with different gate dielectrics, (c) μ_{FE} of TFTs with different gate dielectrics, (d) N_t of TFTs with different gate dielectrics.

Figure 4(b) shows that the SS of device HA2 is 88 mV/dec, which is the lowest SS among five samples, while the SS of device H is 129 mV/dec. Such a small SS is an important feature for switching TFT. As shown in Fig. 4(c), device HA2 has demonstrated the highest mobility of 14.2 $cm^2/V{\cdot}s$, which is larger than that of device H (7.76 $cm^2/V{\cdot}s$). Moreover, in Fig. 4(d), the N_t value of device HA2 is as low as 1.35×10^{12} cm^{-2}, the improvement of device HA2 is due to the relatively low leakage current of stacked film and the low interface trap density between IGZO and gate dielectric. These results prove that the Al_2O_3/HfO_2 stacked film can reduce the N_t and improve the electrical performance of the TFTs.

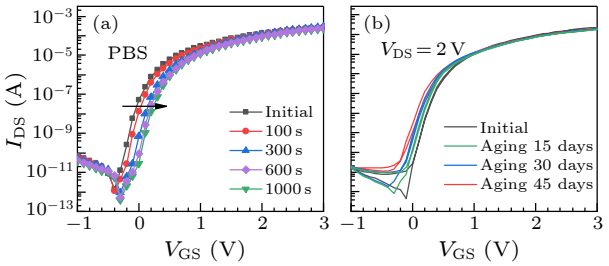

Fig. 5. (a) Transfer curves of device HA2 under PBS test. (b) Transfer characteristics of the device HA2 aging for 45 days in air.

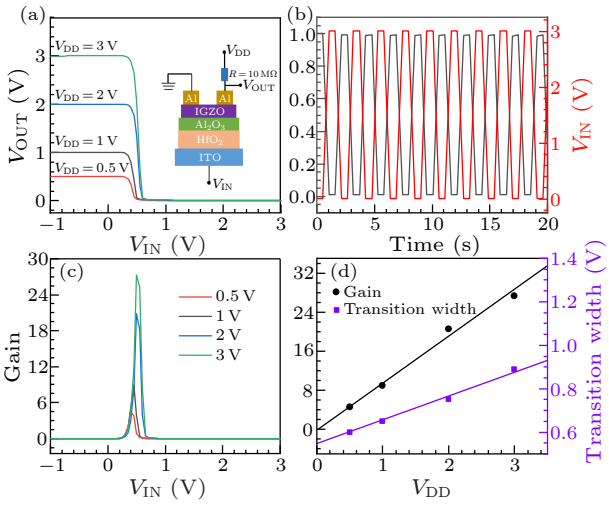

Fig. 6. (a) Voltage transfer characteristics curves (VTCs). (b) Dynamic switching behavior of the inverter under ac square waves at 0.5 Hz. (c) Voltage gain curves at different supplied voltages (V_{DD}). (d) Linear relationship between voltage gains and transition width with V_{DD}.

Furthermore, to investigate the stability of the device HA2. Figure 5(a) shows the transfer curve of TFTs under PBS stress. Here, +0.25 V shift can be observed under PBS of 2 V for 1000 s. The instability of TFTs is explained to charge trapping at the gate dielectric/channel interface.[24,25] In Fig. 5(b), transfer curve still exhibits relatively nice performance after 45 days of aging in air, further characterizing the stability of TFTs. To observe the performance of device HA2 in the circuit, we fabricated an inverter based on the TFT. Stable work of inverter can ensure the realization of the function of the complex circuit, due to fact that the inverter is the basic device constituting most of the integrated logic circuits.

Figure 6(a) shows the static voltage transfer characteristics curves (VTCs) under different V_{DD} and the structure diagram of the inverter which is composed of 10 MΩ resistor and TFT in series. The working mechanism of the inverter is such that, when the input voltage is less than the opening voltage of the TFT, the TFT is in the "OFF" state and a high V_{OUT} is obtained. However, when the input voltage is higher than the opening voltage of the TFT, the TFT can be switched on. Figure 6(b) demonstrates the good dynamic response of inverter. Figure 6(c) shows that voltage gain increases with the increase of V_{DD}. The gain can be characterized with $-\partial V_{OUT}/\partial V_{IN}$. When V_{DD} is 3.0 V, the gain of 27 is obtained. In comparison with previously reported inverters based on CMOS, a higher voltage gain under the condition of lower V_{DD} is achieved in our work.[26,27] As shown in Fig. 6(d), with the increase of V_{DD}, the voltage gains and transition width of the inverter increases linearly.

In summary, Al_2O_3 (2.0 nm)/HfO_2 (13 nm) stacked gate dielectric films can improve the performance of IGZO-based TFTs. Such IGZO-based TFTs exhibit a very good performance, including low SS of 88 mV/dec, large $I_{ON/OFF}$ of 5.24×10^8, and high mobility of 14.2 $cm^2/V{\cdot}s$. Their high stability is proved by PBS and aging test. Furthermore, an inverter with load resistance is constructed, exhibiting good swing voltage characteristics and a high gain of ∼27 when the applied V_{DD} is 3.0 V.

Acknowledgments. This work was supported by the National Key Research and Development Program of China (Grant Nos. 2019YFB2205400 and 2021YFA1200051), and the National Natural Science Foundation of China (Grant No. 62074075).

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