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Bufferless Epitaxial Growth of GaAs on Step-Free Ge (001) Mesa

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GaAs/Ge heterostructures have been employed in various semiconductor devices such as solar cells, high-performance CMOS transistors, and Ⅲ–V/Ⅳ heterogeneous optoelectronic devices. The performance of these devices is directly dependent on the material quality of the GaAs/Ge heterostructure, while the material quality of the epitaxial GaAs layer on the Ge is limited by issues such as the antiphase domain (APD), and stacking-fault pyramids (SFP). We investigate the epitaxial growth of high-quality GaAs on a Ge (001) mesa array, via molecular beam epitaxy. Following a systematic study of the Ge terrace via an *in situ* scanning tunneling microscope, an atomically step-free terrace on the Ge mesa measuring up to $5 \times 5\,\mu m^2$ is obtained, under optimized growth conditions. The step-free terrace has a single-phase c (4×2) surface reconstruction. The deposition of a high-quality GaAs layer with no APD and SFP is then achieved on this step-free Ge terrace. High-resolution transmission electron microscopy and electron channel contrast image characterizations reveal the defect-free growth of the GaAs layer on the step-free Ge mesa. Furthermore, InAs quantum dots on this GaAs/Ge mesa reveal photoluminescent intensity comparable to that achieved on a GaAs substrate, which further confirms the high quality of the GaAs layer on Ge.

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In recent decades, the direct epitaxial growth of Ⅲ–V optoelectronic materials on group Ⅳ platform (Si and Ge) for hybrid photonic integration has become a subject of significant research interest.[1] The evident optoelectronic properties of Ⅲ–V materials, arising from their direct-gap characteristics, makes them promising candidates for use in high-efficiency optical detectors and emitters.[2–5] GaAs/Ge heterostructures, in particular, show potential for applications in high-efficiency solar cells.[6] In addition, owing to the high degree of hole mobility in Ge, and the high electron mobility of GaAs, GaAs/Ge heterostructures with sharp interfaces could also be employed in high-performance complementary metal-oxide-semiconductor (CMOS) transistors, with Ge functioning as the p-MOS, and GaAs as n-MOS.[7] The material quality of GaAs/Ge heterostructures plays a significant role in the aforementioned device performance. Although the lattice mismatch between GaAs and Ge is negligible, the epitaxial growth of GaAs on Ge still faces two critical issues: interfacial defect-induced stacking fault pyramids (SFPs),[8] and antiphase domains (APDs), originating from an odd number of atomic steps at the interface, due to the polar difference between GaAs and Ge.[9] Previous efforts have focused on annihilating the APDs at the GaAs/Ge interface by means of the epitaxial growth of GaAs on offcut Ge (001),[10–12] or on a {113} faceted zigzag structure.[13] Alternatively, it is anticipated that APDs and SFPs can be completely avoided if the GaAs is grown on a step-free Ge (001) surface.

In this work, we report the defect-free growth of GaAs on step-free Ge mesa arrays via molecular beam epitaxy (MBE). We obtain an atomic step-free Ge (001) terrace of up to $5 \times 5\,\mu m^2$ on a pre-patterned Ge mesa structure, under specific conditions, including an appropriate growth temperature and low growth rate. A 20 nm GaAs nucleation layer, followed by a 100 nm GaAs layer, is deposited onto step-free Ge mesa arrays. No defects are observed in the GaAs layer, either by a high resolution transmission microscope (HRTEM) or electron channel contrast imaging (ECCI). In addition, an InAs quantum-dot layer is grown on the as-prepared GaAs/Ge platform. The photoluminescent (PL) measurements show a comparable intensity to that achieved on a GaAs substrate, which further confirms the high-quality growth

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of the GaAs layer on a step-free Ge platform. The defect-free GaAs/Ge heterostructure, with its atomically sharp interface, provides a unique platform for high-performance electronic and optoelectronic devices, and even for realizing topological transition in a GaAs/Ge quantum-well structure.[14]

Figure 1(a) shows a schematic of the fabrication process of the Ge mesa structure. A SiO_2 hard-mask layer is deposited on a Ge (001) substrate, followed by coating and laser direct writing (LDW) patterning. The sample is then wet etched in a mixed H_3PO_4:H_2O_2:H_2O:C_2H_5OH solution, with a ratio of 2 : 1 : 2 : 4, for 8 min. The dimensions of the squared mesas range from $2 \times 2\,\mu m^2$ to $8 \times 8\,\mu m^2$. A top-view scanning electron microscope (SEM) image of the mesa array is shown in the top right corner of Fig. 1(a).

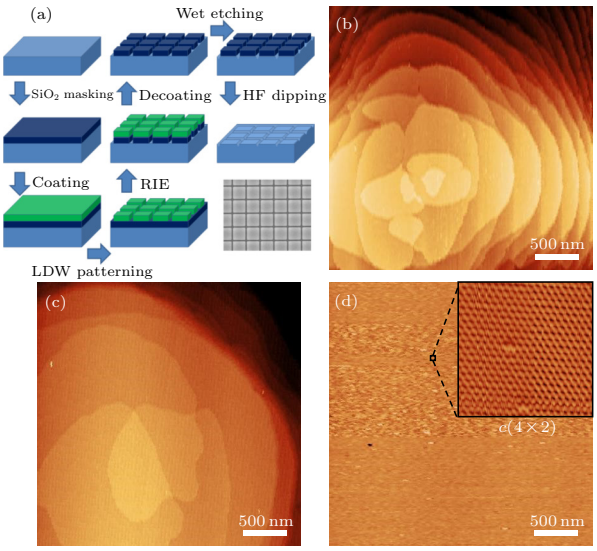

Fig. 1. (a) Process flow diagram of mesa patterning, and overview SEM image of mesa array. STM images of $3.5 \times 3.5\,\mu m^2$ Ge mesa after 6 nm Ge deposition at a substrate temperature of (b) 320 ℃, (c) 400 ℃, and (d) 500 ℃. Scale bar: 500 nm. Atomic resolution STM image shows surface reconstruction of c (4×2).

Having been dipped in diluted HF solution for 1 min to remove the native oxide, and to form a hydrogen passivated surface, the samples are then loaded into an MBE chamber for the epitaxial growth stage of the process. The growth is conducted in a Ⅲ–Ⅴ/Ⅳ joint MBE system, where the sample can be transferred *in situ* between the two chambers. The scanning tunneling microscope (STM) is connected to the MBE system for *in-situ* surface characterization. Once the sample is loaded into the group Ⅳ chamber, the patterned Ge sample is degassed and dehydrogenated at 680 ℃; a 40 nm Ge buffer layer is then deposited at 320 ℃, with a growth rate of 0.1 nm/s.

To obtain the step-free mesa, we firstly investigate its surface morphology under various growth temperatures. Three samples (1, 2, and 3) are grown at a substrate temperature of 320 ℃, 400 ℃, and 500 ℃, respectively. The deposited Ge thickness is 6 nm, with a growth rate of 0.06 nm/min. Figures 1(b), 1(c), and 1(d) show the corresponding surface STM images of the Ge mesas ($3.5 \times 3.5\,\mu m^2$). At 320 ℃, a high-density atomic step is observed [Fig. 1(b)]. By increasing the growth temperature to 400 ℃, the atomic step density is dramatically reduced by at least half [Fig. 1(c)]. Further increasing the growth temperature to 500 ℃ results in the achievement of an atomic step-free Ge surface, as shown in Fig. 1(d). The inset of Fig. 1(d) shows the step-free Ge terrace with a single-phase c (4×2) reconstruction, in contrast to the mixed reconstruction of c (4×2), p (2×2), and (2×1), as observed on the conventional Ge (001) surface.[15]

According to previous studies,[16,17] the two-dimensional Ge island has a critical radius of R_c, which is related to growth temperature and flux rate:

$$R_c \propto \left[\frac{\exp(-\frac{E_{ES}}{kT})}{F}\right]^{1/7}, \quad (1)$$

where E_{ES} represents the Ehrlich–Schwoebel barrier and F is the flux rate.[16,17] If the mesa has a dimension larger than $2R_c$, then Ge islands (single or multiple atomic steps) will always form on the mesa surface. In addition, lager R_c also leads to smaller step density. As such, a high growth temperature results in a step-free mesa, as observed here.

Table 1. Growth condition of samples 4–8.

Sample	4	5	6	7	8
Temperature (℃)	640	740	680	680	680
Ge flux (nm/min)	0.06	0.06	0.06	0.09	0.14

The growth of step-free Ge surfaces at larger sizes requires a relatively higher growth temperature, and a suitable growth rate. As shown in Table 1, five samples grown at higher temperature and different growth rates are investigated here. Samples 4, 5, and 6 are grown at a fixed growth rate of 0.06 nm/min at temperatures of 640 ℃, 740 ℃, and 680 ℃, respectively. Samples 6, 7 and 8 are grown at a fixed growth temperature of 680 ℃, under varying growth rates of 0.06, 0.09, and 0.14 nm/min, respectively. The bottom image in Fig. 2(a) is as schematic representation of the epi-structure, and the top-left atomic force microscope (AFM) image displays the mesa structure. We observe a sidewall with an inclination angle of approximately 5° towards the Ge (001) at all mesa edges. No clear facets are observed, indicating the step-graded slope of the sidewall. Figures 2(b)–2(f) show the AFM images of an $8 \times 8\,\mu m^2$ mesa on each of the five samples, respectively.

As shown in Fig. 2(b), a "crater" structure is formed at 640 ℃. We attribute this to the relatively low growth temperature, at which the Ge adatoms are unable to sufficiently cross the Ehrlich–Schwoebel bar-

rier at the edges. We then increase the growth temperature to 740 ℃. However, as shown in Fig. 2(c), a rough surface is obtained. At such a high growth temperature, bonded Ge atoms begin detaching from the terrace, leaving behind numerous vacancies and pits. At the same time, new steps are formed by the nucleation of the detached Ge atoms. The step-free terrace is therefore no longer stable. This phenomenon is identified as thermal roughening.[18–20] At a growth temperature of 680 ℃, as shown in Fig. 2(d), an $8 \times 8\,\mu m^2$ single-layer Ge terrace is obtained, with several monolayer deep pits localized in the center. Under this condition, the detachment of bonded Ge atoms is relatively weak. We attribute the pits to an accumulation of residual surface vacancies, as the same phenomenon is also observed in Si (001).[21,22]

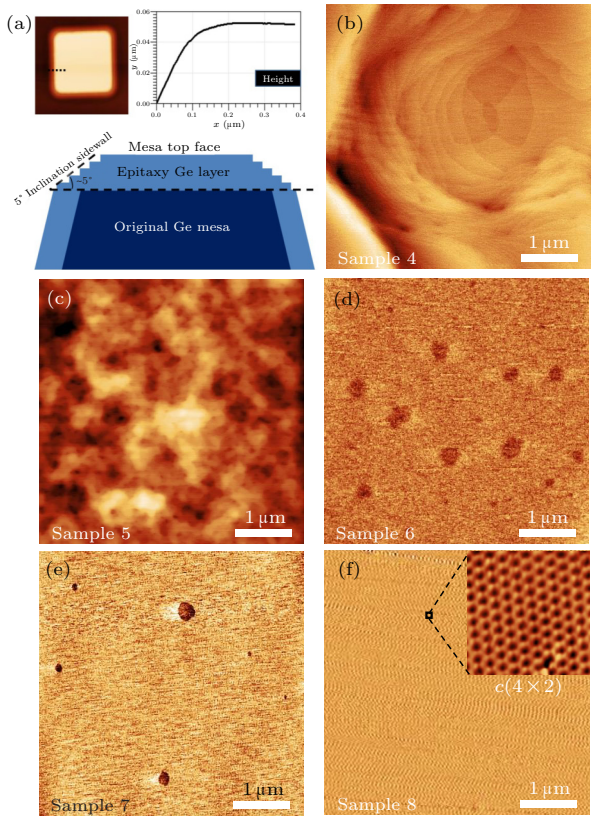

Fig. 2. (a) AFM image and structural schematic of Ge mesa after high-temperature growth. AFM images of $8 \times 8\,\mu m^2$ mesa top-surface for samples 4 (b), 5 (c), and 6 (d). (b) The crater structure at 640 ℃. (c) High-temperature roughening at 740 ℃. (d) Large terrace with monolayer deep pits at 680 ℃. (e) Sample 7 and (f) sample 8 are grown at a higher Ge flux rate, in contrast to sample 6. The scale bar in all images is 1 μm. A 5 μm scale step-free terrace was obtained for sample 8. The atomic-resolution STM image shows c (4 × 2) reconstruction.

At optimum growth temperature of 680 ℃, we investigate the surface morphology under different Ge growth rates. At a growth rate of 0.09 nm/min, as shown in the AFM image of Fig. 2(e), both the size and the density of pits are reduced in comparison to sample 6. This phenomenon indicates that a moderately high Ge flux results in efficient refilling of the vacancies on the terrace. With increasing the Ge growth rate to 0.14 nm/min, a $5 \times 5\,\mu m^2$ step-free terrace is obtained, as shown in Fig. 2(f). The atomic resolution STM image in the inset of Fig. 2(f) also shows a perfect single-phase c (4×2) surface reconstruction, as obtained in Fig. 1(d) at 500 ℃. If we further increase the growth rate to 0.18 nm/min, however, a crater structure forms once again, due to the excessive flux rate.

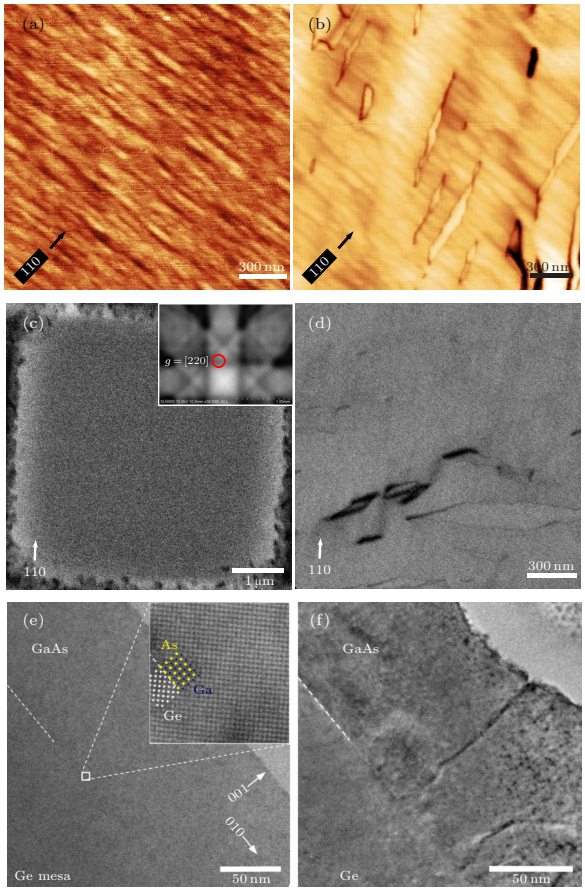

Fig. 3. (a) AFM, (c) ECCI, (e) cross-sectional TEM images of the sample following deposition of 120-nm-thick GaAs on a $5 \times 5\,\mu m^2$ step-free Ge mesa. ECCI diffraction vector $\boldsymbol{g} = [220]$ is indicated by a red ring in the inset of (c). (e) Cross-sectional TEM and high-resolution inset show a defect-free heterostructure interface. For comparison, (b), (d), and (f) show the corresponding results for conventional Ge (001).

Having successfully obtained an atomic step-free Ge terrace (sample 8), the sample is then transferred to a Ⅲ–Ⅴ growth chamber for GaAs growth. The arsenic pre-layer is deposited by exposing the substrate to excessive As_4 flux at 450 ℃ for 8 min. In order to reduce Ge/GaAs intermixing, a low-temperature GaAs buffer layer (450 ℃) with thickness of 20 nm is grown on a $5 \times 5\,\mu m^2$ Ge step-free terrace at a growth rate of 0.06 nm/s. An additional 100 nm GaAs layer is then deposited at 560 ℃. Material characterizations, including surface AFM, ECCI, and cross-sectional TEM

images, are shown in Fig. 3. Here, we compare the AFM, ECCI and TEM results between GaAs on a step-free Ge terrace, and those on a standard Ge substrate. Figure 3(a) shows an APD-free GaAs layer on step-free Ge mesa, with an rms surface roughness of 0.176 nm, while the GaAs layer grown on conventional Ge shows a number of APDs in Fig. 3(b), together with an rms roughness of 1.54 nm. Since the penetration depth of back-scattered electrons is comparable to the GaAs layer thickness, ECCI should effectively detect any defects generated in the GaAs/Ge heterostructure. The ECCI is obtained at a beam voltage of 15 kV, and an emission current of 1.89 nA; a clear electron channeling pattern is acquired at a magnification of 50×, as shown in the inset of Fig. 3(c). The results of ECCI at a diffraction vector of $\boldsymbol{g} = [220]$ are shown in Fig. 3(c), where no defect is observed over the entire mesa structure, which is attributed to an ideal GaAs/Ge interface. In comparison, defects are clearly visible for GaAs grown on a standard Ge substrate, as shown in Fig. 3(d). Cross-sectional TEM comparisons between GaAs on a Ge terrace and GaAs deposited directly onto a standard Ge substrate are shown in Figs. 3(e) and 3(f). By implementing an atomic step-free Ge surface, Ga and As atoms are arranged in an orderly fashion on the Ge lattice, as displayed in the inset of Fig. 3(e). APDs and SFPs are both absent across the entire GaAs layer. In Fig. 3(f), for GaAs directly grown on the Ge substrate, APDs are initiated at the interface, and penetrate through the GaAs, leading to a rough GaAs surface. Overall, by means of a step-free Ge mesa structure, APDs and stacking faults are avoided at the GaAs/Ge interface; as such, a defect-free GaAs layer is acquired.

In order to further verify the material's quality, a three-layer InAs/GaAs dot-in-a-well (DWELL) structure is deposited onto a GaAs/Ge terrace array. The mesa size is $4 \times 4\,\mu m^2$, with the period of the mesa array being approximately 5.5 μm. We calculate that the effective DWELL area constitutes approximately 50% of the whole mesa array region. Figure 4(a) shows a schematic of the InAs/GaAs DWELL structure. The InAs QDs are self-assembled by a 0.81 nm InAs layer, sandwiched between a 1.5 nm $In_{0.17}Ga_{0.83}As$ wetting layer and a 6 nm $In_{0.17}Ga_{0.83}As$ capping layer. The three-layer InAs/GaAs DWELL is sandwiched between two 50 nm $Al_{0.5}Ga_{0.5}As$ cladding layers. The AFM image in Fig. 4(b) shows that InAs/GaAs QDs are grown on the GaAs/Ge template, leaving APDs and stacking fault surface pits at the mesa sidewall, and trenches between the terrace arrays. InAs QDs are distributed uniformly on the GaAs/Ge mesa, at a density of $4.5 \times 10^{10}/cm^2$, with a lateral diameter and height of approximately 50 nm and 10 nm, respectively, as shown in the inset of Fig. 4(b). Both the density and size are similar to those of InAs QDs deposited on a standard GaAs (001) substrate. The room-temperature PL spectra are shown in Fig. 4(c), excited by a cw pump laser with a beam spot diameter of around 50 μm, where the PL peak of the InAs QDs on the step-free Ge mesa is localized at 1280 nm. The PL peak intensity of the InAs QDs on GaAs/Ge mesa array (red line) is about 40% of those on GaAs (blue line), contributing to the previously calculated 50% effective area. The slight peak broadening is attributed to the additional signal generated from non-uniform InAs QDs, localized at mesa edges and trenches. In contrast, the PL peak intensity of InAs QDs on a non-patterned GaAs/Ge area (black line) is 1/10 of those on GaAs/Ge mesas. By performing the PL experiments, we verify that GaAs grown on a step-free Ge mesa provides a high-quality heteroepitaxial platform for Ⅲ–Ⅴ based materials.

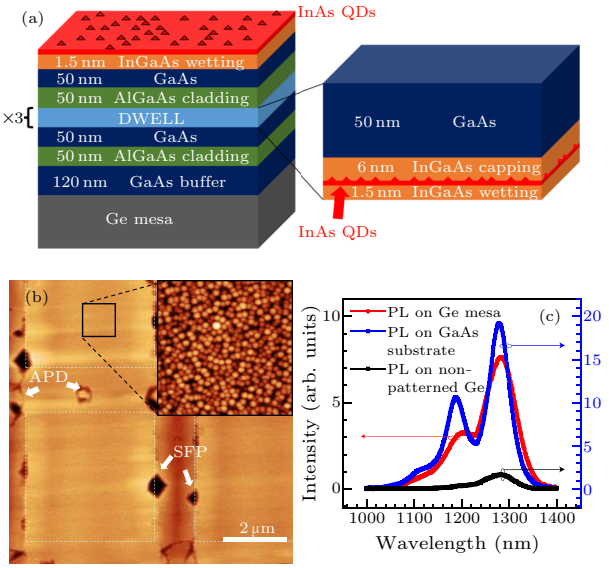

Fig. 4. (a) Schematic of DWELL structure on Ge mesa. (b) AFM image of $4 \times 4\,\mu m^2$ mesa array after DWELL growth. The inserted AFM image (top-right) shows the QDs. (c) Room-temperature PL spectra of DWELL. Red and blue lines denote the spectra of DWELL on a GaAs/Ge mesa and GaAs (001), respectively. The black line indicates the spectrum of DWELL on non-patterned normal GaAs/Ge.

In conclusion, by systematically studying Ge terrace growth under a variety of growth conditions, a step-free Ge terrace up to a $5 \times 5\,\mu m^2$ scale is obtained at 680 ℃, at a growth rate of 0.14 nm/min. An ultra-high-quality GaAs/Ge heterostructure is achieved on a step-free Ge mesa, where APDs and SFP are fully avoided. A GaAs layer with no observed defects, and 0.176 nm of rms surface roughness is achieved. In contrast to GaAs on an offcut Ge substrate, MEE process and dislocation filtering techniques are no longer necessary. These GaAs/Ge mesa arrays may be applied in high performance CMOS transistors and GaAs/Ge quantum well topological devices. Furthermore, an InAs/GaAs DWELL structure is grown on the Ge

mesa, exhibiting a PL intensity similar to the strength of those grown on a GaAs substrate. This template could lead to development of high-performance Ⅲ–V based optoelectronic devices on Ge substrates, such as photo-detectors and micro-laser arrays.

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