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Towards Fabrication of Atomic Dopant Wires via Monolayer Doping Patterned by Resist-Free Lithography

Chufan Zhang(张楚凡)[1†], Ke Li(黎珂)[1†], Xiaoxian Zang(臧孝贤)[2], Fuyuan Ma(马福元)[2], and Yaping Dan(但亚平)[1*]

[1] *University of Michigan–Shanghai Jiao Tong University Joint Institute, Shanghai Jiao Tong University, Shanghai 200240, China*

[2] *Key Laboratory of Solar Energy Utilization & Energy Saving Technology of Zhejiang Province, Zhejiang Energy R&D Institute Co., Ltd., Hangzhou 311121, China*

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Fabrication of atomic dopant wires at large scale is challenging. We explored the feasibility to fabricate atomic dopant wires by nano-patterning self-assembled dopant carrying molecular monolayers via a resist-free lithographic approach. The resist-free lithography is to use electron beam exposure to decompose hydrocarbon contaminants in vacuum chamber into amorphous carbon that serves as an etching mask for nanopatterning the phosphorus-bearing monolayers. Dopant wires were fabricated in silicon by patterning diethyl vinylphosphonate monolayers into lines with a width ranging from 1 μm down to 8 nm. The dopants were subsequently driven into silicon to form dopant wires by rapid thermal annealing. Electrical measurements show a linear correlation between wire width and conductance, indicating the success of the monolayer patterning process at nanoscale. The dopant wires can be potentially scaled down to atomic scale if the dopant thermal diffusion can be mitigated.

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Following Moore's law, semiconductor industry has witnessed an exponential growth over the past few decades. Doping, a crucial process in semiconductor manufacturing, comes across an enormous challenge as the feature size of modern transistors shrinks to sub-10 nm scale where the number and position of individual dopants will influence device performances.[1] Deterministic doping has been placed as one of the highest priorities since the 2011 International Technology Roadmap for Semiconductors (ITRS). Although methods like single ion implantation[2–4] and STM based hydrogen lithography[5–8] have been demonstrated for single dopant manipulation, a parallel process for realization of scalable dopant manipulation has not been found so far.

It may be feasible to control dopants at large scale by nanopatterning the self-assembled dopant carriers. Monolayer doping (MLD) has been proved to be a mild and controllable technique for introducing dopants into silicon.[9–21] Dopant-bearing molecules are first covalently bonded to hydrogen-terminated silicon surfaces via hydrosilylation. The dopants are then driven into bulk silicon and activated during rapid thermal annealing process, sub-5 nm ultrashallow junctions have been fabricated.[10] MLD has shown flexibility and precision in introducing various impurity dopants (P,[9,10,12,13,16] B,[9,11,16,18,19] As,[20,21] N,[17] etc.) into silicon. Introducing dopants via MLD into other semiconductors such as Ge,[22,23] GaAs,[24] and InAs[25] has also been explored. However, most of the researches in this field focus on the synthesis of precursors and wafer scale doping. Selective doping, which has practical significance in device fabrication, has been less explored in MLD research.

Previously, we reported a selective doping strategy by nanopatterning self-assembled monolayers (SAM) to a few nanometers based on standard nanofabrication processes using hydrogen silsesquioxane (HSQ) resist.[26] While HSQ is widely used as negative resist for scientific research, it has poor resistance against hydrogen fluoride (HF) etching that was used to remove unprotected dopant-bearing molecules. As a result, it is challenging to use HSQ alone as an etching mask to nanopattern SAM layers. In this work, we explored the feasibility of a resist-free lithography technique to nanopattern SAM layers for potential atomic scale doping. The resist-free lithography is to use electron beam exposure to decompose organic contaminants in vacuum chamber into amorphous carbon that serves as an etching mask for nanopatterning the phosphorus-bearing monolayers. We first demonstrated that SAM layers can be easily removed after successive steps of plasma enhanced atomic layer deposition of SiO_2 and HF etching. Then we showed that e-beam induced amorphous carbon template has excellent resistance against HF solution. Using this carbonaceous template, we realized the nanoscale patterning of phosphorus-containing mono-

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†Chufan Zhang and Ke Li contributed equally to this work.

*Corresponding author. Email: yaping.dan@sjtu.edu.cn

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layers. For quantitative characterizations, dopant wires with width ranging from 1 μm down to 8 nm were fabricated in silicon using the proposed strategy. Low temperature measurements show that the wire conductance is linearly correlated with the wire width unless the wire width is less than 100 nm. To further improve patterning resolution to atomic scale, new annealing techniques such as pulsed laser annealing should be adopted to mitigate the diffusion length.

Results and Discussion. We first grafted a monolayer of diethyl vinylphosphonate (DVP) molecules on intrinsic silicon wafers (>10000 Ω·cm) and then selectively protected lines of the monolayer with e-beam induced amorphous carbon to form dopant wires. To prevent phosphorus evaporation during e-beam irradiation, a thin layer of silicon oxide was first deposited upon the prepared monolayers by plasma enhanced atomic layer deposition (PE-ALD) with bis(t-butylamino)silane and oxygen plasma as precursors. Previously, we demonstrated that dopant-bearing molecules can be removed with a combination of oxygen plasma and HF etching.[26] Considering that DVP molecules tend to be oxidized in the initial phase of PE-ALD process, the resultant phosphorus-containing compounds can be readily removed by HF etching. XPS was used to characterize sample surfaces after the three sequential steps of surface modification and HF etching. The XPS results are shown in Figs. 1(a)–1(c).

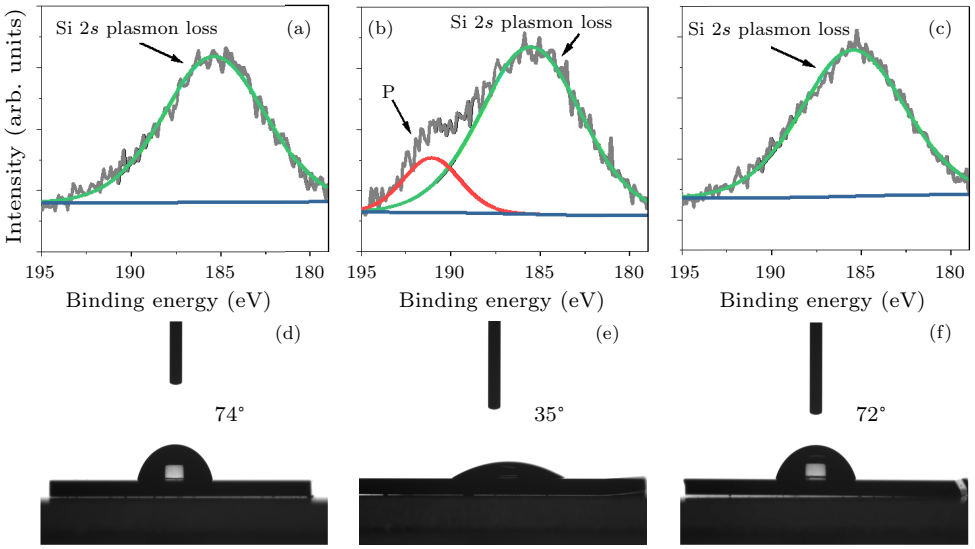

Fig. 1. P 2*s* spectra acquired from (a) blank sample, (b) DVP modified sample, and (c) HF etched sample; and the corresponding contact angle results are shown in (d), (e), and (f), respectively.

Figures 1(a) and 1(b) show the P 2*s* spectra obtained from the sample before and after surface functionalized with DVP molecules, respectively. The broad bump centered around 185 eV is assigned to silicon plasmon loss, while the side shoulder at 191 eV is ascribed to P 2*s* orbitals in P–O bonds. The presence of P 2*s* orbital indicates the successful immobilization of DVP molecules on silicon surfaces. The immobilization of DVP molecules was further confirmed by water contact angle measurements. Compared to the bare silicon sample [Fig. 1(d)], the contact angle of the DVP modified sample drops from 74° to 35° due to the containing of more hydrophilic headgroups (P=O) of DVP molecules. After oxidation in PE-ALD process followed by etching in 2.5% HF for 20 s, the P 2*s* side shoulder disappears [Fig. 1(c)] and the contact angle is recovered to 72°. These observations show the successful removal of phosphorus compounds.

The above processes were further confirmed by electrical measurements. All the three samples were capped with SiO_2 by spin-coating spin-on-glass (SOG, IC1-200, Futurrex Inc) and then annealed at 1050℃ for 30 s, which will drive phosphorus dopants into silicon. The capping layer was then removed by immersing in buffered oxide etchant (BOE) for 5 min. For electrical characterization, aluminum contacts were deposited on four corners of each sample by thermal evaporation. Van der Pauw methods were used to probe the sheet resistance of these three samples and the results are summarized in Table 1. The sheet resistance of the control sample and P-doped sample were measured as 336.1 kΩ/sq and 4.9 kΩ/sq, respectively. This contrast in sheet resistance indicates that phosphorus dopants were successfully driven into silicon from the DVP molecules. Instead of going through the thermal annealing process, a surface-functionalized sample was treated with PE-ALD and BOE etching. The sheet resistance of this sample was increased to 224.2 kΩ/sq, which is comparable to the control sample and close to the theoretical value of intrinsic silicon wafer we used. This indicates that the oxidation in PE-ALD followed by BOE etching has completely removed phosphorus compounds from the functionalized surfaces, consistent with the XPS and contact

angle measurements above.

Table 1. Sheet resistances measured by van der Pauw technique.

Sample	R_s (kΩ/sq)
Control sample (annealed without surface functionalization)	336.1
DVP functionalized	4.9
DVP functionalized, ALD SiO_2 10 nm, 2.5% HF 20 s	224.2

In our previous work, HSQ is used as negative electron beam resist for monolayer patterning. While HSQ is widely used for scientific research, it has poor resistance against HF etching that was used to remove unprotected dopant-bearing molecules. As a result, it is challenging to use HSQ alone as an etching mask to nanopattern SAM layers. Here we show that nanometer scale amorphous carbon pattern can be readily created by e-beam exposure. Hydrocarbon molecules in vacuum chamber (likely from vacuum grease) tend to decompose under e-beam irradiation, resulting in amorphous carbon deposition on sample surface. The resolution of deposited pattern depends on the e-beam size. In contrast to HSQ, the amorphous carbon is highly resistive to HF etching, making it an attractive potential alternative to HSQ resist. To demonstrate this resist-free lithography for nanopatterning dopant carrier molecules, we first investigated the amorphous carbon deposition by performing e-beam exposure at different dosages on a clean silicon wafer. The obtained samples were characterized with atomic force microscopy (AFM). The designed line structures with a width varying from 10 to 80 nm can be clearly observed, as displayed in Fig. 2(a). The measured thicknesses of carbon wires with different dosages were summarized in Figs. 2(d) and 2(e). The thicknesses of carbon wires are dependent on the e-beam doses. Indeed, a linear correlation between thickness and e-beam dose was observed for various line widths. However, the difference in line slope indicates the different deposition rates among the wire widths. We find that the deposition rate linearly increases with wire width when width smaller than 50 nm. The deposition rate tends to saturate with wire width wider than 50 nm, with a rate of ∼0.022 nm per unit dose. This width-related deposition rate, as reflected in Fig. 2(e), can be explained by the proximity effect of e-beam irradiation. As the e-beam scanning across the sample surface, the scattered electrons also contribute to the carbon deposition in the nearby region, which in return leads to the thickness increase of the resultant carbon wires.

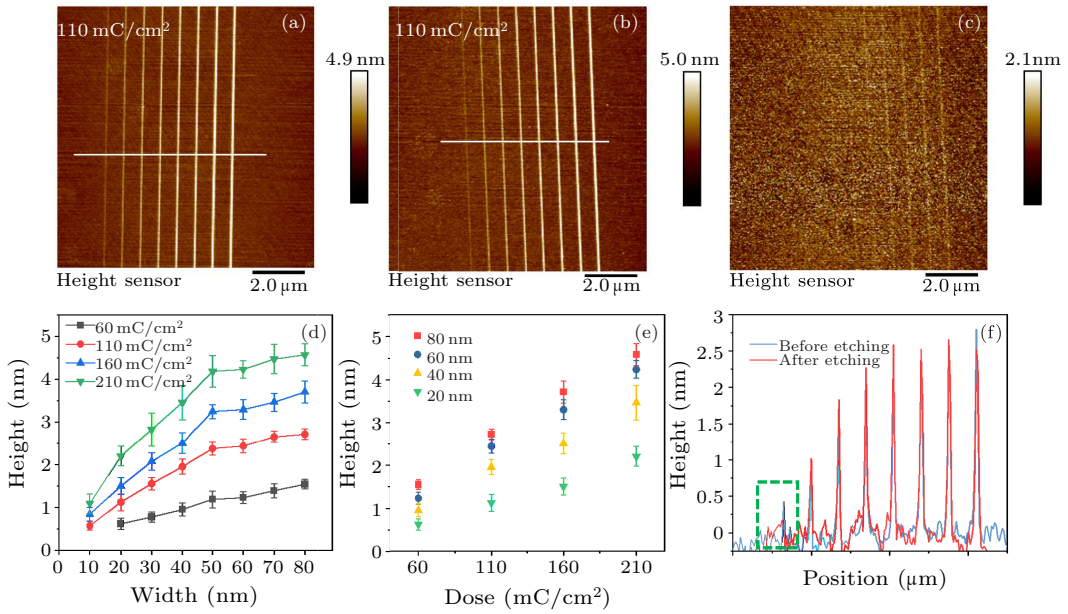

Fig. 2. AFM image of carbon wires with width ranging from 10 to 80 nm deposited with e-beam dose of 110 mC/cm^2, (a) before HF etching, (b) after HF etching, and (c) after O_2 plasma cleaning. (d) Height of carbonaceous wires vs line width for exposure dose of 60, 110, 160, 210 mC/cm^2, extracted from AFM images before HF etching. (e) Height of carbonaceous wires vs exposure dose for wire widths of 20, 40, 60, 80 nm, extracted from AFM images before HF etching. (f) Line profile extracted from Figs. 2(a) and 2(b).

The same sample was then immersed in 2.5% HF solution for 60 s. In Fig. 2(b), the carbon wires created with a dose of 110 mC/cm^2 has hardly changed after the wet etching process. Figure 2(f) shows the height information extracted from Figs. 2(a) and 2(b). The height of this set of carbon wires remains essentially the same except for those with initial height less than 0.5 nm (marked with green frame). The results indicate that the etching resistance of the deposited amorphous carbon against hydrofluoric acid is associated with film thickness. The amorphous carbon layer could provide effective protection only if the thickness is greater than 0.5 nm. A control sample was further treated with oxygen plasma for 60 s. As displayed in

Fig. 2(c), the carbon wires were almost completely removed, which further confirmed the existence of e-beam induced carbon.

Dopant wires in silicon were fabricated following the procedure illustrated in Fig. 3(a). DVP molecules were first grafted on the device layer of SOI substrate (>10000 Ω·cm) that were cleaned properly (see the experimental section for details). SiO_2 of 30 nm was then grown upon the monolayers using a PE-ALD equipment (Beneq TFS-200, Finland) to prevent phosphorus evaporation during the following e-beam irradiation process. Carbon wires were formed on the SiO_2 by e-beam induced carbon deposition, which acted as an etching mask to protect the underlying SiO_2 and DVP from being etched away by HF solution. The resulting sample was then annealed at 1050℃ for 90 s, to drive in phosphorus dopants and to form dopant wires. To facilitate electrical measurements, each wire is connected to a pair of pre-ion-implanted pads.

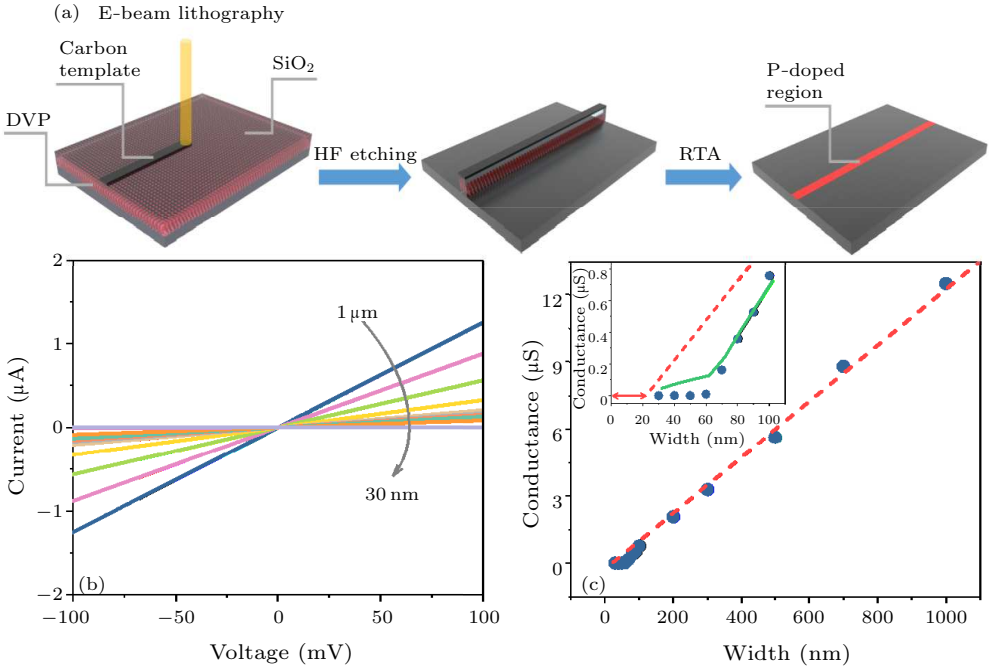

Fig. 3. (a) Process flow of the selective doping strategy. (b) Two probe measurements at 77 K of I–V curves of dopant-wire devices with width ranging from 30 nm to 1 μm. (c) Conductance of dopant-wire devices as a function of width ranging from 30 nm to 1 μm, measured at 77 K.

The conductivity of silicon substrate at room temperature is relatively high. To eliminate background current, dopant wire devices were characterized using a cryogenic probe station at 77 K. Figure 3(b) shows the current-voltage (I–V) characteristics for dopant wires with nominal width varying from 30 nm to 1 μm. All the dopant wires show ohmic I–V characteristics, indicating the success of the whole selective doping process. The conductance of each dopant wire is extracted and shown in Fig. 3(c). For wires wider than 100 nm, the conductance shows a linear dependence on wire width. From the linear correlation, we found that the sheet resistance of wires is calculated to be 3.2 kΩ/sq at 77 K, which indicates that a relatively high concentration of phosphorus has diffused into silicon substrate. However, the fitted line (red dash) does not project to zero at zero width. An offset of 22 nm was observed at the x axis, as displayed in the inset of Fig. 3(c). This phenomenon can be explained by the side etching of SiO_2 during HF etching process. During the monolayer patterning process, the carbonaceous pattern was used to prevent the underlying SiO_2 from being attacked by HF solution. However, the HF etching of SiO_2 is isotropic. As the sidewalls of patterned wires are continuously exposed to HF solution, the wire will be continuously narrowed. In our case, approximately 11 nm has been etched away on both sides of the wires, which is reasonable considering the 30-nm thickness of SiO_2 we used. For the nominal wire width of 30 nm, the actual doping width is ∼8 nm. However, due to the thermal diffusion as we discussed below, we actually lost control of dopants within this 8-nm-wide wire.

For wires narrower than 100 nm, a deviation of wire conductance from the fitted line can observed in the inset of Fig. 3(c). This result can be interpreted by the diffusion induced attenuation in dopant concentration during thermal annealing process, as described in our previous report.[26] Using the mentioned method, we find the best fit when diffusion length $\sqrt{Dt} \sim 20$ nm by enumerating possible diffusion lengths [green line in Fig. 3(c)]. For an annealing time of 90 s, the diffusion

coefficient is calculated to be $4.4 \times 10^{-14}\,\mathrm{cm}^2/\mathrm{s}$. This value is quite close to previous literature report,[27] where the diffusivity D can be expressed as Eq. (1) with the corresponding value $3.14 \times 10^{-14}\,\mathrm{cm}^2/\mathrm{s}$.

$$D = 5.7 \exp\Big[-\frac{3.75(\mathrm{eV})}{kT}\Big]. \tag{1}$$

In the cross-section perpendicular to the wire axial direction, the x axis is pointing to bulk silicon from surface and the y axis is along the silicon surface. The doping profile $C(x, y, t)$ of dopant wire can be derived as Eq. (2) following the "source-limited" diffusion model, where N_0 is surface dopant concentration, D is diffusivity, t is annealing time, and w is line width.[26]

$$C\Big(x, y, t\Big) = \frac{N_0}{2\sqrt{\pi D t}} e^{-\frac{x^2}{4Dt}} \Big[\mathrm{erf}\Big(\frac{y + w/2}{2\sqrt{Dt}}\Big) - \mathrm{erf}\Big(\frac{y - w/2}{2\sqrt{Dt}}\Big)\Big]. \tag{2}$$

From the room temperature measurement, the sheet resistance of wires is calculated to be $2.35\,\mathrm{k\Omega/sq}$. For a diffusion length of 20 nm, the surface dopant concentration of $1.26 \times 10^{13}\,\mathrm{cm}^{-2}$ can be found by solving Eq. (3).

$$\begin{aligned} R_{\mathrm{s}}^{-1} &= \int_0^{\infty} q\mu C(x,t)dx \\ &= \int_0^{\infty} q \times \Big(\mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + [\frac{C(x,t)}{N_{\mathrm{ref}}}]^{\alpha}}\Big) \\ &\quad \times \frac{N_0}{\sqrt{\pi D t}} e^{-\frac{x^2}{4Dt}} dx. \end{aligned} \tag{3}$$

Typically, $\mu_{\min} = 68.5\,\mathrm{cm}^2/\mathrm{Vs}$, $\mu_{\max} = 1414\,\mathrm{cm}^2/\mathrm{Vs}$, $N_{\mathrm{ref}} = 9.2 \times 10^{16}\,\mathrm{cm}^{-3}$, $\alpha = 0.711$.

Clearly, the maximum doping concentration is located at $C(0, 0, t)$. For a given diffusion length, $C(0, 0, t)$ is proportional to $\mathrm{erf}(\frac{w}{4\sqrt{Dt}})$. Using Eq. (2), a peak concentration of $3.55 \times 10^{18}\,\mathrm{cm}^{-3}$ can be calculated for wires wider than 100 nm. The peak concentration of dopant wire will decrease when the diffusion length of phosphorus dopant is comparable to wire width. A slight decrease of peak concentration may result in the transition from degenerate to non-degenerate doping wires. As we all know that the ionization rate of phosphorus dopants in degenerated region at 77 K is much higher than the rate in non-degenerated region. As the wire narrows down, the non-degenerate part of wire gradually dominates the wire conductance, and hence, deviates from the linear correlation.

In conclusion, a resist-free patterning strategy has been developed for selective doping of silicon via self-assembled monolayers. With the combination of e-beam induced carbon deposition and HF etching, phosphorus wires with width ranging from 1 μm down to 8 nm were fabricated and characterized. For wires with wider width, low temperature electrical measurement shows a linear correlation between width and conductance, which indicates the success of the whole selective doping process. The fitted sheet resistance of $3.2\,\mathrm{k\Omega/sq}$ at 77 K indicates that a relatively high concentration of phosphorus has diffused into silicon substrate. A transition from degenerate doping to fully non-degenerate doping was also observed for wires with narrower width as previously mentioned,[26] which should be ascribed to the relatively large diffusion length of phosphorus dopants. The present work may provide a possible pathway for deterministic doping of silicon at atomic scale if the dopant thermal diffusion is mitigated by adopting flash annealing or laser annealing techniques to greatly shorten the diffusion length and improve the dopant incorporation rate.

Experimental Section—Monolayer Formation. Alignment markers were first etched into on SOI wafer [6 inch, (100)-oriented, 10-μm-thick device layer, resistivity >10 kΩ·cm, Ultrasil LLC] with a depth of 3 μm by photolithography and reactive ion etching. To facilitate the formation of Ohmic contact of each dopant wire device, a second photolithography was conducted on the same substrate to define the contact regions, followed by ion implantation of phosphorus dopants at a concentration of $10^{19}\,\mathrm{cm}^{-3}$. After striping of photoresist, the SOI wafer was cleaved into 1.5 cm by 1.5 cm pieces, and thoroughly cleaned with organic solvents (acetone, ethanol) and piranha solution (H_2SO_4:H_2O_2 = 3:1) to remove organic residues. The cleaned substrate was then rinsed with DI water and dried under nitrogen flow.

The surface functionalization of hydrogen-terminated silicon with DVP molecules was followed by previous literature reports.[16,26] DVP (> 98%, TCI Shanghai) was first diluted with anhydrous 1,3,5-trimethylbenzene (> 98%, water < 50 ppm, Aladdin) at a ratio of 1 : 12 in a glovebox filled with Ar, followed by deoxygenation using Ar bubbling for 10 min. The cleaned SOI sample was immersed in 2.5% HF solution for 90 s to remove native oxide and to form a dense hydrogen terminated surface. The freshly etched sample was quickly rinsed with DI water and dried by nitrogen, and immediately transferred into the prepared precursor mixture. The hydrosilylation process was performed at 160℃ overnight using a heating jacket, and the reaction was stopped by removing the heat. The obtained sample was ultrasonicated with acetone, ethanol and DI water for 3 min each to remove any physiosorbed molecules.

Patterning of Self-Assembled Monolayers. SiO_2 films with a thickness of 30 nm were first grown on the prepared substrate by PE-ALD, to prevent the dopant evaporation during e-beam irradiation. E-beam induced carbon deposition was performed on a Vistec EBPG-5200+ electron-beam lithography system, with an acceleration voltage of 100 keV, beam current of 0.3 nA, and dose ranging from 10 to $210\,\mathrm{mC/cm}^2$. Thin layer of amorphous carbon was deposited onto desired region and forming wires with width ranging from 30 nm to 1 μm to connect to a pair of prepared

ion-implanted pads. Nanopatterning of DVP monolayers was achieved by dipping the fabricated sample into 2.5% HF solution for 20 s, where the region protected by carbon wires would stay intact while the exposed SiO_2 along with underlying DVP molecules can be etched away. The etched sample was then rinsed with DI water and dried under nitrogen flow.

Capping Layer Deposition and Thermal Annealing. The carbon template was first removed by oxygen plasma cleaning (Harrick Plasma, USA) for 1 min to reduce carbon contamination. Then, a thin layer of silicon oxide was applied on the substrate by spin-coating of IC1-200 (Futurrex Inc, USA), as previously described.[12,17] The sample was annealed at 1050℃ for 90 s, with a ramping rate of 10℃/s. After annealing, the capping layer was removed by BOE solution ($HF:NH_4F = 6:1$, J.T. Baker Co. USA).

Electrical Characterizations. Metal contacts were made on ion implanted area of dopant wire devices by photolithography and thermal evaporating 200-nm aluminum. Electrical measurements were performed on a cryogenic probe station (Model TTPX, Lake Shore Cryotronics, Inc., USA) at 77.6 K. A Keysight B1500 A semiconductor device parameter analyzer was used to generate and collect voltage/current data.

The devices were fabricated at the center for Advanced Electronic Materials and Devices (AEMD), and XPS, AFM and contact angle measurements were conducted at the Instrumental Analysis Center (IAC), Shanghai Jiao Tong University.

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