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Giant-Capacitance-Induced Wide Quantum Hall Plateaus in Graphene on $LaAlO_3/SrTiO_3$ Heterostructures

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Hybrid structures of two distinct materials provide an excellent opportunity to optimize functionalities. We report the realization of wide quantum Hall plateaus in graphene field-effect devices on the $LaAlO_3/SrTiO_3$ heterostructures. Well-defined quantized Hall resistance plateaus at filling factors $\upsilon = \pm 2$ can be obtained over wide ranges of the magnetic field and gate voltage, e.g., extending from 2 T to a maximum available magnetic field of 9 T. By using a simple band diagram model, it is revealed that these wide plateaus arise from the ultra-large capacitance of the ultra-thin LAO layer acting as the dielectric layer. This is distinctly different from the case of epitaxial graphene on SiC substrates, where the realization of giant Hall plateaus relies on the charge transfer between the graphene layer and interface states in SiC. Our results offer an alternative route towards optimizing the quantum Hall performance of graphene, which may find its applications in the further development of quantum resistance metrology.

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As a typical two-dimensional (2D) Dirac electron system, graphene has attracted intense interest due to its unique electronic features, such as the bipolar field effect, non-zero Berry phase, and energy-independent Fermi velocity.[1,2] Especially, Dirac-type carriers of this semi-metal lead to exceptionally large cyclotron gaps in the Landau level (LL) spectrum, making graphene competitive for realizing the quantum Hall effect (QHE) at much reduced magnetic fields and/or much higher temperatures.[3−6] As a consequence, there have been extensive efforts devoted to optimizing the QHE performance of graphene towards the development of quantum resistance metrology beyond conventional GaAs systems,[7] and the epitaxial graphene grown on SiC substrates (G/SiC) has proven to be a suitable choice.[8−10] Besides the relatively large size of the as-grown graphene wafer that can sustain a large breakdown current of the QHE, the remarkable wide Hall plateau in G/SiC allows resistance quantization over the entire sample despite local variations of carrier density, enabling the realization of the quantized Hall resistance with high precision.[11] In G/SiC, the acquisition of wide Hall plateau is rooted in the electric-field- or magnetic-field-dependent charge transfer between interface states in SiC and the LL states in graphene.[12,13] However, this charge transfer process normally leads to a strong doping of graphene,[14] and additional carrier density control is thus needed to enter into a well-defined quantized Hall region within a small magnetic field.[7]

On the other hand, constructing graphene-based hybrid structures has been demonstrated to be a ready and effective way to tune the electronic transport properties of graphene. A typical example is the graphene field-effect device built on the $LaAlO_3/SrTiO_3$ (LAO/STO) heterostructure, a representative oxide heterostructure hosting two-dimensional electron gas (2DEG) at the interface.[15,16] In this graphene-$LaAlO_3$-$SrTiO_3$ hybrid device (denoted as G-LAO-STO), an ultra-low operating voltage is needed when utilizing the ultra-thin LAO layer as the dielectric layer.[17] Significant improvement of carrier mobility for graphene is readily achieved and the quantum transport performance also gets significantly enhanced, benefiting from the screening effects of LAO/STO on multiple scattering processes.[18] Our recent work further demonstrated that well-defined QHEs can be realized under relatively modest conditions compared with most other graphene devices.[19]

In this study, similar hybrid structures are fabricated, and the detailed characteristics of the QHE in graphene are systematically investigated. Well-

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defined quantized Hall resistance plateaus at filling factors $v = \pm 2$ can be obtained over a wide range of the magnetic field and gate voltage. By analyzing the Hall data via a simple band diagram model,[12,13,20] the realization of wide Hall plateaus is revealed to originate from the ultra-large gate capacitance of the ultra-thin LAO layer. Our results thus reveal a brand-new route to enlarge the operational parameter space of the QHE in graphene. This G-LAO-STO hybrid device also offers an alternative for developing quantum resistance metrology with high precision.

The G-LAO-STO devices, as schematically shown in Fig. 1(a), were fabricated following the established procedures detailed in our previous report.[19] LAO/STO (001) heterostructures were fabricated via pulsed laser deposition, with the thickness of the grown LAO layer monitored by reflection high-energy electron diffraction intensity oscillations. Monolayer graphene flakes were mechanically exfoliated from Kish graphite and transferred onto the LAO/STO surface via a completely dry transfer method.[21] Figure 1(c) shows the typical scanning electron microscope image of the finally obtained G-LAO-STO devices. The Hall-bar electrodes were patterned by electron-beam lithography, and Ti/Pd/Au films with the thickness of 0.3/5/40 nm were deposited as electrode materials via e-beam evaporation. Finally, the graphene layer was also etched into the Hall-bar geometry through an oxygen plasma etching process. The good conductivity of the LAO/STO interface in the G-LAO-STO device was carefully verified, with the basic transport properties consisting well with those in our previous studies.[22,23] The BN-encapsulated graphene devices (BN-G-BN, see Fig. 1(b)) were fabricated as a "control sample". The stack was assembled onto the SiO_2/Si substrate via the typical van der Waals assembly technique,[24] and shaped into a Hall-bar geometry by electron-beam lithography and reactive ion etching (Fig. 1(d)).

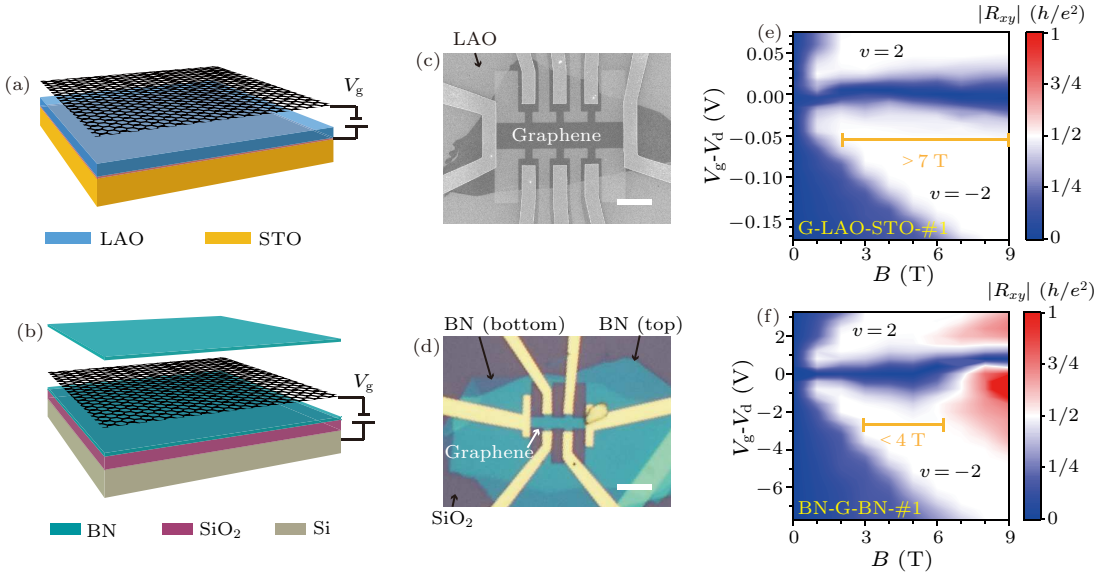

Fig. 1. [(a),(c)] Schematic illustration and scanning electron microscope image of the G-LAO-STO device, respectively. [(b),(d)] Schematic illustration and the optical microscope image of the BN-G-BN device, respectively. The scale bars in (c) and (d) are 5 μm. [(e),(f)] $|R_{xy}|$ as a function of B and $(V_g - V_d)$ measured at 1.5 K for G-LAO-STO-1 and BN-G-BN-1, respectively. V_d is the gate voltage corresponding to the Dirac point of graphene.

The transport measurements were performed in an Oxford Instruments ^{4}He cryostat with standard AC lock-in techniques. For both of the devices, the carrier polarity and density of graphene can be readily tuned by applying a gate voltage (V_g). In G-LAO-STO, the ultra-thin LAO layer (< 2 nm for 5-uc LAO) and the conducting LAO/STO interface are utilized as the natural dielectric layer and the gate electrode (Fig. 1(a) and Fig. S1(a) in the supplementary material), respectively. While for BN-G-BN, the 300-nm-thick SiO_2 layer serves as the back-gate dielectric layer. For G-LAO-STO the typical carrier mobility extracted from Hall measurements (e.g., 27000 $cm^2/V{\cdot}s$ at a carrier density $n \sim 9.1 \times 10^{10}\,cm^{-2}$ and temperature $T = 1.5$ K) is significantly enhanced as compared with previous pristine graphene on SiO_2, but is still smaller than the typical value of BN-G-BN (up to 68000 $cm^2/V{\cdot}s$ at $T = 1.5$ K).

Next, we will focus on the quantum transport performance under a magnetic field applied perpendicular to the graphene plane. Figures 1(e) and 1(f) show the Hall resistance (R_{xy}) mapping as a function of V_g and the magnetic field (B) measured at 1.5 K for G-LAO-STO and BN-G-BN, respectively. It is clear that for G-LAO-STO, a much smaller operating gate voltage is needed, due to the much larger gate capacitance of the ultra-thin LAO layer. Well-defined quantized Hall resistance plateaus can be observed even

under B below 2 T in both the devices, consistent with their relatively high carrier mobilities. However, the $\upsilon = \pm 2$ Hall plateaus (white regions) in G-LAO-STO cover much larger proportions of the parameter space along both axes than those in BN-G-BN. Especially, a wide $\upsilon = -2$ Hall plateau extending from ∼2 T to a maximum available field of 9 T can be obtained at certain V_g. This characteristic can also be observed in the simultaneously obtained mapping of the longitudinal resistance (R_{xx}) (Fig. S2), manifesting as the wide regions of zero R_{xx} corresponding to the $\upsilon = \pm 2$ Hall plateaus. Although there has been a lot of research devoted to the quantum transport performance of graphene, the observation of such a wide quantum Hall plateau thus far has been achieved in limited systems, e.g., epitaxial graphene on SiC,[25,26] and InSe covered graphene.[27]

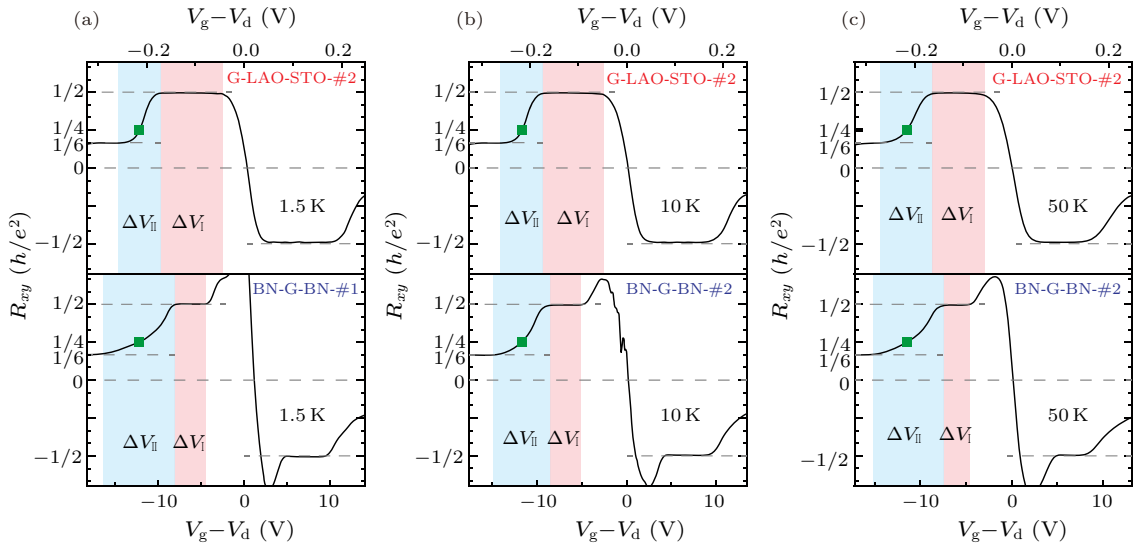

Fig. 2. (a) R_{xy} vs $(V_g - V_d)$ curves measured at $B = 9$ T and $T = 1.5$ K for G-LAO-STO-2 and BN-G-BN-1. [(b),(c)] R_{xy} vs $(V_g - V_d)$ curves under 9 T for G-LAO-STO-2 and BN-G-BN-2 obtained at 10 K and 50 K, respectively.

If we plot the R_{xy}–V_g curves taken under a quantizing magnetic field, more details can be obtained. Figure 2(a) respectively shows the typical results of G-LAO-STO-2 and BN-G-BN-1 measured at $T = 1.5$ K and $B = 9$ T. Since different gate voltages are used, these two curves are aligned in x-axis according to the position of $R_{xy} = h/4e^2$ (green squares) and the Dirac point of graphene. It is evident that in G-LAO-STO the relative width of the $\upsilon = \pm 2$ Hall plateaus along V_g are much larger than those in BN-G-BN. To better demonstrate it, we define the regions corresponding to the $\upsilon = -2$ Hall plateau and the $N = -1$ LL as region I (red region) and region II (blue region), respectively. The relative width of the Hall plateau can thus be represented as $w = \Delta V_I / \Delta V_{II}$, where ΔV_I and ΔV_{II} are the gate-voltage ranges of the two regions, respectively. From other comparison results shown in Figs. 2(b) and 2(c), a larger w can be commonly achieved in G-LAO-STO. Note that these wide Hall plateaus presented in Fig. 2 do not arise from the gate hysteresis, since negligible hysteresis behavior in response to the reversal of the sweeping direction is seen (Figs. S1(b)–S1(e)). This observation together with the wide Hall plateau along B (Fig. 1(e)) indicates the substantially enlarged operational parameter space of the QHE in the present G-LAO-STO device.

To unveil the underlying mechanism for the obtained wide Hall plateaus in G-LAO-STO, we first develop a simple band diagram model[12,13,20] to account for the tuning effect of V_g, as schematically illustrated in Fig. 3(a). Note that applying V_g not only induces charge carriers in graphene, but also leads to the Fermi energy shift for both graphene and LAO/STO interface. Nevertheless, since the density of states in the LAO/STO interface (on the order of 10^{15} eV^{-1} cm^{-2})[28,29] is much larger than that in the graphene layer (on the order of 10^{13} eV^{-1} cm^{-2}),[20,30] the Fermi energy shift of LAO/STO is negligible. Thus the effect of V_g on the carrier density modulation can be described using the equation

$$e(V_g - V_d) = E_F - \frac{e^2}{C_{LAO}} n, \tag{1}$$

where E_F is the Fermi energy of graphene, and C_{LAO} is the geometrical capacitance of the LAO layer. In our previous work,[19] the validity of this equation has been demonstrated by satisfactory fits of the nonlinear V_g dependence of n determined from the low-field Hall data (< 0.5 T). Moreover, the extracted C_{LAO} is more than two orders larger than that of conventionally used 300-nm-thick SiO_2, benefiting from the ultra-small thickness and relatively high dielectric constant of the LAO layer (20–25).[31]

Considering graphene under a quantizing magnetic field, carriers are ranged in LLs (the right panel in Fig. 3(a)). In this case, Eq. (1) remains valid, but varies in detailed form based on the location of the Fermi level (Fig. 3(b)). If ignoring the impact of LL

broadening, a semi-quantitative estimation of the dependence of carrier density can be readily figured out. When the Fermi level is inside the gap between the neighboring Nth and $(N+1)$th LLs (e.g., region I in Fig. 3(b)), the Nth LL is fully filled and the carrier density can be expressed as $n = -(4N+2)eB/h$. When the Fermi level is in the Nth LL (e.g., region Ⅱ), the Fermi energy equals the energy of the Nth LL, i.e., $E_{\rm F} = E_{\rm N} = {\rm sgn}(N)v_{\rm F}\sqrt{2e\hbar B|N|}$. Based on Eq. (1) by involving the above expressions (see Note 1 in the supplementary material for details), the main characteristics of the experimental $(V_{\rm g}-V_{\rm d})$-dependent n curve can be well reproduced (Fig. 3(d)). The parameters used here are $C_{\rm LAO} = 1.59\,\mu{\rm F/cm^2}$ and $v_{\rm F} = 1.17\times10^6\,{\rm m/s}$, according to the values obtained in our previous work.[19] In region I the dominant variable term is the first term on the right side of Eq. (1) corresponding to the quantum Hall plateaus, such that $\Delta V_{\rm I} \sim (E_0 - E_{-1})/e = v_{\rm F}(2\hbar B/e)^{1/2}$. In region Ⅱ, the second term on the right side dominates the variation, such that $\Delta V_{\rm Ⅱ} \sim (1/C_{\rm LAO})4e^2B/h$. Therefore, in the n vs $(V_{\rm g}-V_{\rm d})$ curve, $w = \Delta V_{\rm I}/\Delta V_{\rm Ⅱ} \sim C_{\rm LAO}v_{\rm F}h^{3/2}/(4\pi^{1/2}e^{5/2}B^{1/2}) \propto C_{\rm LAO}$, which should be quite high due to the ultra-large value of $C_{\rm LAO}$. As a result, quantum Hall plateaus over a large proportion of the gate-voltage range are achieved in the present G-LAO-STO device.

By utilizing the same model, the typical characteristics of the quantum Hall plateau along the magnetic field could also be reproduced to some extent. It is well known that the intervals of LLs enhance with increasing B (Fig. 3(c)), the variation of the relative position between Fermi level and LLs leads to oscillations of the carrier density.[12] Here we take the R_{xy} vs B data obtained at $V_{\rm g}-V_{\rm d} = -0.048\,{\rm V}$ as an example. According to $v = -nh/eB$ and $R_{xy} = h/ve^2$, the experimental n vs B data can be obtained, and the result is shown in Fig. 3(e). On the other hand, according to Eqs. (S1) and (S2) in the supplementary material, the B dependence of n profiles can be described as follows: in situations like region I (Eq. (S1)), n increases linearly with B, while in situations like region Ⅱ (Eq. (S2)), n decreases linearly with $B^{1/2}$. Thus the n vs B curve can also be simulated by further computing the lower/upper critical magnetic field of the quantum Hall plateau. For instance, the lower critical field ($B_{\rm IL}$) and upper critical field ($B_{\rm IU}$) of the $v=-2$ Hall plateau (region I) can be represented as $B_{\rm IL} = \left(\frac{-2\pi ehD}{\sqrt{\pi eh^3v_{\rm F}^2C_{\rm LAO}^2-8\pi^2e^4hD}+\sqrt{\pi eh^3v_{\rm F}^2C_{\rm LAO}^2}}\right)^2$ and $B_{\rm IU} = -\frac{h}{2e^2}D$, respectively (see Note 2 in the supplementary material for details), where $D = (V_{\rm g}-V_{\rm d})C_{\rm LAO}$ (<0) is the electric displacement. As depicted in Fig. 3(e), in region I the simulation result agrees well with the experimental data. Note that $B_{\rm IU}$ is constant for a fixed D, while the obtained $B_{\rm IL}$ should be quite small due to the ultra-large value of $C_{\rm LAO}$. Thus, the large width of the $v=-2$ Hall plateau along B, i.e., $B_{\rm IU}-B_{\rm IL}$, can also be reasonably explained.

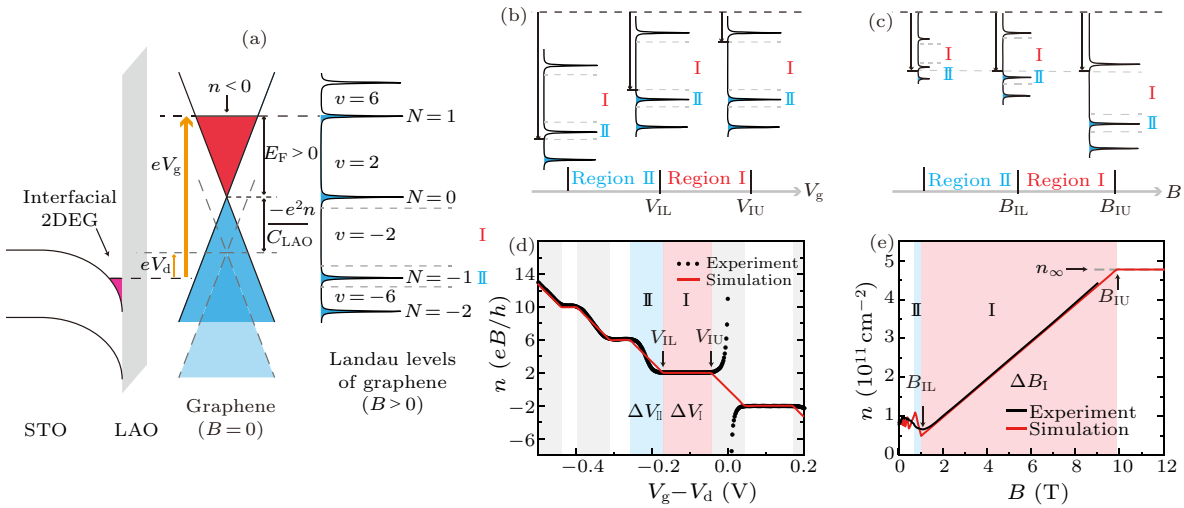

Fig. 3. (a) Schematic band diagram across the G-LAO-STO hybrid structure. The middle and right panels show the band diagram of graphene under $B=0$ (Dirac cone form) and quantizing B (LL form), respectively. The dashed diagram in the middle panel illustrates a case where the Fermi level of graphene is at the Dirac point. [(b),(c)] Evolution of the Fermi level and the LLs of graphene with varying $V_{\rm g}$ and B, respectively. (d) $(V_{\rm g}-V_{\rm d})$-dependent n under 9 T and the corresponding simulation result. (e) B-dependent n with $V_{\rm g}-V_{\rm d} = -0.048\,{\rm V}$ and the corresponding simulation result. The experimental data of n in (d) and (e) are calculated via $n = -veB/h = -B/(eR_{xy})$ from the R_{xy} data, while the measurements are conducted at 1.5 K in G-LAO-STO-2.

Here we would like to address that the above analyses of the QHE are applicable in a wide variety of cases. To demonstrate it, n as a function of $(V_{\rm g}-V_{\rm d})$ under different B were simulated using Eq. (1) (dashed lines in Fig. 4(a)), and then compared with the experimental data (solid lines). It is evident that the main characteristics are well reproduced, especially for plateaus at small filling factors. With decreasing B,

the widths of the Hall plateaus decrease accordingly due to the reduction of energy gaps between adjacent LLs. In addition, the value of V_g at which the LL is half-filled ($\upsilon = 4N$), corresponding to the position of R_{xx} peak, can be estimated by solving Eq. (1) with $E_F = E_N$ and $n = -4NeB/h$.[13,32] As can be clearly seen from Fig. 4(b), the simulated curves agree well with the experimental data, further demonstrating the validity of our model.

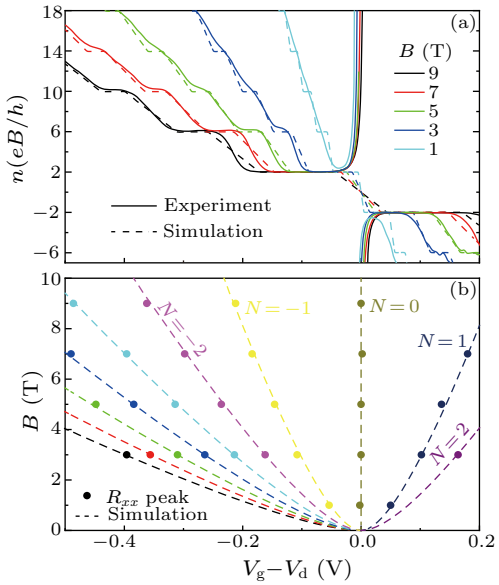

Fig. 4. (a) $(V_g - V_d)$-dependent n under different B and the corresponding simulation results. (b) The values of V_g and B corresponding to half-fillings of graphene LLs. The circular points represent the peak positions in R_{xx} vs $(V_g - V_d)$ data (Fig. S3) obtained under different B, while the dashed lines represent the simulation results. The experimental data in (a) and (b) are obtained at 1.5 K in G-LAO-STO-2.

Unlike the case of epitaxial graphene on SiC, in which the realization of giant quantum Hall plateaus was mainly attributed to the charge transfer between graphene and interface states in SiC,[12,13] in the present G-LAO-STO system the ultra-large gate capacitance of the LAO layer plays a key role. Normally, interface states will accommodate a portion of charges induced by the gate-voltage while tuning the Fermi level of graphene.[13] As a consequence, the voltage range corresponding to the quantum Hall plateau, e.g., ΔV_I, would be significantly enlarged when the effect of interface states dominates the widening of the Hall plateau (see Note 3 and Fig. S4 in the supplementary material for details). However, in G-LAO-STO the experimental ΔV_I agrees well with the value simulated without involving interface states (Figs. 3(d) and S4(c)), revealing the negligible effect of interface states on the widening of the quantum Hall plateau.

In summary, quantum Hall plateaus over a wide range of the magnetic field and gate-voltage are successfully realized in G-LAO-STO, a hybrid device consisting of graphene and LAO/STO heterostructure. Note that in terms of the localization model, the lower-quality samples may also present wide Hall plateaus.[33,34] However, the low carrier mobility results in a relatively large critical magnetic field where the quantum Hall plateau emerges, and high accuracy of the quantum Hall resistance is also hard to achieve. In our G-LAO-STO devices, the carrier mobility of graphene is substantially enhanced as compared with previous pristine graphene on SiO_2, and the obtained wide Hall plateaus originate from the ultra-large gate capacitance of the LAO layer. The good sample quality, together with high tunability, make G-LAO-STO an ideal candidate to obtain quantized Hall resistance with high precision under modest conditions. Such a universal approach utilizing a large-capacitance dielectric layer can also be readily extended to more generalized 2D material systems for optimizing the quantum transport performance.[35,36]

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Supplementary Materials: Giant-capacitance-induced wide quantum Hall plateaus in graphene on $LaAlO_3/SrTiO_3$ heterostructures

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Supplementary notes:

Note 1: Detail forms of the potential equilibrium equation (Eq. (1) in the main text) under a quantizing magnetic field.

As mentioned in the main text, Eq. (1) remains valid while under a quantizing magnetic field, but varies in detail form depending on the location of the Fermi level (Fig. 3(b)).

A. When the Fermi level is inside the gap between the neighboring Nth and (N+1)th LLs of graphene (e.g. region I in Fig. 3(b)), the Nth LL is fully filled, $E_{\mathrm{N}} \leqslant E_{\mathrm{F}} \leqslant E_{\mathrm{N+1}}$, where Eq. (1) can be rewritten as:

$$e\left(V_{\mathrm{g}} - V_{\mathrm{d}}\right) = E_{\mathrm{F}} - \frac{e^2}{C_{\mathrm{LAO}}}\frac{-(4N+2)eB}{h} \qquad \text{(S1)}$$

B. When the Fermi level is in the Nth LL (e.g. region II), the Nth LL is partly filled, $-(4N+2)eB/h \leq n \leq -(4N-2)eB/h$, where Eq. (1) can be rewritten as:

$$e\left(V_{\mathrm{g}}-V_{\mathrm{d}}\right)=sgn(N)v_{\mathrm{F}}\sqrt{2e\hbar B|N|}-\frac{e^{2}}{C_{\mathrm{LAO}}}n \tag{S2}$$

Note 2: Determination of the upper/lower critical magnetic field of the quantum Hall plateau

Taking ν=-2 Hall plateau as an example, the upper critical field B_{IU} corresponding to the lower edge of N=0 LL (right plane in Fig. 3(c)) fulfills the following equation:

$$e\left(V_{\mathrm{g}}-V_{\mathrm{d}}\right)=-\frac{e^{2}}{C_{\mathrm{LAO}}}\frac{2eB_{\mathrm{IU}}}{h} \tag{S3}$$

That is,

$$B_{\mathrm{IU}}=-\frac{h}{2e^{2}}\left(V_{\mathrm{g}}-V_{\mathrm{d}}\right)C_{\mathrm{LAO}}=-\frac{h}{2e^{2}}D=\frac{h}{2e}n_{\infty} \tag{S4}$$

Here n_{∞} represents the final carrier density of graphene (as indicated in Fig. 3(e)), and D = (V_{g}-V_{d})C_{LAO} is the electric displacement.

The lower critical field B_{IL} corresponding to the upper edge of N=-1 LL (middle plane in Fig. 3(c)) fulfills the following equation:

$$e\left(V_{\mathrm{g}}-V_{\mathrm{d}}\right)=-v_{\mathrm{F}}\sqrt{2e\hbar B_{\mathrm{IL}}}-\frac{e^{2}}{C_{\mathrm{LAO}}}\frac{2eB_{\mathrm{IL}}}{h} \tag{S5}$$

That is,

$$B_{\mathrm{IL}}=\left[\frac{hC_{\mathrm{LAO}}}{4e^{3}}\left(\sqrt{2e\hbar{v_{\mathrm{F}}}^{2}+\frac{-8e^{4}(V_{\mathrm{g}}-V_{\mathrm{d}})}{hC_{\mathrm{LAO}}}}-\sqrt{2e\hbar{v_{\mathrm{F}}}^{2}}\right)\right]^{2}=\left(\frac{-2\pi ehD}{\sqrt{\pi eh^{3}{v_{\mathrm{F}}}^{2}{C_{\mathrm{LAO}}}^{2}-8\pi^{2}e^{4}hD}+\sqrt{\pi eh^{3}{v_{\mathrm{F}}}^{2}{C_{\mathrm{LAO}}}^{2}}}\right)^{2} \tag{S6}$$

Note 3: Analysis of the effect of interface states on the quantum Hall plateau

When there are interface states with constant density of states γ locating between graphene and the gate electrode, both the Fermi levels of the interface states and graphene will vary while applying a gate-voltage. That is, a portion of charges induced by the gate-voltage will be accommodated by the interface states, which acts as an interfacial trap capacitance.[1] Figures S4(a,b) show the schematic

band diagram and the corresponding equivalent capacitive circuit, where $C_Q = e^2(dn/dE_F)$ represents the equivalent quantum capacitance of graphene; $C_{it} = e^2\gamma$ represents the interfacial trap capacitance; C_1 represents the capacitance between the gate electrode and the interface states, which normally approaches the value of gate capacitance; C_2 represents the capacitance between the interface states and graphene, which normally is quite large.

According to the principle of charge conservation, the equilibrium between the electrochemical potentials of the interface states and graphene can be expressed as:

$$E_F - \frac{e^2}{C_2}n = -\frac{e^2}{C_{it}}n_{it} \tag{S7}$$

Here n_{it} represents the change of the carrier density of the interface states.

Analogously, the equilibrium between the electrochemical potentials of the interface states and the gate electrode can be expressed as:

$$-\frac{e^2}{C_{it}}n_{it} - \frac{e^2}{C_1}(n + n_{it}) = e(V_g - V_d) \tag{S8}$$

By combining Eqs. (S7) and (S8), we can obtain the following equation:

$$e(V_g - V_d) = \frac{C_1+C_{it}}{C_1}E_F - \frac{e^2}{(\frac{C_1C_2}{C_1+C_2+C_{it}})}n \tag{S9}$$

This equation is quite similar to Eq. (1), while the only differences are the coefficients of the terms on the right side. Following the analysis procedures analogous to those described above, the dependence of n on V_g/B after involving the effect of the interface states can also be obtained. Especially, ΔV_I can be depicted as $\Delta V_I \sim [(C_1+C_{it})/C_1]\cdot v_F(2\hbar B/e)^{1/2}$. Compared to the calculated value without interface states, i.e. $v_F(2\hbar B/e)^{1/2}$, ΔV_I would be enlarged by $(C_1+C_{it})/C_1$ times. However, as shown in Figs. 3(d) and S4(c), the experimental obtained ΔV_I are nearly identical with $v_F(2\hbar B/e)^{1/2}$,

implying the negligible effect of interface states on the widening of the quantum Hall plateau in G-LAO-STO.

Supplementary figures:

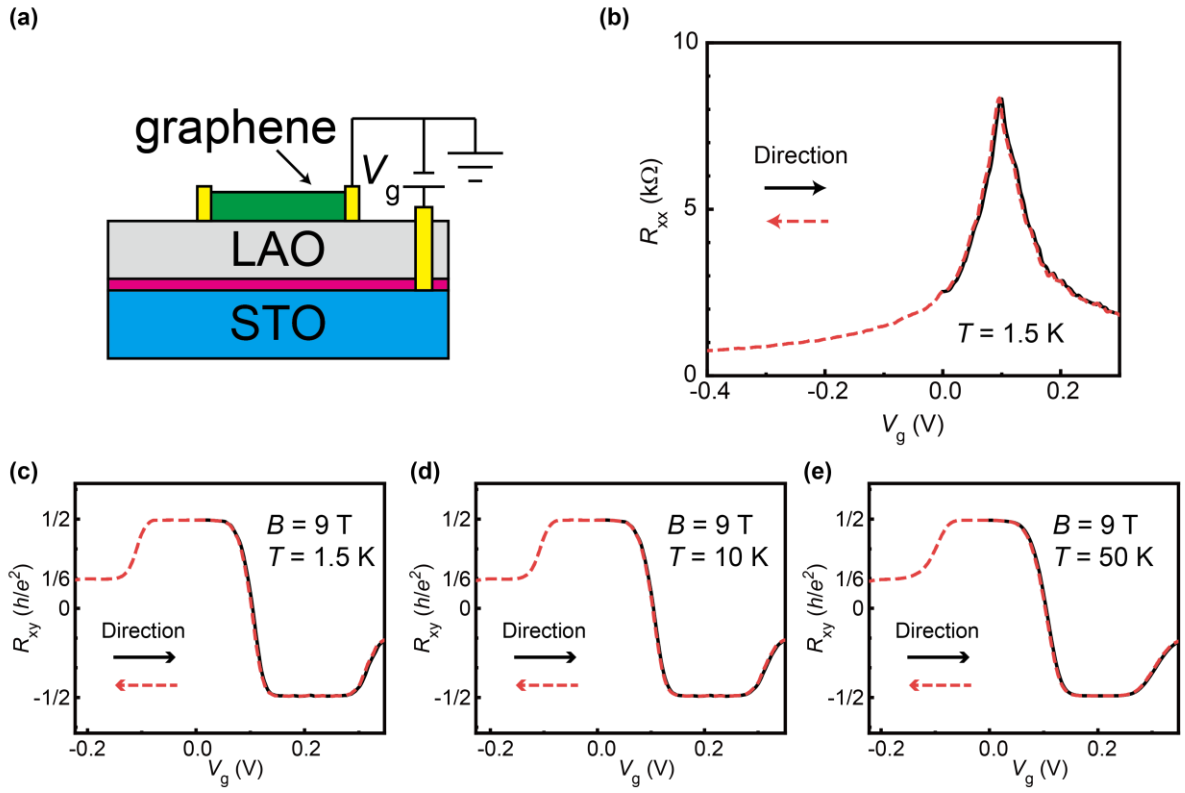

Fig. S1. (a) Schematic illustration of the G-LAO-STO device, in which the LAO layer and the conducting LAO/STO interface are utilized as the dielectric layer and the gate electrode, respectively. (b) R_{xx} vs V_g curves for G-LAO-STO-#2 obtained at 1.5 K under zero magnetic field. (c-e) R_{xy} vs V_g curves for G-LAO-STO-#2 under 9 T magnetic field obtained at 1.5 K, 10 K and 50 K, respectively. The arrows indicate the directions of V_g sweeping.

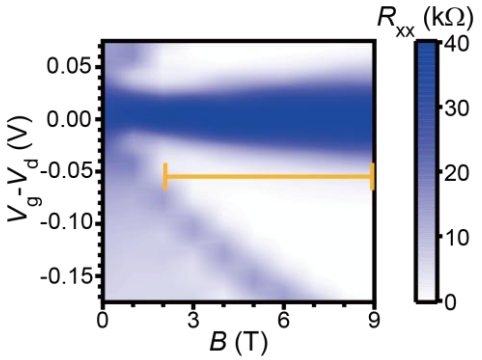

Fig. S2. R_{xx} as a function of B and (V_g–V_d) measured at 1.5 K for G-LAO-STO-#1. V_d is the gate-voltage corresponding to the Dirac point of graphene. These data were taken simultaneously with Fig. 1(e) in the main text.

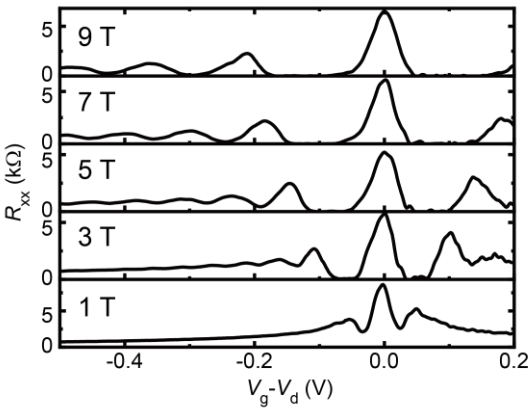

Fig. S3. (V_g–V_d) dependent R_{xx} at 1.5 K under different magnetic fields in G-LAO-STO-#2.

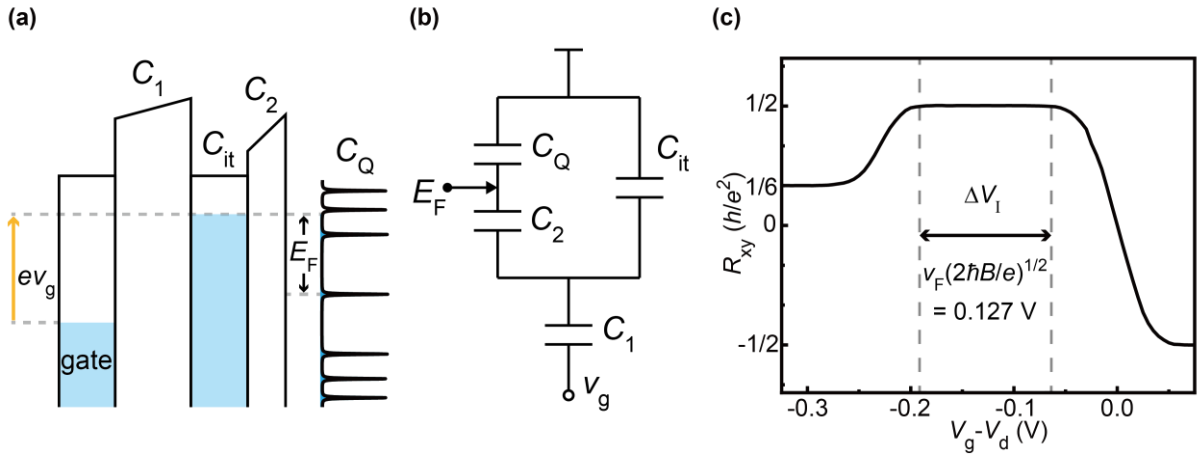

Fig. S4. (a) The schematic band diagram of the G-LAO-STO while involving the effect of interface states. (b) Equivalent capacitive circuit of (a). (c) (V_g–V_d) dependent R_{xy} under measured at B=9 T and T=1.5 K for G-LAO-STO-#1. The dashed range represents the simulated gate-voltage range of region I (ΔV_I) without interface states.

Supplementary references:

[1] Takase K, Tanabe S, Sasaki S, Hibino H and Muraki K 2012 *Phys. Rev. B* **86** 165435