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Ultrathin Al Oxide Seed Layer for Atomic Layer Deposition of High-κ Al_2O_3 Dielectrics on Graphene

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Due to the lack of surface dangling bonds in graphene, the direct growth of high-κ films via atomic layer deposition (ALD) technique often produces the dielectrics with a poor quality, which hinders its integration in modern semiconductor industry. Previous pretreatment approaches, such as chemical functionalization with ozone and plasma treatments, would inevitably degrade the quality of the underlying graphene. Here, we tackled this problem by utilizing an effective and convenient physical method. In detail, the graphene surface was pretreated with the deposition of thermally evaporated ultrathin Al metal layer prior to the Al_2O_3 growth by ALD. Then the device was placed in a drying oven for 30 min to be naturally oxidized as a seed layer. With the assistance of an Al oxide seed layer, pinhole-free Al_2O_3 dielectrics growth on graphene was achieved. No detective defects or disorders were introduced into graphene by Raman characterization. Moreover, our fabricated graphene top-gated field effect transistor exhibited high mobility ($\sim$6200 $cm^2V^{-1}s^{-1}$) and high transconductance ($\sim$117 μS). Thin dielectrics demonstrated a relative permittivity of 6.5 over a large area and a leakage current less than 1.6 pA/μm^2. These results indicate that Al oxide functionalization is a promising pathway to achieve scaled gate dielectrics on graphene with high performance.

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Graphene becomes an interesting candidate as an alternative material for post-silicon electronics since its intriguing electronic, optical and mechanical properties.[1–3] However, until now, the majority of the efforts have been focused on the integration of graphene devices in the back-gated geometry due to the difficulty of compact and conformal top-gated dielectric deposition directly onto the two-dimensional (2D) channel for the realization of high-performance top-gated field effect transistors (FETs).[4–6] To realize the practical application of graphene in integrated circuits (ICs), top-gated graphene FETs with high-κ dielectric is necessary. Firstly, compared with a traditional 300 nm SiO_2 back-gate dielectric layer, the top-gate dielectric layers are much thinner and have higher values of dielectric constant κ, thus permitting further device scaling and lower operation voltage. Secondly, back-gated FETs are not compatible with IC technology as it cannot individually tune each device like a top gate. Additionally, top-gated configurations are essential to suppress coulomb scattering in graphene channels with the enhanced gate coupling, carrier mobility and saturated current.[7,8]

As the mainstream approach to prepare high-κ dielectric layer in modern semiconductor fabrication technology, atomic layer deposition (ALD) can yield a high-quality dielectric due to its precise thickness controllability, excellent surface conformal coverage, and low deposition temperatures.[9,10] Disappointedly, conformal deposition of dielectrics on graphene remains challenging since there are not sufficient dangling bonds or nucleation sites on the 2D channel for the initiation of uniform dielectric deposition via this standard industrial technique.[1,11–13] The chemically inert nature coupled with the hydrophobicity leads to the non-conformal growth of oxide layer on graphene via ALD, which greatly restricts their industrial applications.[1,14] To overcome the chemical inertness of such 2D materials for growth of uniform high-κ films, various surface treatments have been developed prior to ALD growth, such as chemical functionalization with ozone,[12,13,15] plasma treatments[16,17] and polymer coatings.[18–20] These methods not only increase the technical complexity, but also degrade the quality of the underlying graphene and reduce the overall gate capacitance. In this regard, interface or dielectric engineering is an important step towards the practical implementation of graphene devices with the optimized performance.

In this letter, we propose an effective and convenient method to grow high-quality Al_2O_3 dielectrics on graphene. Here, we pretreated graphene surface with the deposition of thermally evaporated ultrathin Al metal layer prior to the Al_2O_3 growth by ALD. Then the device was placed in a drying oven for 30 min to be naturally oxidized as a seed layer.

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After that, the top-gated graphene FET was fabricated by a standard micro-nano fabrication process. There are three advantages of this functionalization method: (1) Al oxide can be used as a seed layer to provide the nucleation sites on the surface of graphene, which could assist the chemisorption of the precursors. (2) Thermal evaporation of Al onto graphene surface is a physical process in high vacuum.[21] Therefore, no obvious structural damage or defects emerge in graphene compared with other chemical methods, such as ultraviolet ozone or plasma pretreatment.[12,13,15–17] (3) After the thermal evaporation of Al, this ultra-thin metal layer will be rapidly oxidized to form amorphous Al_2O_3, thus the capacitance will not be significantly reduced like polymer coating pretreatment.[18–20] Our experimental results confirm the validity of this method. A continuous and dense Al_2O_3 thin film is formed and no D peak appears in graphene during the whole process. Additionally, our fabricated graphene top-gated device exhibits high mobility ($\sim$6200 $cm^2V^{-1}s^{-1}$) and high transconductance ($\sim$117 μS).

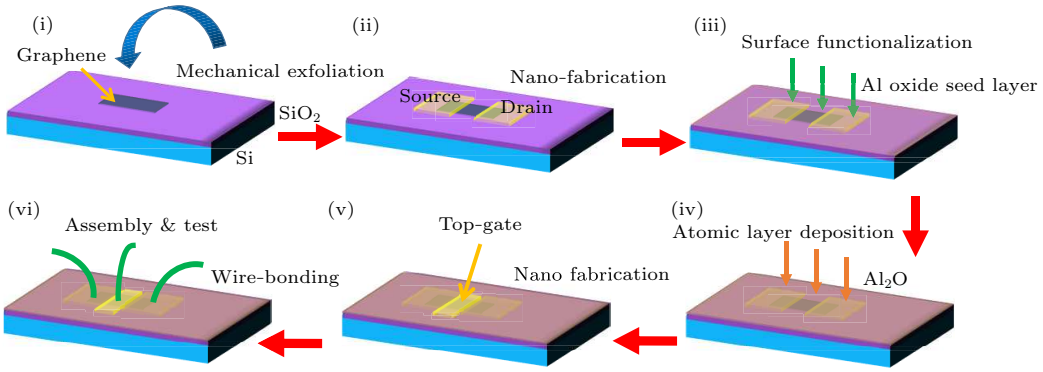

Fig. 1. The fabrication process of high-performance top-gated graphene FET with the assistance of Al oxide seed layer.

Figure 1 illustrates the fabrication process of top-gated graphene FET with the assistance of an Al oxide seed layer. (i) Firstly, scotch tape was used to mechanically exfoliate graphene flakes from bulk graphene crystals (Smart Elements). The exfoliated graphene flakes were then quickly transferred onto a degenerately p-type doped silicon substrate with 300 nm SiO_2. (ii) Next, the source and drain contacts were patterned using e-beam lithography (EHT: 10 kV, aperture size: 30 μm, beam current: 217.1 pA), and 10 nm Ti/50 nm Au were deposited using thermal evaporation (vacuum: 1×10^{-5} Pa, evaporation rate: Ti 0.5 Å/s; Au 1.5 Å/s). (iii) After the lift-off process, the device was transferred again to the thermal evaporator vacuum chamber to deposit 2 nm Al nucleation layer (vacuum: 1×10^{-5} Pa, evaporation rate: 0.3 Å/s). The Al nucleation layer was completely oxidized after the device was placed in a drying oven for 30 min.[22] (iv) Subsequently, high-κ Al_2O_3 was integrated with graphene FET by ALD growth. Here, the dielectric layer was carried out with successive cycles of trimethylaluminum (TMA) and H_2O precursors, with an nitrogen (N_2) carrier gas (99.9997%, Airgas) at a flow rate of 40 sccm, 0.015 s pulse + 10 s N_2 purge time for TMA, 0.015 s pulse + 10 s N_2 purge time for H_2O at a substrate temperature of 150℃. The ALD growth were performed in an argon-filled glovebox with an O_2 and H_2O concentration less than 1 p.p.m. (parts per million). (v) After Al_2O_3 deposition, a top-gate electrode (5 nm Ti/50 nm Au) was completed by the second lithographic patterning and metallization process. (vi) Finally, the as-made device was wire bonded onto a leaded chip carrier for subsequent electrical measurements.

The topography of the samples was characterized via atomic force microscopy (AFM, Bruker company, scanning mode: Semi-contact, scanning frequency: 1.01 Hz) scanning electron microscopy (SEM, Raith E-line plus company) and high-resolution optical microscopy (Nikon Eclipse LV100D). The Raman spectrum was recorded by a Confocal Raman Spectrometer (WiTec 300R, exciting laser wavelength: 532 nm, spot size: 2 μm). All characterizations were conducted in the ambient conditions at room temperature (300 K). The electrical measurements were performed in a custom-designed high-vacuum system (base pressure $\sim$ 10^{-6} mbar) with an Agilent 2912 A source measure unit at room temperature.[21] Noticeably, the back-gate was kept floating to avoid gate-coupling effect in the top-gate measurement.[23]

We first carried out the characterization of the ALD growth quality. For pristine graphene with direct ALD growth, the film quality is very poor, as demonstrated in Fig. 2(a) by the rms surface roughness with the discontinuous "grains" ($R_{rms} \sim 2.8$ nm). With the assistance of a high-resolution SEM image (Fig. 2(b)), we could clearly observe the existence of such "grains", and the average diameter of the "grain" is 30–50 nm. As previously reported, these islands are exactly Al_2O_3 dielectrics grown by ALD.[18,24] Additionally, we do not find a smaller "grain" size when trying a longer idle N_2 purge time (40 s), as shown in Fig. S1, indicating that 10 s is enough and saturated for the Al_2O_3 dielectric layer growth on graphene. Adopting longer idle N_2 purge time may not be significantly helpful for improving the growth quality of

Al_2O_3 dielectric layer.[25] Theoretically, ALD relies on the chemisorption or the rapid reaction of precursor molecules with surface functional groups.[14] Since pristine graphene does not have any dangling bonds or surface groups to react with the precursors, no ALD occurs on the graphene plane. However, in our experiment, the Al_2O_3 could still be deposited on the graphene surface. We propose that during the ALD growth process, graphene would inevitably physically adsorb H_2O precursors and therefore perform some limited growth reactions with TMA precursors (Fig. 2(c)).[24,26] Nevertheless, the film is not dense and uniform, which is far from meeting the requirements of the electrical devices.[4,8] In addition, there appear the quasicontinuous bright lines of Al_2O_3 preferentially grown on the edges of the graphene sheets, suggesting dangling bonds on the edges or possible termination by −OH or other reactive species.[18]

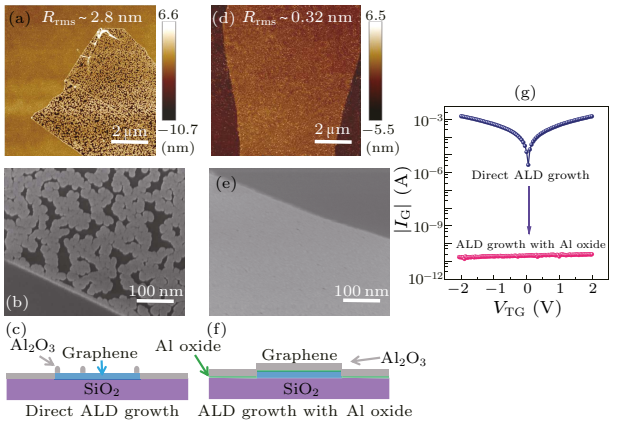

Fig. 2. ALD of 90 cycles Al_2O_3 on pristine graphene and Al oxide seeded graphene. (a) AFM image (b) SEM image and (c) Schematic of Al_2O_3 growth on pristine graphene. Here R_{rms} denotes the rms surface roughness in AFM characterization. (d) AFM image (e) SEM image and (f) Schematic of Al_2O_3 growth on Al oxide seeded graphene (∼ 2 nm thermal evaporated Al). (g) Tunneling (Leakage) current of metal-insulator-semiconductor (MIS) device based on direct ALD growth and Al oxide seeded ALD growth.

In contrast, after the thermal evaporation of 2 nm Al seed layer on the graphene flake, the Al_2O_3 layer was successfully integrated. Complete and uniform packing is evidenced by Al_2O_3 coated over the whole piece of graphene demonstrated by AFM image (Fig. 2(d)) and SEM image (Fig. 2(e)). The mean roughness of the Al_2O_3 film on graphene is reduced to ∼0.32 nm, which is comparable with the Al_2O_3 film on the SiO_2 substrate (∼0.28 nm). Here, as shown in Fig. 2(f), the Al oxide is induced as a seed layer, activating the ALD nucleation sites on the graphene surface. Furthermore, we carried out the experiment of the direct ALD growth on few-layer graphene, as shown in Fig. S2 in the supplementary material. Obviously, the roughness of the sample is still large with R_a ∼ 3.1 nm, indicating the dangling-free property of such a 2D van der Waals material though with a multiple layer.[4,14,27] To understand the dielectric properties of such insulating films, I–V characteristics were compared based on metal-insulator-semiconductor (MIS) devices (shown in Fig. 2(g)).[4,28] When the imposed voltage sweeps from −2 V to +2 V, the tunneling current I_G (leakage current) of the Al oxide seeded grown Al_2O_3 film is controlled less than 1.6 pA/μm^2, and is eight orders of magnitude lower than that of the directly grown Al_2O_3 film. These results indicate this functionalization method is useful for high-quality Al_2O_3 dielectric layer grown on dangling-free graphene.

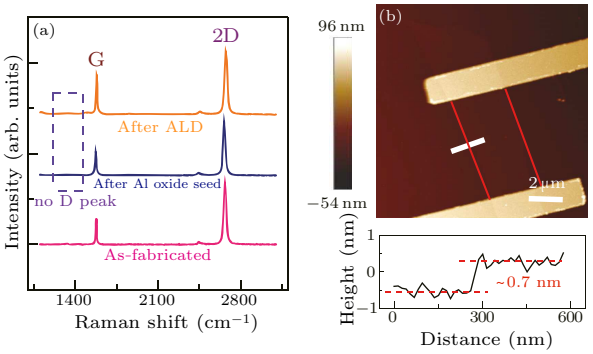

Fig. 3. Characterization of graphene quality in the functionalization process. (a) Raman spectrum of graphene taken immediately after mechanical exfoliation, after Al oxide seeded and after ALD growth. (b) AFM images of the graphene device after ALD growth. The height of the sample is about 0.7 nm.

High-resolution Raman spectroscopy was used to monitor the structural disorder during the functionalization process.[29] As shown in Fig. 3(a), the G peak (1580 cm^{-1}) is significantly lower than the 2D peak (2680 cm^{-1}), which indicates that graphene is monolayer.[30] After Al oxide seeded, the graphene structural defect peak (D peak, around 1350 cm^{-1})[31] still does not appear, showing that this pretreatment approach does not introduce any noticeable lattice damage or bond-disorder into graphene channels. We propose that compared with other chemical methods,[12,13,15–17] thermal evaporation of Al onto graphene surface is a physical process in high vacuum (∼10^{-7} Torr), thus causing limited influence on graphene.[12,13] In the end, after ALD growth (in general, the reaction process of ALD is a mild and slow), the D peak still does not appear though with a relatively high deposition temperature (150℃), meaning that our fabricated Al_2O_3/Al oxide/graphene stack owns a good interface quality. In addition, it can be seen from Fig. 3(b) that the topograph of graphene is very clean and uniform, which shows the formation of a condense Al_2O_3 film on graphene. The thickness of the sample is around 0.7 nm. Although the theoretical thickness of graphene is 0.33 nm, there exists interspace between the graphene and the substrate, therefore the actual measurement may be slightly larger.[29]

Next, the transport characteristics of the device were measured at room temperature in a high vacuum chamber. Figure 4(a) schematically shows our device structure. Top gate voltage and back gate

voltage are imposed through the top dielectric layer (30 nm Al_2O_3) and the back dielectric layer (300 nm SiO_2), respectively. The growth per cycle (GPC) is estimated to be 0.11 nm/cycle. Therefore, thickness of the top dielectric layer is approximately 30 nm.[4,32] Here we systematically compare the electrical properties of graphene FET in two different configurations, to illustrate the powerful regulation based on the Al oxide seeded grown Al_2O_3 dielectric layer. As depicted in Fig. 4(b), the drain-source current (I_{DS}) increases linearly in pace with bias voltage, indicating good ohmic contact between graphene and the electrode.[4,5,33] The aspect ratio (L/W) of the channel is approximately 2.5 as shown in the optical image. Additionally, though with thinner thickness, a lower leakage current is achieved for the Al_2O_3 dielectric (-15 pA at $V_G = -8$ V) than that of the standard 300 nm SiO_2 dielectric (-35 pA at $V_G = -8$ V), which can be attributed to the large bandgap and high film quality of the ALD grown Al_2O_3 layer (Fig. 4(c)).[8] Figures 4(d) and 4(e) demonstrate the transfer characteristics in two different configurations. From the positive sweeping curve of graphene top-gated FET (Fig. 4(d)), when the gate voltage increases from -8 V to -5 V, the current decreases from 143 μA to 82 μA, therefore the normalized I_{ON}/I_{OFF} ratio is evaluated to be 0.6 V^{-1}. In contrast, the normalized I_{ON}/I_{OFF} ratio for graphene in back-gated configuration only reaches 0.03 V^{-1}. The results undoubtedly verify a greater gate regulation ability of the top-gate dielectric layer. Moreover, with continually three times sweeping, the transfer curves overlap very well in top-gated configuration, in contrast with distinct mismatch in back-gated configuration, indicating that the Al_2O_3 dielectric has fewer charge traps than standard SiO_2 dielectric. This can also be reflected from the reduced hysteresis window (back-gated configuration: 30 V; top-gated configuration: 1 V).[34,35]

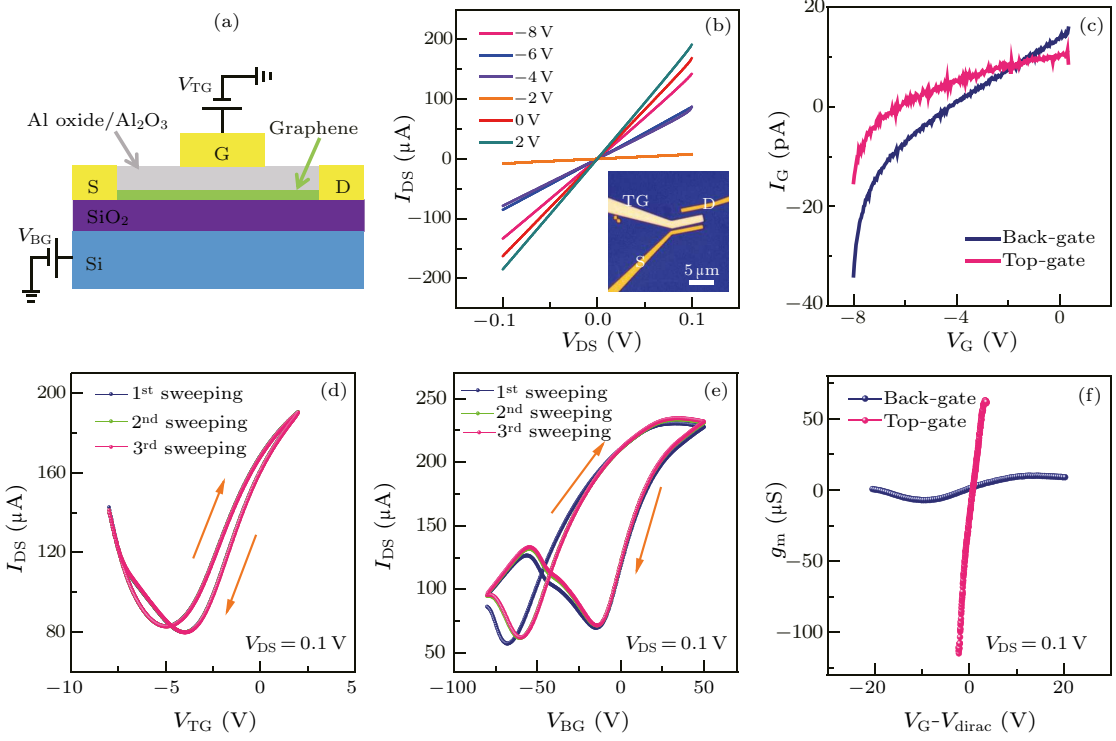

Fig. 4. Electrical properties of top-gated graphene FET with 270 cycles (∼30 nm) Al_2O_3 dielectric layer. (a) Structural schematic of the top-gated device. V_{TG} and V_{BG} represent top-gate voltage (dielectric layer: 30 nm Al_2O_3) and back-gate voltage (dielectric layer: 300 nm SiO_2), respectively. (b) Output characteristics of top-gated graphene FET as a function of top gate voltages (−8–2 V). The inset is the optical image. Here, S, D, V_{TG} represent source electrode, drain electrode and top-gate electrode, respectively. (c) Leakage current in different device configurations. (d) I_{DS}–V_{TG} curve with three times sweeping in top-gated configuration. The hysteresis is clockwise. (e) I_{DS}–V_{BG} curve with three times sweeping in back-gate configuration. (f) Transconductance variation as a function of normalized gate voltage (V_G–V_{Dirac}) curves of graphene FET in two configurations.

Noticeably, the Dirac point of graphene FET usually locates at positive V_G since p-doping by oxygen/water in the ambient atmosphere.[5,6] However, after Al oxide seed pretreatment, an apparent negative shift emerges in transfer curves. We propose that the negative shift of Dirac point originates from the Al induced n-type doping effect during the ALD growth, which is consistent with the literature.[25,36] Additionally, there is an inflection point in hole conduction region in Fig. 4(e), which may be attributed to the poor gating of the SiO_2 (with tremendous oxide trap states) dielectric layer at a large gate bias.[34,35] Here we theoretically discuss the movement of the graphene Fermi surface in two configurations.[37] As shown in Fig. S3 in the supplementary material, the Fermi level of graphene could be more effectively shifted in the

top-gated configuration due to the higher regulation ability by our fabricated high-quality Al_2O_3 dielectric films.[8,37]

Table 1 summarizes some significant parameters (in hole conduction region) of our fabricated graphene FET. Here, the transconductance g_m and carrier mobility μ can be extracted from[4]

$$g_m = \frac{dI_{DS}}{dV_G}\frac{L}{W}, \quad (1)$$

$$\mu = \frac{g_m}{V_{DS}C_i}, \quad (2)$$

where I_{DS} is the drain-source current, V_G is the gate voltage, V_{DS} is the drain-source voltage, L is the channel length, W is the channel width and C_i is the gate capacitance. The extracted hole carrier mobility of graphene FET is $6200\,cm^2V^{-1}s^{-1}$, indicating a good transport performance since the suppression of coulomb scattering in graphene channels.[8] Noticeably, the electron mobility ($7100\,cm^2V^{-1}s^{-1}$) is slightly higher than the hole mobility ($6200\,cm^2V^{-1}s^{-1}$). The better electron conduction mainly comes from the n-type doping effect of the Al oxide seed layer, which facilitates the transport of electron carrier.[25] Additionally, from Fig. 4(f), it can be seen that the maximum transconductance is 117 μS ($V_{TG} = -2.2$ V). As previously reported, there is not too much influence on the graphene carrier mobility in the two configurations since the capacitance only plays a role of regulating induced charges.[23] Accordingly, we assume that graphene retains the same mobility in the top-gated configuration and back-gated configuration. We can conclude:[4,23]

$$\frac{g_m(TG)}{g_m(BG)} = \frac{C_i(TG)}{C_i(BG)}. \quad (3)$$

Compared with the maximum g_m of graphene in back-gated configuration (7.1 μS), the regulation ability of the Al_2O_3 dielectric layer is approximately 16.5 times that of SiO_2 ($C_{TG}/C_{BG} \sim 16.5$). Using the back-gate capacitance value of $C_{BG} = 11\,nF/cm^2$, the top-gate capacitance is estimated to be $C_{TG} = 182\,nF/cm^2$, corresponding to a relative dielectric constant of 6.5 for the Al_2O_3 film. The good gate regulation ability not only has the applications in electronic devices, but also has potential application prospects in optoelectronic devices, such as gated photoconductors or photovoltaic devices.[33,38,39] Furthermore, we compare the electrical performance of this work and previously reported top-gated graphene FET based on other pretreatment methods, as shown in Table S1 in the supplementary material.[24,32,40–45] By utilizing Al oxide as a seed layer prior to ALD growth, the fabricated top-gated graphene FET shows a good performance with high transconductance, high mobility and low leakage current. If the thickness of the dielectric layer is scaling down, dielectric constant and transconductance could be further enhanced.

Table 1. Significant performance parameters of graphene FET in top-gated and back-gated configurations in the hole conduction region.

Parameter configurations	Leakage current	Dirac point	Maximum transconductance	Mobility
Top-gated	−15 pA	−5.7 V	117 μS	$6200\,cm^2V^{-1}s^{-1}$
Back-gated	−35 pA	−59.5 V	7.1 μS	$6200\,cm^2V^{-1}s^{-1}$

In conclusion, we have investigated an Al oxide functionalization method to grow high-quality Al_2O_3 dielectric films on dangling-free graphene. This physical technique, introducing no detective defects or disorders into graphene, can achieve pinhole-free, thin dielectrics over a large area with a relative permittivity of 6.5 and a leakage current less than $1.6\,pA/\mu m^2$. In addition, the fabricated graphene top-gated device exhibits good mobility ($\sim 6200\,cm^2V^{-1}s^{-1}$) and high transconductance (~ 117 μS).

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Supplementary Materials for "Ultrathin Al Oxide Seed Layer for Atomic Layer Deposition of High-κ Al_2O_3 Dielectrics on Graphene"

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The quality of Al_2O_3 dielectric layer is related to the N_2 purge time of TMA or H_2O during ALD. In the growth process, the role of inert N_2 gas is to remove the unreacted precursor molecules and the reaction by-products. Theoretically, if the N_2 purge time is longer, the reaction surface of sample (graphene in our experiment) could be cleaner, therefore the growth quality of dielectric layer would be better[1]. However, in our experiment, we do not find a smaller "grain" size when trying a longer idle N_2 purge time (40 s) during ALD process, shown in Fig. S1. We propose that 10 s is enough and saturated for the Al_2O_3 dielectric layer growth on graphene. Adopting a longer idle N_2 purge time (> 10 s) may not be significantly helpful for improving the growth quality of Al_2O_3 dielectric layer. In addition, longer idle N_2 purge time (30 s or longer) is time-consuming, accordingly, we chose the idle time is 10 s, which was also commonly adopted by previous literature[2].

We have carried out the experiment of the direct ALD growth on few-layer graphene, as shown in Fig. S2. Obviously, the roughness of the sample is still large

with Ra ~ 3.1 nm, indicating the dangling-free property of such 2D van der Waals material though with multiple layer[1, 3, 4]. Here, from the Raman spectrum shown in Fig. R2(b), the G peak intensity is distinctly higher than the 2D peak intensity, which shows the graphene is few-layer rather than monolayer or bi-layer[5].

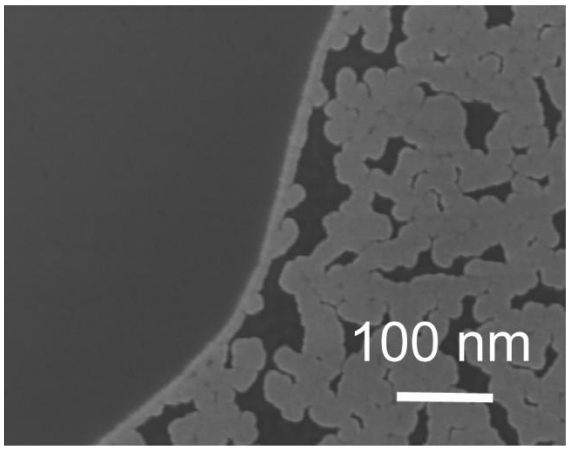

Fig. S1. SEM image of Al_2O_3 growth on pristine graphene with a longer idle N_2 purge time (~ 40s).

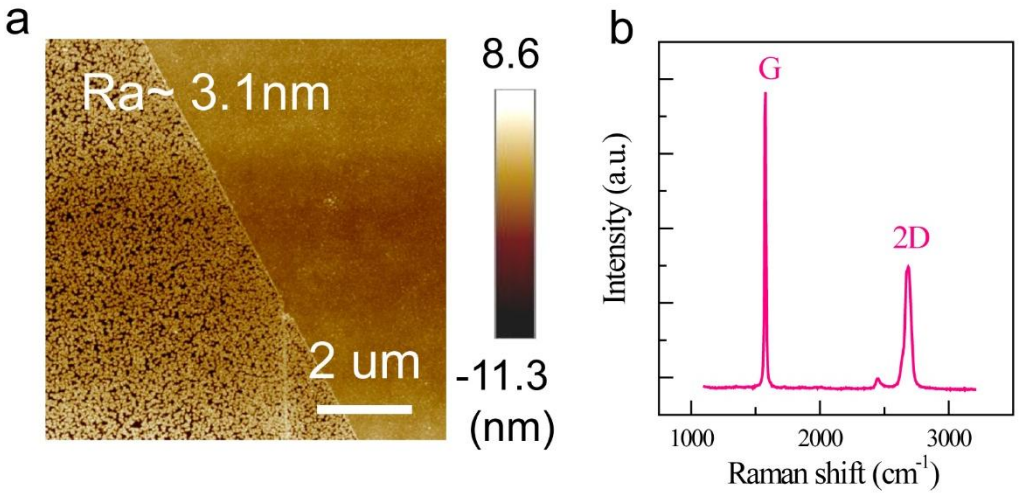

Fig. S2. (a) AFM image of Al_2O_3 growth on pristine few-layer graphene. (b) Raman spectrum of corresponding few-layer graphene used in the experiment.

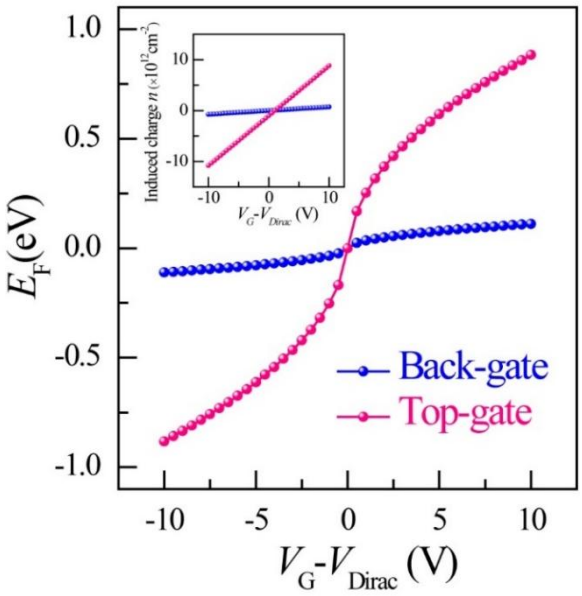

Fig. S3. E_F-V_G curves of graphene FETs in top-gated and back-gated configurations. The inset shows the variation tendency of the induced charge against gate voltage.

Since the electrical properties of graphene FETs are closely related to the graphene Fermi surface, here we theoretically discuss the movement of the Fermi surface in two configurations. The induced charge amount *n* can be expressed as[6]:

$$n = C_i * (V_G - V_{Dirac})/q$$

Where C_i is the capacitance of dielectric layer, V_G is the gate voltage, V_{Dirac} is the Dirac point voltage. For back-gated configuration, the Fermi level (E_F) of graphene as a function of gate voltage can be fitted with the theoretical model[6]:

$$E_F = hv_F\sqrt{(\pi n)}/2\pi q = hv_F\sqrt{\pi(V_{BG} - V_{Dirac})/q}/2\pi q$$

Here, h is Planck constant, v_F is Fermi speed, q is elementary charge. However, for top-gate configuration, the quantum capacitance of graphene cannot be neglected, and thereby the changes of the Fermi level (E_F) of graphene in top-gated configuration can be expressed as[6]:

$$E_F = -1 + \sqrt{1 + 4A(V_{TG} - V_{Dirac})}/2A \qquad A = 4\pi e^3/C_{TG}\,h^2\,v_F^2$$

Obviously, the Fermi level of graphene could be more effectively shifted in top-gated configuration due to the higher regulation ability by our fabricated high quality Al_2O_3 dielectric films[7].

Table S1. Electrical performance of this work and previous reported top-gated graphene FETs based on other pretreatment methods[8-15]. Here, ME represents mechanical exfoliation, CVD represents chemical vapor deposition, g_m represents transconductance, μ represents carrier mobility, κ represents dielectric layer constant and I_G represents leakage current.

Materials	Nucleation promotor	Dielectrics	g_m (μS)	μ ($cm^2V^{-1}s^{-1}$)	κ	I_G ($pA/\mu m^2$)	Ref.
Graphene (ME)	Al oxide seed layer	30 nm Al_2O_3	117	6200	6.5	1.6	This work
Graphene (ME)	Ozone-based ALD	15 nm Al_2O_3	——	5000	8	0.1	[8]
Graphene (ME)	Ozone-based ALD	15 nm Al_2O_3	——	4200	7.8	<100	[9]
Graphene (ME)	Pre-H_2O treatment	135 cycles Al_2O_3	——	——	7.2	1	[10]
Graphene (ME)	Physical vapour deposition	50 nm SiO_2	70	4400	3	~1×10^3	[11]
Graphene (ME)	Polymer dielectric by iCVD	20 nm pV3D3	——	3800	2.9	3×10^4	[12]
Graphene (ME)	NO_2 pretreatment	30 nm Al_2O_3	——	7000	6	——	[13]
Graphene (CVD)	Wetting property control method	25 nm Al_2O_3	20.1	249.5	——	——	[14]
Graphene (CVD)	Plasma-Assisted ALD	9.3 nm Al_2O_3	——	720	90	——	[15]

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