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A CMOS Compatible Si Template with (111) Facets for Direct Epitaxial Growth of Ⅲ–V Materials *

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Ⅲ–V quantum dot (QD) lasers monolithically grown on CMOS-compatible Si substrates are considered as essential components for integrated silicon photonic circuits. However, epitaxial growth of Ⅲ–V materials on Si substrates encounters three obstacles: mismatch defects, antiphase boundaries (APBs), and thermal cracks. We study the evolution of the structures on U-shaped trench-patterned Si (001) substrates with various trench orientations by homoepitaxy and the subsequent heteroepitaxial growth of GaAs film. The results show that the formation of (111)-faceted hollow structures on patterned Si (001) substrates with trenches oriented along [110] direction can effectively reduce the defect density and thermal stress in the GaAs/Si epilayers. The (111)-faceted silicon hollow structure can act as a promising platform for the direct growth of Ⅲ–V materials for silicon based optoelectronic applications.

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Over the past decade, silicon photonics have attracted significant attention owing to its prominent properties, such as low-cost, low-power-consumption, high-speed, high-capacity and integrability with CMOS processing technology.[1,2] However, the lack of stable and reliable Si-based light sources hinders the development of silicon photonics.[3,4] As Ⅲ–V materials exhibit superior optical properties than group Ⅳ materials as efficient light sources, epitaxial growth of Ⅲ–V semiconductors on standard silicon substrates has been considered as a key development trend for realizing the integrable light sources on the silicon-based photonic integrated circuits. Unfortunately, considering large lattice mismatch, different polarities and thermal expansion coefficient difference, the epitaxy of Ⅲ–V materials on Si suffers from several critical issues, including high density threading dislocations (TDs), antiphase boundaries (APBs) and thermal micro-cracks,[5–7] which have been major obstacles preventing the realization of silicon-based on-chip lasers.

Recently, many approaches have been adopted to grow high quality Ⅲ–V layers on Si substrates, such as by utilizing the Si substrates with a small offcut angle to suppress the APBs,[8–10] GaP or Ge intermediate layers on Si (001)[11–13] and V-groove patterned Si substrates.[14–16] Based on the techniques mentioned above, 1300 nm InAs QD lasers on Si substrates have been epitaxially grown and fabricated.[8–12,15,16] However, each of these techniques has their own drawbacks. The offcut Si substrates are not CMOS compatible. The complex and thick intermediate buffer layers make the thermal cracks worse and also increase the cost. Although the selective-area growth on specially patterned substrate by using aspect ratio trapping (ART) method can partially overcome the drawbacks of offcut substrates and thick buffer layers, it still faces the big challenge of thermal mismatch, which induces thermal cracks between Ⅲ–V and Si due to the difference of their thermal expansion coefficients. In the year of 2018, Wei *et al.* reported a specially designed (111)-faceted silicon hollow structure by the homoepitaxial method for growth of high-quality Ⅲ–V materials.[17] The (111)-faceted silicon hollow structures were demonstrated to be effective for avoiding APBs and reducing the threading dislocation density (TDD). Moreover, the hollow structures under V-groove structure can release the built-up thermal stress, thus avoiding thermal cracks on the epitaxial Ⅲ–V layers. In this Letter, we systemically study the formation of (111)-faceted silicon hollow structures on a U-shape patterned Si substrate under different growth conditions. The epitaxial growths of Si and GaAs on two differently oriented U-shaped patterns, along [100] direction and [110] direction, respectively, are compared. By direct epitaxial growth of GaAs buffer layers and InGa(Al)As/GaAs quantum well dislocation filter structures on these specially

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designed Si (001) substrates, high-quality Ⅲ–Ⅴ layers with low TDD ($10^6/cm^2$) in the absence of thermal cracks are achieved in this work for the future Ⅲ–Ⅴ/Si hybrid photonic integrations.

Here epitaxial samples are grown by a dual chamber solid source molecular beam epitaxy (MBE) system. The surface morphologies are clarified by scanning electron microscopy (SEM) and atomic force microscopy (AFM). The x-ray diffraction (XRD), cross-sectional transmission electron microscopy (TEM), and photoluminescence (PL) measurements are conducted to study the crystallographic properties of the samples.

The U-shaped grating structures were patterned on the standard 8-inch Si (001) wafers as follows. The 8-inch wafer was deposited with a SiO_2 layer as hard mask by plasma enhanced chemical vapor deposition (PECVD). Subsequently, the deep ultraviolet (DUV) photolithography with the resolution of 180 nm linewidth was utilized to define the U-shaped grating structures. The grating structures were then transferred onto the Si (001) wafer via dry etching. Lastly, the patterned substrates were treated with oxygen plasma and immersed in the diluted hydrofluoric acid (HF) solution to remove the photoresist and the SiO_2 layer, respectively. Two differently oriented U-shape patterned Si substrates were fabricated as shown in the SEM images of Fig. 1. The U-shaped grating structures along [100] (shown in Figs. 1(a) and 1(b)) and [110] (shown in Figs. 1(c) and 1(d)) directions both have a period of 360 nm with a 140-nm-width ridge and a depth of 500 nm.

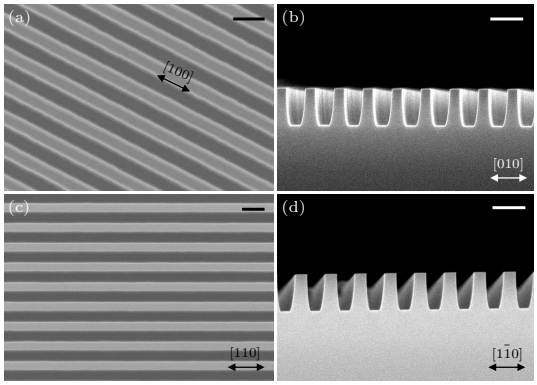

Fig. 1. Top-view SEM images of grating structures on Si (001) substrates, respectively, along [100] direction (a) and [110] direction (c). [(b), (d)] Cross-sectional SEM images of the U-shaped patterns along [100] and [110] directions, respectively. All the scale bars are 400 nm.

Before loading into MBE chamber, the patterned 8-inch wafer was cleaved into 32 mm ×32 mm dies and cleaned under standard RCA process to remove the contaminants, following by HF deoxidation process. After 15 min outgassing at 700℃ in group Ⅳ MBE chamber, the patterned substrates were cooled down to 350℃ for Si homoepitaxial growth. Figure 2 shows the schematic structure of the Si buffer layer grown on patterned Si (001) substrates. Different thicknesses (x in units of nm) of Si homoepitaxial layers were deposited on the patterned Si substrates to study the evolution of the forming structures.

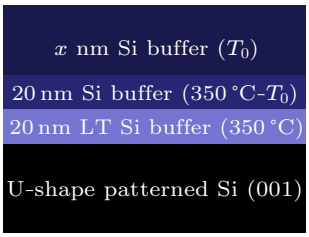

Fig. 2. Schematic structure of Si buffer layer grown on patterned Si (001) substrates. Here x is the thickness of the silicon buffer layer grown at T_0 (growth temperature).

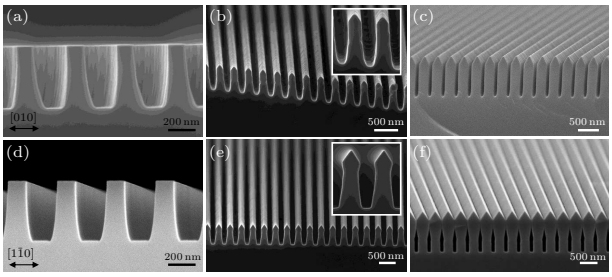

Fig. 3. Cross-sectional SEM images of patterned Si substrates with different thickness of Si homoepitaxial layers: (a) 0 nm, (b) 150 nm and (c) 600 nm (patterns along [100] direction), (d) 0 nm, (e) 150 nm and (f) 600 nm (patterns along [110] direction). Insets: Zoomed-in SEM images of U-shaped patterns long [100] (b) and [110] (e) directions with 150 nm Si buffer layers.

The structural properties of the patterned Si substrates with different thicknesses of Si buffer layers are investigated in the following. In Fig. 2, a Si buffer layer with a total thickness of 150 nm was first deposited on the U-shaped Si substrate along [100] direction, which included a 20-nm-thick low temperature (LT) Si buffer layer at 350℃, a 20-nm-thick Si buffer at the temperature ranging from 350℃ to 550℃ ($T_0 = 550$℃), following by an additional 110-nm-thick high temperature (HT) Si buffer layer at 550℃. The growth rate of the Si buffer layers was fixed at 1 Å /s for all steps. As the cross-sectional SEM image shown in Fig. 3(b), triangular-like structures were achieved on the top of the 140-nm-wide Si ridges along [100] direction, comparing with the original structures shown in Fig. 3(a). The inset in Fig. 3(b) shows the zoomed-in cross-sectional SEM image of the triangular-like structures, which appear to have two (110) facetted surfaces on both sides. By increasing the deposition thickness of silicon buffer to 600 nm, the triangular-like structures remain unchanged and the gaps between ridges shrink correspondingly due to the lateral growth along [010] direction as shown in Fig. 3(c).

An identical experiment was also conducted on the U-shaped Si substrate along [110] direction. As shown in Fig. 3(e), sharp triangular structures consisting of two equivalent {111} facets were formed on the ridges along [110] direction shown in Fig. 3(d), with deposition of 150 nm Si buffer. Interestingly, the (111) faceted top ridges grow fast and leave a neck-shaped

structure. With further deposition up to 600 nm Si, the growing top ridges merge into a continuous film and (111)-faceted Si hollow structures with curvature sidewalls were achieved as shown in Fig. 3(f). In contrast, the sidewalls of ridges grown on [100] oriented patterns are straight (100) planes and hollow structures are not able to be obtained on such patterns. We speculate that this is due to the different surface energies of the (100), (110) and (111) facets. On [110] oriented patterns, the lower surface energy of the {111} facets compared to the (110) side facets drives the fast growth of the top ridges, while on the [100] oriented patterns, the lower surface energy of the (100) sidewall facets compared to the top (110) facets keeps the sidewalls incurvature.

As reported in previous studies,[14,18–21] most of the threading dislocations and APBs between Ⅲ–V and Si substrates are lying and gliding on (111) facets, and they can be controlled and confined at the interfaces by V-grooved structures. Most importantly, the hollow structures can effectively reduce the thermal mismatch between GaAs and Si.[17] Therefore, we conclude that only the homoepitaxial growth on U-shaped grating patterns along [110] direction can function as an excellent defect-trapping and thermal stress releasing template for the growth of high-quality Ⅲ–V materials. In the next, we systematically investigate the Si homoepitaxy under different growth temperatures on the U-shape patterned Si (001) substrates orientated along [110] direction.

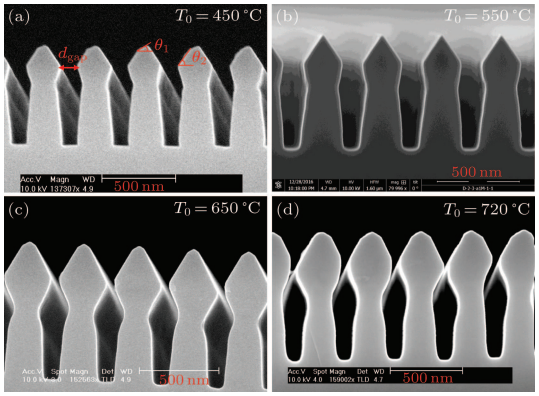

Fig. 4. Cross-sectional SEM images of patterned Si substrates along [110] direction with 250 nm Si buffer layers at different growth temperatures (T_0): (a) 450℃, (b) 550℃, (c) 650℃, and (d) 720℃.

All of the 250-nm-thick silicon buffer layers were grown on four identical samples at different growth temperatures (T_0) of 450℃, 550℃, 650℃, and 720℃ with a same growth rate of 1 Å/s. The structural characterization by cross-sectional SEM for these four samples are shown in Fig. 4. As shown in Fig. 4(a), when the growth temperature T_0 was fixed at 450℃, two stable facets could be observed on the triangular-like structures. The angles (θ_1 and θ_2) of these two facets to (001) plane were measured with the values of approximately 24.6° and 54.9°, which are in line with the adjacent angle of Si (113) facet (25.24°) and the typical angle of Si (111) facet (54.7°), respectively. With increased growth temperature T_0 to 550℃, highly uniform and symmetric rooftops were achieved with only two equivalent Si (111) planes as shown in Fig. 4(b). With further increment in T_0, the triangular rooftops intend to form two metastable (111) planes due to the stronger migration of silicon atoms. As shown Figs. 4(c) and 4(d), bald rooftops can be observed with multiple facets at the temperatures of 650℃ and 720℃. Moreover, with the increase of growth temperature T_0, the lateral growth of the top ridges increases as shown in Fig. 4, which is due to the increased diffusion length of Si adatoms at high growth temperature. Therefore, the size and geometry of the hollow structures are tunable by varying the growth temperature.

These results show the evolution of Si homoepitaxy on U-shape patterned Si (001) substrates under different growth conditions. It is demonstrated that high-quality (111)-faceted Si hollow structures can be achieved at growth temperature of 550℃ with an approximately 600-nm-thick Si buffer layer. By implementing these templates, we discuss the feasibility of epitaxial growth Ⅲ–V photonic structures on Si (001) substrates for silicon photonic integrations in the following part.

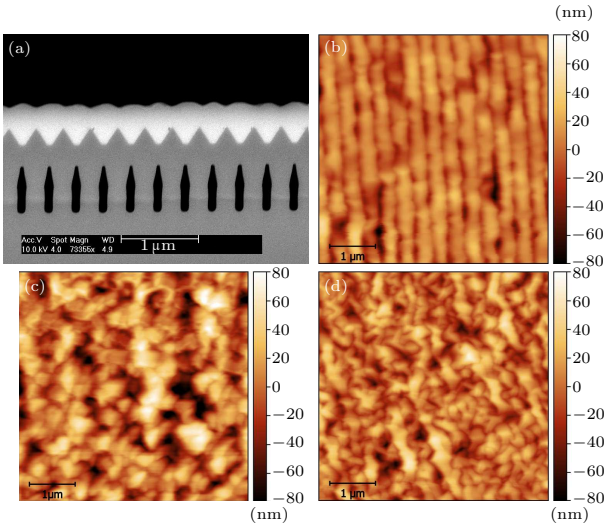

Fig. 5. (a) Cross-sectional SEM image of 400 nm GaAs layers grown on (111)-faceted Si (001) hollow structures. The $5 \times 5\,\mu m^2$ surface AFM images of 400 nm GaAs layers grown on the (111)-faceted Si (001) substrate (b), the patterned Si (001) substrate along [100] direction (c), and the standard Si (001) substrate (d).

The (111)-faceted Si (001) hollow substrates are expected to be one of the most reliable templates for growing high-quality GaAs by trapping the defects at the GaAs/Si interface via geometric reforming. Here the GaAs layers were grown on the (111)-faceted Si (001) hollow substrates by utilizing a two-step growth method, which consisted of a 40-nm-thick GaAs nucleation layer at 350℃ and a 360 nm GaAs buffer layer at 560℃. Figures 5(a) and 5(b) show the cross-sectional SEM image and $5 \times 5\,\mu m^2$ surface AFM image of 400 nm GaAs layers grown on (111)-faceted Si

(001) hollow substrates, respectively. Identical experiments were also carried out on both the patterned Si (001) substrate along [100] direction (Fig. 3(c)) and the standard Si (001) substrate. Figures 5(c) and 5(d) show the $5 \times 5\,\mu m^2$ surface AFM images of 400 nm GaAs layers, respectively, grown on the patterned Si (001) substrate along [100] direction and on the standard Si (001) substrate. By comparing the surface morphologies of GaAs on these three different Si templates, APB-free GaAs layers can be obtained only on the (111)-faceted Si hollow structures. However, due to the deep trenches (approximately 255 nm) of the (111)-faceted Si hollow structures, the surface of GaAs buffer layers exhibits ridge-like morphology along [110] direction as observed in Figs. 5(a) and 5(b). The root-mean-square (rms) roughness of 14.9 nm is measured for the $5 \times 5\,\mu m^2$ region of 400 nm GaAs on the (111)-faceted Si (001) hollow substrate. Note that the ridge-like GaAs surface can be further flattened by depositing additional GaAs/AlGaAs superlattice and InGa(Al)As/GaAs quantum-well dislocation filters.[17,22]

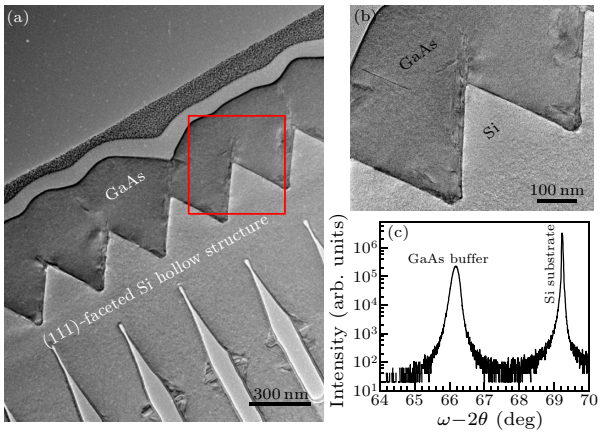

Fig. 6. (a) Cross-sectional bright-field TEM image of 400 nm GaAs on the (111)-faceted Si hollow structures, taken along the [110] axis. (b) Zoomed-in TEM image of the GaAs/Si interface region, which is marked in (a). (c) XRD ω–2θ scan of 400 nm GaAs film on the (111)-faceted Si (001) hollow substrate.

Furthermore, the bright-field cross-sectional TEM characterization was conducted to further investigate the GaAs material quality on (111)-faceted Si hollow structures as shown in Figs. 6(a) and 6(b). Benefitting from the homo-epitaxially formed and high-quality Si (111) planes, the defects are mostly confined at the interface. Limited TDs are observed propagating into the upper region. Moreover, XRD measurement was also carried out to investigate crystallographic quality of the GaAs film. Figure 6(c) shows the ω–2θ spectrum of 400 nm GaAs on the patterned Si (001) substrate. A sharp peak of GaAs buffer with the full width at half maximum (FWHM) of 671.7 arcsec (Si substrate: 132.1 arcsec) was achieved, which indicates a relatively good crystalline quality of the GaAs layer on the (111)-faceted Si hollow substrate.

To flatten the GaAs surface and to lower the TDD on GaAs surface, additional approximately 1600-nm-thick Ⅲ–Ⅴ buffer layers were deposited as shown in Fig. 7(a). The InGaAs/GaAs and InAlAs/GaAs strained layers (SLs) as dislocations filter layers (DFLs) were grown on the GaAs/Si platforms to reduce the TDD to the order of $10^6/cm^2$. Five layers of GaAs/AlGaAs superlattices (SLs) were also deposited to smoothen the GaAs surface. The growth details of Ⅲ–Ⅴ epi-layer can be found in Ref. [17]. Figure 7(b) shows the top-view SEM image of the whole Ⅲ–Ⅴ structure on the (111)-faceted Si (001) hollow substrate. For comparison, the same structure was also grown on the standard Si (001) substrate shown in Figs. 7(c) and 7(d), showing a rough surface full of APBs.

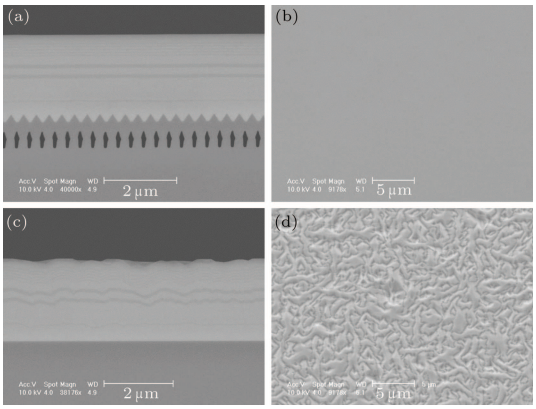

Fig. 7. Cross-sectional SEM images of approximately 2000-nm-thick Ⅲ–Ⅴ layers grown (a) on the (111)-faceted Si (001) hollow substrate and (c) on the standard Si (001) substrate. Top-view SEM images of Ⅲ–Ⅴ layers (b) on the (111)-faceted Si (001) hollow substrate and (d) on the standard Si (001) substrate, respectively.

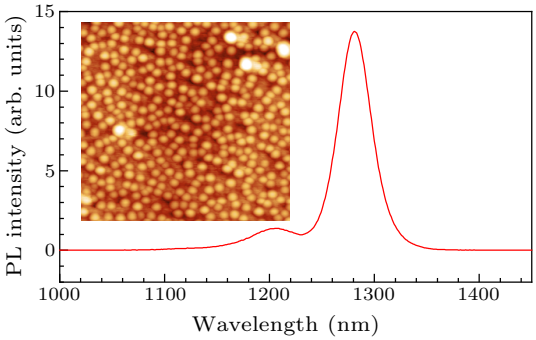

Fig. 8. Room-temperature PL spectrum of InAs/GaAs QDs on the Si (001) substrate. Inset: $1 \times 1\,\mu m^2$ AFM image of surface InAs/GaAs QDs.

To further confirm the quality of GaAs layers on these (111)-faceted Si (001) hollow substrates, a 7-layer self-assembled InAs/GaAs QD structure was grown. The room-temperature PL spectrum of the QD sample is shown in Fig. 8, which indicates that the InAs/GaAs QDs on Si (001) have a highly efficient O-band emission at the peak wavelength of 1281 nm with 29 meV spectral linewidth. The inset in Fig. 8 is the $1 \times 1\,\mu m^2$ AFM image showing the homogeneous surface InAs QDs on Si (001) with a dot density of $3.66 \times 10^{10}/cm^2$.

In summary, we have systematically investigated the Si homoepitaxy on U-shape patterned Si (001) oriented along both [110] and [100] directions. A hollow structure can be obtained on [110] oriented patterns, while it is infeasible to obtain such a structure on [100] oriented patterns. By varying the growth temperature of homoepitaxy on [110] oriented patterns, the dimensional and geometric evolutions of hollow structures are experimentally demonstrated. Furthermore, by implementing this technique, APB and thermal crack free GaAs epi-layers can be obtained for applications of silicon based Ⅲ–V optoelectronic devices.

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