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Improvement of Operation Characteristics for MONOS Charge Trapping Flash Memory with SiGe Buried Channel *

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We propose and investigate a novel metal/SiO_2/Si_3N_4/SiO_2/SiGe charge trapping flash memory structure (named as MONOS), utilizing SiGe as the buried channel. The fabricated memory device demonstrates excellent program-erasable characteristics attributed to the fact that more carriers are generated by the smaller bandgap of SiGe during program/erase operations. A flat-band voltage shift 2.8 V can be obtained by programming at +11 V for 100 μs. Meanwhile, the memory device exhibits a large memory window of ∼7.17 V under ±12 V sweeping voltage, and a negligible charge loss of 18% after 10^4 s' retention. In addition, the leakage current density is lower than 2.52×10^{-7} A·cm^{-2} below a gate breakdown voltage of 12.5 V. Investigation of leakage current-voltage indicates that the Schottky emission is the predominant conduction mechanisms for leakage current. These desirable characteristics are ascribed to the higher trap density of the Si_3N_4 charge trapping layer and the better quality of the interface between the SiO_2 tunneling layer and the SiGe buried channel. Therefore, the application of the SiGe buried channel is very promising to construct 3D charge trapping NAND flash devices with improved operation characteristics.

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The increasing demand of high density nonvolatile memory has made polycrystalline silicon (poly-Si) an attractive channel material for three-dimensional (3D) charge trapping NAND flash devices. However, the very low electron mobility and high trap densities of poly-Si channel deteriorate the device performance such as lower drive current (I_d) for reading operations and larger sub-threshold slope (SS).[1] To improve memory performances, such as higher program/erase (P/E) efficiency and lower power consumption, a series of studies have been carried out to engineer the memory dielectric layers, i.e., optimizing blocking layer,[2] charge trapping layer[3] or tunneling layer.[4] The optimized memory layer stacks can enhance the electric field across the tunneling layer and suppress the electric field across the blocking layer, resulting in improved P/E efficiency and data retention. Moreover, the optimization of channel material can also improve memory performance. Recently, some efforts on the utilization of SiGe channel with high electron/hole injection rate have been reported to be able to improve P/E efficiency.[5–7] Electron/hole injection increases because SiGe has a smaller bandgap than silicon. As the electron/hole injection located at the tunneling oxide/SiGe channel increases, the number of electrons tunneling through the tunneling oxide is increased and the P/E speed is improved. Furthermore, the tunneling electric-field strength can be enhanced owing to the SiGe buried channel.[8] Integration of SiGe channel into current 3D charge trapping NAND flash memory has the potential to realize low power consumption and high operating efficiency.

Since it is difficult for SiGe to form a good interface with the widely used dielectrics in industry, a thin silicon cap layer is necessary to be deposited on top of SiGe to avoid its direct contact with gate stacks. The thin Si-cap layer is helpful for suppressing the out-diffusion of Ge atoms and forming the SiO_2 tunneling layer with better interface quality.[9] A better interface between the SiO_2 tunneling layer and the Si-cap layer is obtained when compared with that formed by directly oxidizing the SiGe layer.

To further improve the performance for future 3D NAND flash memory, we propose and investigate a novel metal/SiO_2/Si_3N_4/SiO_2/SiGe memory structure (named as MONOS), utilizing SiGe as the buried channel. As is expected, the proposed MONOS memory devices exhibit superior charge trapping efficiency, large memory window, fast P/E speed, and excellent data retention characteristics.

The MONOS memory devices with SiGe buried channel were fabricated on p-type Si (100) wafer with resistivity of 8–12 Ω·cm. Prior to SiGe epitaxial growth, p-type wafer was cleaned by the standard RCA method, and the surface oxide was removed using a dilute HF 1% solution. Then a 20-nm-thick epitaxial SiGe layer with 30% Ge contents was grown using reduced pressure chemical vapor deposition (RPCVD) at a pressure of 20 Torr,[10] followed by a 5-nm-thick Si-cap layer for suppressing the out-

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diffusion of Ge atoms. Then, a 2-nm-thick tunneling SiO_2 was grown by rapid thermal oxidation at 800℃, and a 10-nm-thick Si_3N_4 charge trapping layer was deposited by plasma enhanced chemical vapor deposition (PECVD). Next, a 6-nm-thick blocking SiO_2 was deposited by the same PECVD method. Afterwards, a 30-nm-thick aluminum was deposited subsequently as the metal gate. Finally, forming gas annealing (FGA) was applied for 30 min and at 400℃ to passivate the interface between the SiO_2 tunneling layer and the SiGe buried channel. Figure 1 shows the schematic diagram of the fabricated MONOS memory device structure.

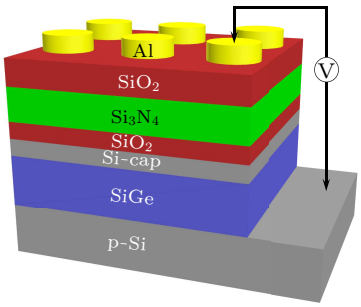

Fig. 1. The schematic diagram of the fabricated MONOS memory device structure.

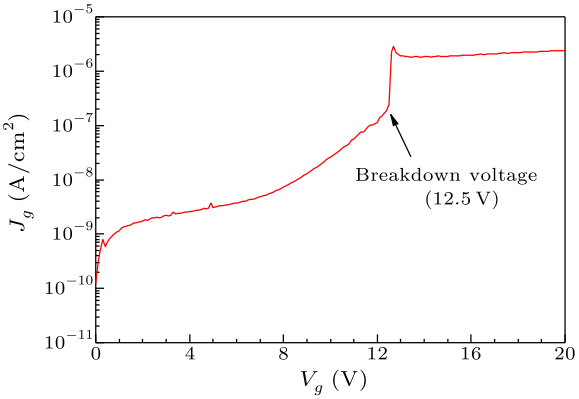

Fig. 2. Leakage current-voltage characteristics for MONOS memory devices.

Electrical capabilities including high frequency capacitance-voltage (C–V) hysteresis characteristics, constant current stress (CCS), P/E speed, and retention time were measured by a Keithley 4200 semiconductor characterization system (Keithely 4200 SCS) at room temperature. In addition, J–V leakage current characteristics were measured with an Agilent 4156C semiconductor analyzer.

Before the evaluation of memory characteristics, the gate breakdown voltage (BV_g) is measured. Figure 2 reveals the leakage current density for the MONOS memory devices measured at room temperature. The gate voltage is varied from 0 to 20 V to measure the breakdown voltage of the MONOS devices and a large BV_g of 12.5 V is observed for all memory devices. Meanwhile, the leakage current density is lower than 2.52×10^{-7} A·cm^{-2} below the gate breakdown voltage. Owing to the small gate leakage current, the retention characteristics can be improved for our memory structure.

The band diagram of the MONOS memory structure is shown in Fig. 3, which is defined according to the electron affinity and the band gap values.

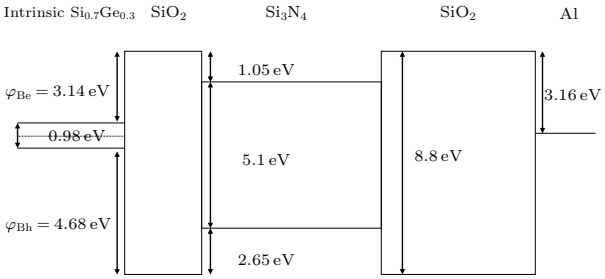

Fig. 3. Band diagram of the MONOS memory structure without external electrical field.

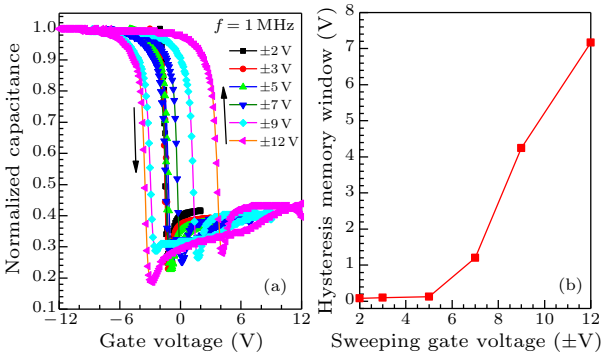

Fig. 4. (a) Bi-directional normalized C–V hysteresis for MONOS memory devices. (b) Dependence of sweeping voltage on hysteresis memory window for MONOS memory devices.

Figure 4(a) shows the bi-directional capacitance-voltage (C–V) hysteresis curves for MONOS memory devices with Si_3N_4 as the charge trapping layer by applying different sweeping voltages measured at 1 MHz. A typical hysteresis loop direction of charge trapping was observed during positive-negative-positive voltage sweep. The counterclockwise hysteresis is attributed to the injection of deep-inversion electrons from the channel.[11] With respect to the positive-negative sweep, the device undergoes a positive voltage stress at the initial sweep stage, which is equivalent to a program operation. In this status, the channel electrons will accumulate at the tunneling SiO_2 layer/SiGe interface. If the gate voltage is high enough, some electrons might tunnel through the SiO_2 tunneling layer and might be captured by the defect states of the Si_3N_4 charge trapping layer. During the negative-positive sweep, the device undergoes a negative voltage stress at the initial stage, which is equivalent to the erase operation. In this status, the storage electrons will tunnel back to the channel; simultaneously holes will tunnel through the SiO_2 tunneling layer and become trapped in the Si_3N_4 layer.

Figure 4(b) summarizes the dependence of the sweeping voltage on the hysteresis memory window

for the fabricated MONOS memory devices. When sweeping the gate voltage from 5 to −5 V and then reversing it, the MONOS structure exhibits a negligible C–V hysteresis, indicating that charge trapping and de-trapping hardly take place in this voltage sweep range. Large hysteresis is observed for voltage sweeps above ±7 V. As the sweeping voltage increases from ±7 V, ±9 V and ±12 V, the hysteresis memory window (flat-band voltage shift, $\Delta V_{\rm FB}$) increases from 1.2 V, 4.24 V and 7.17 V. The excellent charge trapping characteristics of our MONOS memory devices are believed to originate from the high density of trap states of Si_3N_4 films and higher electron/hole injection rate of SiGe buried channel with smaller bandgap.

Using a very simple calculation method, the charge trap density $N_{\rm t}$ can be estimated by[12]

$$N_{\rm t} = \frac{C_{\rm total}\Delta V_{\rm FB}}{q}, \tag{1}$$

where $C_{\rm total}$ is the accumulation capacitance per unit area, $\Delta V_{\rm FB}$ is the hysteresis memory window, and q is the electron charge. In this case, $C_{\rm total} = 140\,{\rm nF/cm^2}$. According to the above equation, the charge trap density under ±12 V sweeping voltage is estimated to be $6.27 \times 10^{12}\,{\rm cm^{-2}}$, indicating that the Si_3N_4 charge trapping layer exhibits a high density of charge traps.

The C–V and G–V measurements were carried out to estimate the interface state density $D_{\rm it}$. According to the conductance method proposed by Nicollian, $D_{\rm it}$ can be obtained to be[13]

$$D_{\rm it} = \frac{1}{qA}\left(\frac{\langle G_{\rm p}\rangle}{\omega}\right)_{\rm fp}[f_{\rm D}(\sigma_{\rm s})]^{-1} \approx \frac{0.4}{qA\omega}\langle G_{\rm p}\rangle, \tag{2}$$

$$\langle G_{\rm p}\rangle = \frac{\omega^2 C_{\rm ox}^2 G_{\rm m}}{G_{\rm m}^2 + \omega^2(C_{\rm ox} - C_{\rm m})^2}, \tag{3}$$

where $\langle G_{\rm p}\rangle$ is the maximum ac conductance with its corresponding test value capacitance $C_{\rm m}$ and conductance $G_{\rm m}$, $C_{\rm ox}$ is estimated from the capacitance in the accumulation region of the C–V curve, and A and ω are the gate area and the ac signal frequency, respectively.

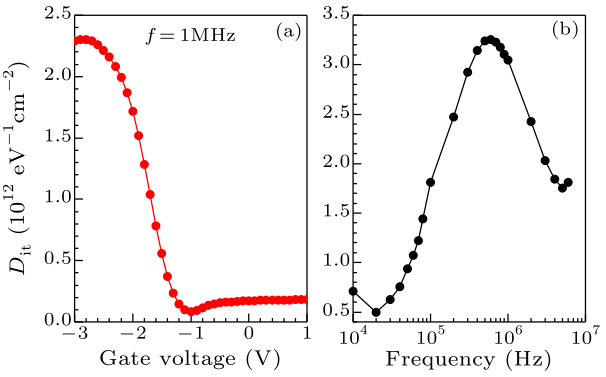

Fig. 5. (a) Interface state density curve of the MONOS memory devices. (b) The distribution of interface state density as a function of frequency.

The interface state density curve is obtained at f = 1 MHz, as shown in Fig. 5(a). Peak value represents the interface densities, which is calculated to be $2.3 \times 10^{12}\,{\rm eV^{-1}\cdot cm^{-2}}$. The estimated $D_{\rm it}$ is comparatively low for memory devices, which is mainly attributed to the interface passivation via forming gas annealing. Figure 5(b) compares $D_{\rm it}$ of the MONOS at different frequencies. With the increase of frequency, $D_{\rm it}$ reaches a peak and then decreases. The peak value of $D_{\rm it}$ occurs at 600 kHz.

Figure 6(a) shows the charge trapping characteristics of MONOS memory devices. Various constant current stresses (CCS) were applied to the gate electrode. The voltage-drop at the gate stacked layer was measured as the gate voltage shift varying with increasing the stress time. The shift in gate voltage is attributed to the charge trapping in the Si_3N_4 trap layer.[14] Accordingly, we can obtain that the MONOS structure has good charge trapping characteristics. Moreover, the location of majority trap sites in the $SiO_2/Si_3N_4/SiO_2$ stack is estimated by the computation of charge trap centroid. The charge trap centroid ($X_{\rm cent}$) extracted by CCS measurement is computed by[15]

$$X_{\rm cent} = \frac{t_{\rm stack}}{[1 - \Delta V_{\rm g}^{-}/\Delta V_{\rm g}^{+}]}, \tag{4}$$

where $X_{\rm cent}$ is measured from the metal gate/SiO_2 blocking layer interface, $t_{\rm stack}$ is the thickness of $SiO_2/Si_3N_4/SiO_2$ stack, and $\Delta V_{\rm g}^{+}$ and $\Delta V_{\rm g}^{-}$ are the negative and positive gate voltage shifts after constant current stress, respectively. Here we applied constant current stress of $10\,\mu{\rm A/cm^2}$ to the gate electrode, as shown in Fig. 6(b). The calculated $X_{\rm cent}$ is 10.85 nm, which signifies that $X_{\rm cent}$ is located at ∼10.86 nm below the aluminum/blocking SiO_2 interface. Thus the charge trap centroid is located at ∼4.85 nm below the blocking SiO_2/Si_3N_4, which is close to the middle of the Si_3N_4 charge trapping layer.

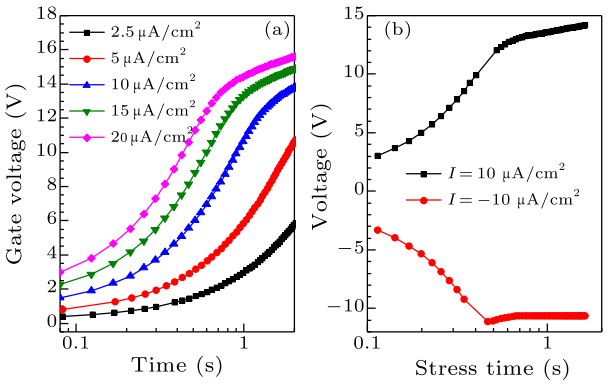

Fig. 6. (a) Charge trapping characteristics for the MONOS memory devices under various constant current stresses. (b) Charge trapping characteristics of the MONOS structure under constant current stress of $10\,\mu{\rm A/cm^2}$.

Typical P/E transients for the MONOS memory devices are shown in Fig. 7. The memory structure is efficiently programmed and erased at several typical operating voltages of ±7 V, ±9 V, and ±11 V. Before

the erasing measurement, the memory devices are first programmed at 11 V for 100 ms to obtain the same $\Delta V_{\rm FB}$ of 4.1 V. The shift of $V_{\rm FB}$ is significant after programming or erasing for 10 μs, indicating the enhanced electron/hole injection rate of the SiGe buried channel. As a result, $\Delta V_{\rm FB}$ of 2.8 V can be obtained at +11 V program voltage for 100 μs. With −11 V erase voltage for 100 ms, $\Delta V_{\rm FB}$ of −5.66 V can be realized, indicating the erasing efficiency of the memory structure.

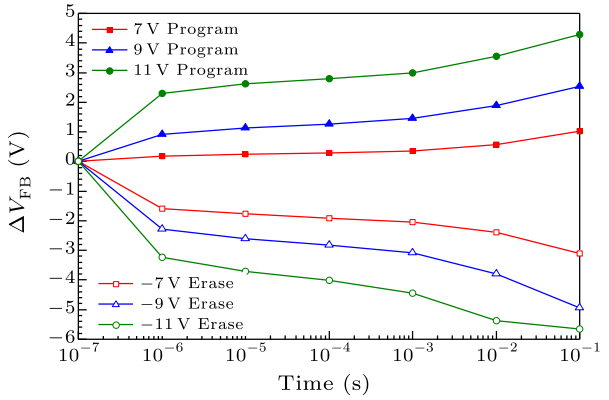

Fig. 7. P/E transient characteristics for MONOS memory devices.

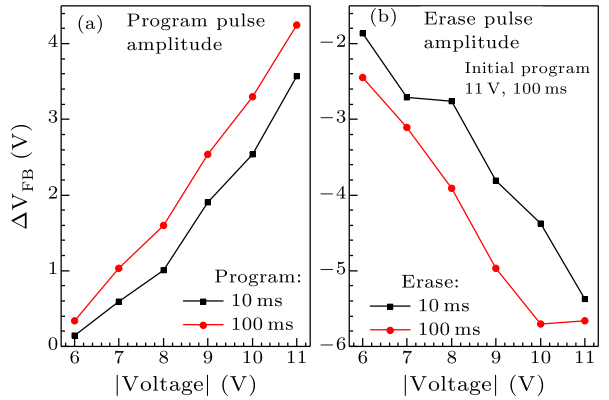

Fig. 8. Program/erase window at different applied gate voltages (in the range of 6–11 V). The operating conditions are: program and erase for 10 ms and 100 ms pulse durations.

Figure 8 shows the $\Delta V_{\rm FB}$ values of the fabricated MONOS memory when the devices are programmed and erased at various gate voltages for 10 ms and 100 ms pulse durations. It is worth mentioning that the memory devices are first programmed at 11 V for 100 ms to obtain a $\Delta V_{\rm FB}$ of 4.1 V before the erasing operation. The memory window increases by increasing the applied gate voltage. Meanwhile, increasing the P/E pulse duration can also enlarge the memory window. From Fig. 8, we also notice that the erase speed is slightly faster than the program speed. The asymmetrical P/E characteristics can be ascribed to a smaller valence band offset (2.03 eV) than the conduction band offset (2.09) between the Si_3N_4 charge trapping layer and the SiGe buried channel, as shown in Fig. 3. Consequently, more holes are thus injected into the Si_3N_4 trapping layer to improve the erasing speed.

Figure 9(a) presents the data retention characteristics of the fabricated MONOS memory devices at room temperature. The memories are first programmed to obtain a $\Delta V_{\rm FB}$ of 3.2 V before data retention test. The charge loss $Q_{\rm loss}$ is defined as[16]

$$Q_{\rm loss} = \frac{V_{\rm FB}(0) - V_{\rm FB}(t)}{V_{\rm FB}(0) - V_{\rm FBi}} \times 100\%, \qquad (5)$$

where $V_{\rm FBi}$ is the flat-band voltage at the initial state, $V_{\rm FB}(0)$ is the flat-band voltage after programming to obtain a certain $V_{\rm FB}$ shift, and $V_{\rm FB}(t)$ is the flat-band voltage after the retention time t. The MONOS memory device shows a good data retention property of 18% charge loss after 10^4 s, and the retained charge after 10 y can be extrapolated to be 51%. Hence, the retention performance is good enough for practical applications.

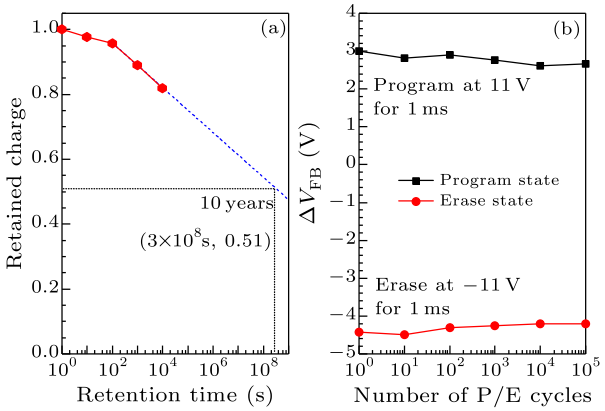

Fig. 9. (a) Data retention characteristics for MONOS memory devices. (b) Data endurance characteristics for MONOS memory devices.

To investigate the endurance performance, a P/E pulse voltage (±11 V with pulse width of 1 ms) up to 10^5 cycles is applied. Figure 9(b) shows the endurance characteristics of the MONOS memory device. A negligible endurance degradation of 2% is observed even after 10^5 P/E cycles, which indicates that the MONOS memory device is good enough to be used for flash memories.

To clarify the role of the trap charge in the formation of leakage current, the conduction mechanism of the leakage current is necessarily investigated. There are several possible mechanisms responsible for leakage current, such as direct quantum tunneling, the Fowler–Nordheim tunneling, the Schottky emission and the Poole–Frenkel emission. For a nano-flash memory device, a low-field (<5 MV/cm) direct quantum tunneling and the Schottky emission mechanism have been reported.[17]

The Schottky emission (SE) mechanism is described as[18]

$$J = A^* T^2 \exp\left[\frac{-q(\Phi_{\rm B} - \sqrt{qE/4\pi\varepsilon_{\rm r}\varepsilon_0})}{kT}\right], \qquad (6)$$

where J is the current density, E is the electric field, A^* is the effective Richardson constant, Φ_B is the barrier height, ε_r is the dielectric constant, q is the electronic charge, and k is the Boltzmann constant.

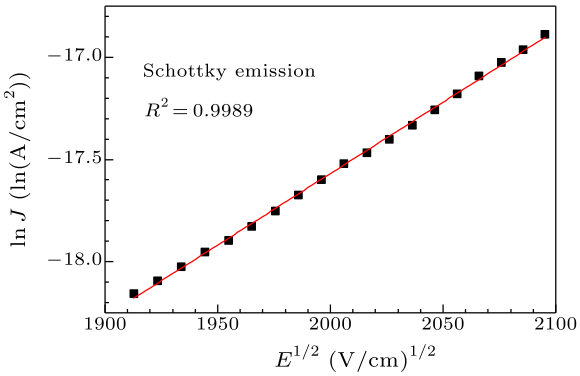

Fig. 10. Schottky emission model fitted for the determination of conduction mechanisms in MONOS memory devices.

According to the measured data in Fig. 2, the logarithmic current density $\ln(J)$ versus the square root of electric field $E^{1/2}$ are plotted as shown in Fig. 10. Relative fair linear tendency of the plots of $\ln(J)$ versus $E^{1/2}$ for the samples is obtained, implying the Schottky emission at the electric field between 3.6 MV/cm and 4.4 MV/cm. The plot of $\ln(J)$ versus $E^{1/2}$ is very well fitted ($R^2 = 0.9989$) with the Schottky emission mechanism, and Φ_B and ε_r are calculated to be 1.22 eV and 4.34, respectively. This ε_r value is very close to the dielectric constants of SiO_2.

In summary, we have realized a novel MONOS memory device structure based on the SiGe buried channel. The P/E speeds of MONOS memory devices are significantly improved by employing the SiGe buried channel. Meanwhile, the proposed design achieves superior characteristics in terms of large memory windows, lower leakage current and long retention time, which are resulted from the higher trap density of the Si_3N_4 charge trapping layer and the better quality of the SiO_2 tunneling layer/SiGe buried channel interface. Therefore, the application of the SiGe buried channel is very promising to construct 3D charge trapping NAND flash devices with improved operation characteristics, and we will carry out more in-depth research to further optimize the memory device performance.

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