Crystallization Process of Superlattice-Like Sb/SiO_2 Thin Films for Phase Change Memory Application *

Xiao-Qin Zhu(朱小芹)[1], Rui Zhang(张锐)[1], Yi-Feng Hu(胡益丰)[1,3,4**], Tian-Shu Lai(赖天树)[2], Jian-Hao Zhang(张剑豪)[1], Hua Zou(邹华)[1], Zhi-Tang Song(宋志棠)[5]

[1]*School of Mathematics and Physics, Jiangsu University of Technology, Changzhou 213001*
[2]*State Key Laboratory of Optoelectronic Materials and Technologies, School of Physics, Sun Yat-Sen University, Guangzhou 510275*
[3]*State Key Laboratory of Silicon Materials, Zhejiang University, Hangzhou 310027*
[4]*Key Laboratory of Microelectronic Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029*
[5]*State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Micro-System and Information Technology, Chinese Academy of Sciences, Shanghai 200050*

(Received 27 November 2017)

After compositing with SiO_2 layers, it is shown that superlattice-like Sb/SiO_2 thin films have higher crystallization temperature (∼ 240°C), larger crystallization activation energy (6.22 eV), and better data retention ability (189°C for 10 y). The crystallization of Sb in superlattice-like Sb/SiO_2 thin films is restrained by the multilayer interfaces. The reversible resistance transition can be achieved by an electric pulse as short as 8 ns for the $Sb(3\,nm)/SiO_2(7\,nm)$-based phase change memory cell. A lower operation power consumption of 0.09 mW and a good endurance of 3.0×10^6 cycles are achieved. In addition, the superlattice-like $Sb(3\,nm)/SiO_2(7\,nm)$ thin film shows a low thermal conductivity of 0.13 W/(m·K).

PACS: 68.05.Cf, 68.55.−a, 68.65.−k DOI: 10.1088/0256-307X/35/5/056803

Phase change memory (PCM) technology is widely recognized as one of the promising next-generation nonvolatile memory solutions, which offers high density, good endurance, low power consumption, fast programming capability, and fabrication compatibility with complementary metal oxide semiconductor (CMOS).[1,2] The basic principle is based on the electrothermal-induced reversible phase change of the chalcogenide materials between the amorphous (showing high resistivity) and crystalline states (showing low resistivity). The data storage can be realized by discerning the enormous differentiation of the two resistance states.[3]

Before the large-scale application of PCM, there are two prominent issues which should be solved, including the slow phase change speed and high operation power consumption.[4,5] In many solutions, numerous new phase change materials have been developed because the characteristics of phase change materials have great influence on PCM. Nowadays, $Ge_2Sb_2Te_5$ (GST) is the most widely used phase change material for its business application in optical storage.[6] However, the poor data retention (85℃ for 10 y) and slow switching speed in SET and RESET operation processes limit its application in future mass storage.[7] It was reported that the PCM device based on the GST material is difficult to have an entire operating window when the width of the voltage pulse is shorter than 100 ns, which is insufficient to meet the requirement of dynamic random access memory (DRAM) (∼10 ns).[8] Recently, it has been proved that Sb-rich phase change materials, such as Ge-Sb,[9] Sn-Sb[10] and Cu-Sb-Te,[11] have faster switching characteristics due to the growth-dominated crystallization mechanism. In comparison of bulk materials, the phase change materials with superlattice-like (SLL) structures have better performance in working speed and a lower programming current.[12] Moreover, SLL phase change materials can combine the phase change performance of different composite layers to obtain an excellent comprehensive property.[13] In this work, two elemental materials of Sb and SiO_2 are used to prepare SLL Sb/SiO_2 thin films. Using thermal and electric characterizations, the potential application of PCM can be evaluated.

SLL Sb/SiO_2 thin films with different periods and thickness ratios, as well as monolayer Sb thin film, were deposited on 0.5-mm-thick oxidized Si (100) wafers using an rf magnetron sputtering system at room temperature. The total thickness of the thin films and the periodicity were set to be 50 nm and 5, respectively. The thickness of each individual layer was controlled by the deposition time. Prior to the growth of SLL Sb/SiO_2 thin films, the deposition rates of Sb and SiO_2 single layers were predetermined. An Alpha-Step 500 profiler (Tencor Instrument) was used

*Supported by the National Natural Science Foundation of China under Grant No 11774438, the Natural Science Foundation of Jiangsu Province under Grant No BK20151172, the Changzhou Science and Technology Bureau under Grant No CJ20160028, the Qing Lan Project, the Opening Project of State Key Laboratory of Silicon Materials under Grant No SKL2017-04, and the Opening Project of Key Laboratory of Microelectronic Devices and Integrated Technology of Institute of Microelectronics of Chinese Academy of Sciences.

**Corresponding author. Email: hyf@jsut.edu.cn

© 2018 Chinese Physical Society and IOP Publishing Ltd

to measure the thickness of the films. All the deposition processes were carried out under the conditions of Ar atmosphere at the pressure of 0.4 Pa, the flow rate of 30 sccm, and an rf power of 30 W. To ensure uniformity of deposition, the rotation speed of the substrate was set to 20 rpm.

In situ temperature-dependent resistance (R–T) of the samples was performed in Ar atmosphere using a custom-made two-point-probe setup to obtain the phase-change details by a TP 94 temperature controller. The data retention was estimated by measuring the resistance of samples using the isothermal heating. The crystalline phases of the films were analyzed by x-ray diffraction (XRD, Rigaku D/MAX 2550V) with Cu K_α radiation in the 2θ degree range from 20° to 60°, with a scanning step of 1°/min. The so-called 3ω method was set up and integrated with an atomic force microscope to probe the nanoscale thermal property with the intention of measuring the local thermal conductivity. The voltage-current (V–I), resistance-voltage (R–V), and reversible switching properties of PCM cells based on GST and SLL Sb/SiO_2 thin films were measured by a Tektronix AWG5012B arbitrary waveform generator and a Keithley 2602A parameter analyzer.

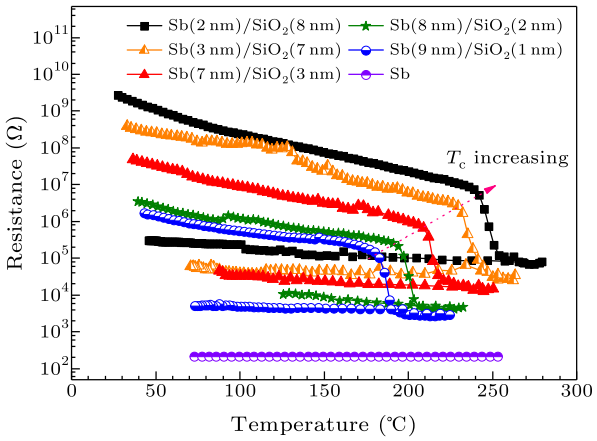

Fig. 1. The R–T curves of SLL Sb/SiO_2 and monolayer Sb thin films.

Figure 1 shows the R–T curves of SLL Sb/SiO_2 and monolayer Sb thin films at an invariable rate of 30℃/min (initially, because of a thermally assisted trap-limited conduction the heat conduction assists trap limit, when the temperature begins to rise the rate of decline of all resistance amorphous SLL Sb/SiO_2 film is slow). Initially, the resistance of all amorphous SLL Sb/SiO_2 thin films decreased slowly with the increase of temperature due to a thermally assisted trap-limited conduction.[14] Then a quick drop of resistance followed, which was associated with the transformation between amorphous and crystalline states. The transform temperature was defined as the crystallization temperature T_c. As shown in Fig. 1, all SLL Sb/SiO_2 thin films had achieved a tremendous resistance decreasing of nearly two orders of magnitude, which could discriminate the operation of reading and writing. In contrast, the poor thermal stability of the pure Sb thin film resulted in the formation of the Sb crystalline phase during the deposition process, thus we could not observe significant resistance changes during heating. According to the measurement, T_c for Sb(9 nm)/SiO_2(1 nm) was 182℃. With increasing the thickness ratio of SiO_2 to Sb in SLL Sb/SiO_2 thin films, T_c increased gradually to 192℃ for Sb(8 nm)/SiO_2(2 nm), 209℃ for Sb(7 nm)/SiO_2(3 nm), 230℃ for Sb(3 nm)/SiO_2(7 nm) and 240℃ for Sb(2 nm)/SiO_2(8 nm), respectively. Generally, the thermal stability of the amorphous film could be roughly evaluated through the crystallization temperature T_c. Obviously, more SiO_2 elements greatly improved the amorphous stability of the Sb film. In addition, the resistance of the crystalline state increased from $2 \times 10^2\,\Omega$ of Sb to $9.8 \times 10^4\,\Omega$ of Sb(2 nm)/SiO_2(8 nm). This is helpful to reduce the driving current for the reset operations of PCM according to Ohm's law.

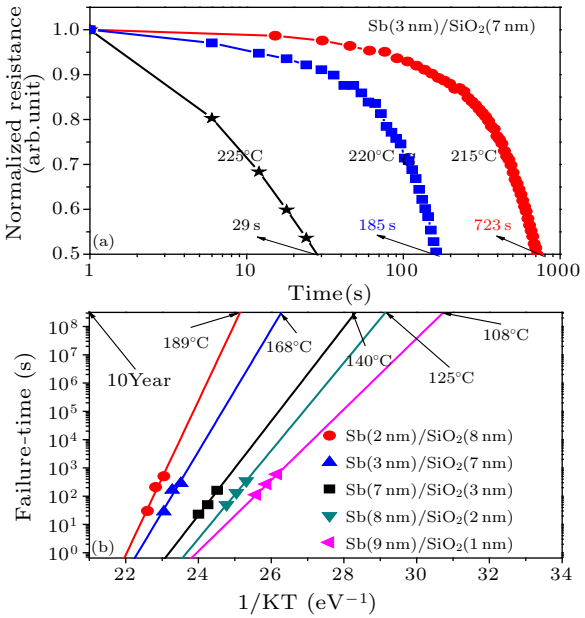

Fig. 2. (a) The normalized resistance of SLL Sb(3 nm)/SiO_2(7 nm) thin film as a function of annealing time at various temperatures. (b) Arrhenius plots of data retention showing extrapolated temperatures of 10-year data retention for SLL Sb/SiO_2thin films.

Data retention capability is a very important parameter for PCM devices and is usually estimated by extrapolating isothermal Arrhenius curves.[15] The time-dependent resistance at different temperatures was used to evaluate the data retention of SLL antimony/SiO_2 films. The failure time was defined as the time when the resistance reaches half the initial value at a specific isothermal temperature. Figure 2(a) shows that the failure times of Sb(3 nm)/SiO_2(7 nm) at 225, 220 and 215℃ were 28, 185 and 723 s, respectively. That is, as the isothermal temperature decreases, the longer the time the phase change material

needs to accumulate enough energy for crystallization. The plot of logarithm failure time versus $1/(k_bT)$, which fits a linear Arrhenius relationship due to its thermal activation nature, can be expressed as[16]

$$t = \tau_0 \exp[E_c/(k_b \times T)], \quad (1)$$

where E_c, t, τ, k_b and T are the activation energy, the failure time, the pre-exponential factor depending on the material's properties, Boltzmann's constant and the absolute temperature of concern, respectively. A higher E_c will increase the obstacle for crystallization, resulting in better amorphous thermal stability. The 10-year lifetime for SLL Sb/SiO_2 thin films increased from 108℃ of Sb(9 nm)/SiO_2(1 nm) to 189℃ of Sb(2 nm)/SiO_2(8 nm). From this perspective, SLL Sb/SiO_2 thin films possess better reliability of the amorphous state to meet the application of data storage at elevated temperature.

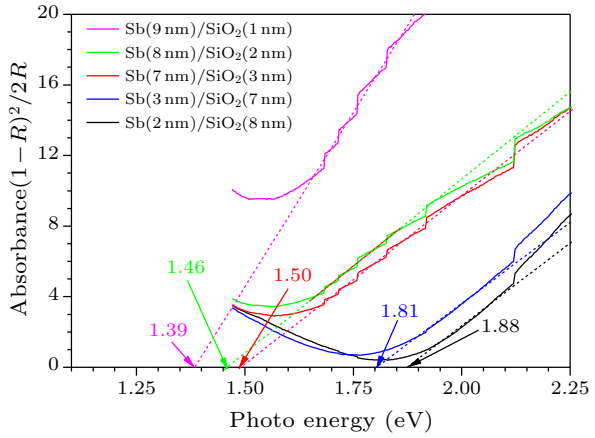

Fig. 3. The Kubelka–Munk function of SLL Sb/SiO_2 thin films.

The band gap energy E_g could be determined by extrapolating the absorption edge onto the energy axis, as shown in Fig. 3. The conversion of the reflectivity to absorbance data was obtained by the Kubelka–Munk (K-M) function[17]

$$K/S = (1 - R)^2/(2R), \quad (2)$$

where R is the reflectivity, K is the absorption coefficient and S is the scattering coefficient. The band gap energy of Sb(9 nm)/SiO_2(1 nm), Sb(8 nm)/SiO_2(2 nm), Sb(7 nm)/SiO_2(3 nm), Sb(3 nm)/SiO_2(7 nm) and Sb(2 nm)/SiO_2(8 nm) thin films were 1.39, 1.46, 1.50, 1.81 and 1.88 eV, respectively. With the increase of the relative thickness of the SiO_2 layer, E_g of amorphous films was extended. Because the carrier density inside the semiconductors was proportional to $\exp(-E_g/2kT)$,[18] an increase in the band gap would lead to the reduction of carriers, which made a major contribution to the increase of the film resistivity after adding more SiO_2. This finding was supported by the change trends of resistance curves in Fig. 1.

Figure 4 shows the XRD patterns of pure SLL Sb(3 nm)/SiO_2(7 nm) thin films. No diffraction peaks were observed in as-deposited and 150℃ annealed SLL Sb(3 nm)/SiO_2(7 nm) thin films in Fig. 4, indicating an amorphous nature. The first appearance of the Sb (110) diffraction peak was at the temperature 234℃, which demonstrates its good amorphous thermal stability. When the annealing temperature rises to 280℃, another tiny Sb(015) appears in the thin film of SLL Sb(3 nm)/SiO_2(7 nm). Moreover, no SiO_2 diffraction peaks were observed in all the XRD curves. It shows that the existence of SiO_2 in amorphous state was beneficial to improve the stability of Sb material.

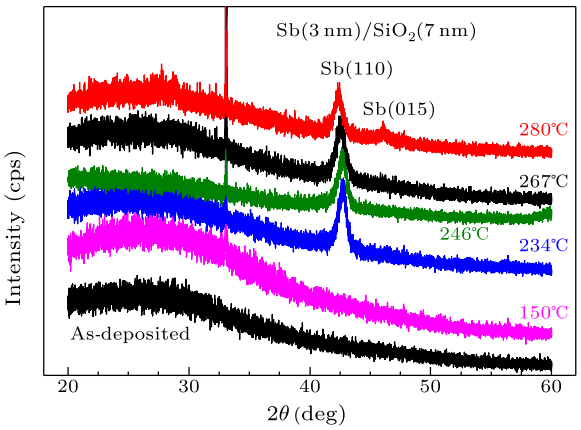

Fig. 4. XRD patterns of SLL Sb(3 nm)/SiO_2(7 nm) thin film annealed at different temperatures for 10 min in Ar atmosphere.

The thermal conductivity of the phase change film is one of the factors that affect the power dissipation of the PCM cells.[19] In this study, scanning probe microscopy (SPM) was used to investigate microstructures and local thermal conductivity properties of various materials and devices in nanoscale.[20] Based on SPM, scanning thermal microscopy (SThM) was developed to give simultaneous surface topography image and thermal property image of materials with micro or submicrometer spatial resolution. Monolayer SiO_2, Sb, and SLL Sb(3 nm)/SiO_2(7 nm) thin films were used as thermal conductivity measuring. The results show that the thermal conductivity of the SLL Sb(3 nm)/SiO_2(7 nm) thin film is 0.13 W/(m·K), which is much lower than those of monolayer SiO_2 (0.75 W/(m·K)) and Sb (2.53 W/(m·K)). A low thermal conductivity can help to reduce the heat dissipation, so as to improve the heating efficiency. Therefore, a low thermal conductivity of SLL structure is believed to play a part in decreasing the power consumption of PCM devices.

PCM cells based on SLL Sb(3 nm)/SiO_2(7 nm) and GST thin films were fabricated to test and verify their electrical properties using the 0.18 μm CMOS technology. The cross-sectional transmission electron microscopy image is shown in the inset of Fig. 5(a). A 20-nm-thick TiN layer was deposited to improve the interface between the phase change layer (PCL) and

the top electrode (Al). Figure 5(b) shows the current-voltage (I–V) switching characteristics of the cell devices. With the increase of the sweeping current, the voltage returns to a smaller value, indicating negative resistance characteristics. The low conductive state of Sb(3 nm)/SiO_2(7 nm) was maintained until the threshold voltage $V_{th} = 1.4$ V was reached, which is much lower than that of GST (4.2 V). After switching, the voltage drops suddenly and the device transforms into a highly conductive state.

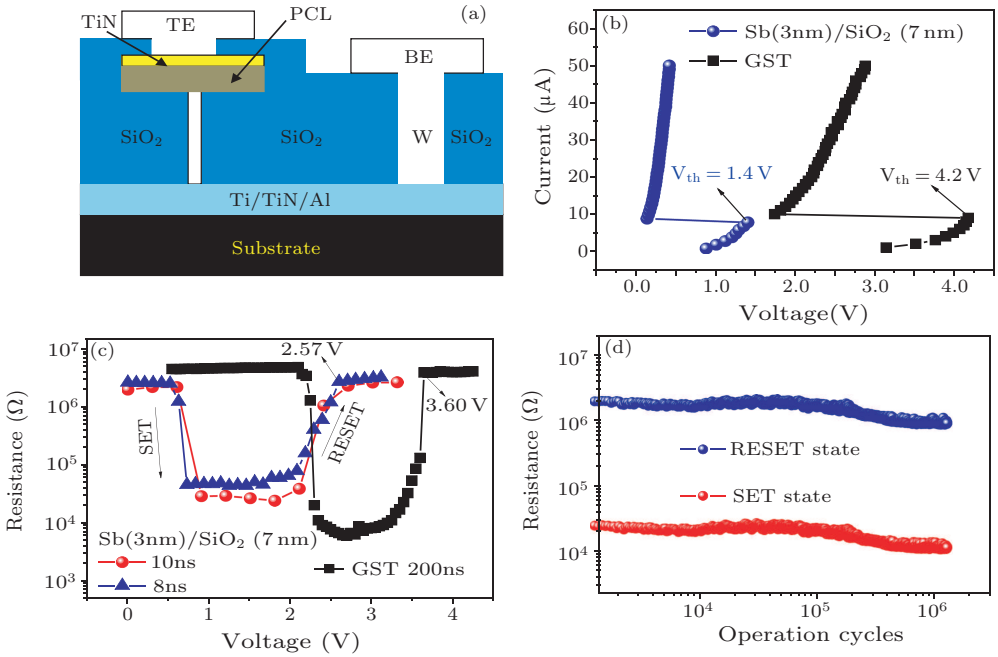

Fig. 5. (a) The schematic diagram of the PCM cell structure. (b) Current-voltage characteristics of PCM devices fabricated with the SLL Sb(3 nm)/SiO_2(7 nm) thin film. (c) Resistance-voltage characteristics of the PCM cells based on the SLL Sb(3 nm)/SiO_2(7 nm) thin film. (d) The reversible switching of the Sb(3 nm)/SiO_2(7 nm)-based PCM device.

The R–V curves, as shown in Fig. 5(c), exhibit a reversible switching phenomenon between the SET and RESET states. The GST-based PCM device could achieve a stable operation window with the pulse width 200 ns and RESET voltage 3.60 V. By contrast, the Sb(3 nm)/SiO_2(7 nm)-based cell could easily have the resistance switching with the pulse width 8 ns. The result indicates that SLL Sb(3 nm)/SiO_2(7 nm) has a faster switching speed than GST. This is ascribed to the result of the precipitation of Sb crystallites. Sb is characterized by an explosive crystallization, which is a thermal process with the heat that is released at the crystallization front serving to drive the crystallization of the surrounding amorphous regions further. Sb crystallite can be used as a template for subsequent crystallization to reduce the crystallization time of Sb(3 nm)/SiO_2(7 nm).[21]

According to the relation $P = V^2/R$, the power for the Sb (3 nm)/SiO_2(7 nm)-based PCM device was 0.09 mW, which is much lower than that of GST (1.22 mW). Therefore, SLL Sb(3 nm)/SiO_2(7 nm) thin film power consumption is lower. Moreover, the reversible switching up to 3.0×10^6 cycles without failure, as shown in Fig. 5(d), is realized for the Sb(3 nm)/SiO_2(7 nm)-based device cell. Good durability further proves the practicability of SLL Sb/SiO_2 thin films in PCM devices.

In summary, SLL Sb/SiO_2 materials have been investigated for use as appropriate phase-change materials in PCMs. Compared with pure Sb, SLL Sb/SiO_2 materials have better amorphous thermal stability (Sb(9 nm)/SiO_2(1 nm), T_c = 182℃; Sb(8 nm)/SiO_2(2 nm), T_c = 192℃; Sb(7 nm)/SiO_2(3 nm), T_c = 209℃; Sb(3 nm)/SiO_2(7 nm), T_c = 230℃; Sb(2 nm)/SiO_2(8 nm), T_c = 240℃). The value of $T_{10-year}$ of Sb(3 nm)/SiO_2(7 nm) materials reaches 168℃, and the value of Sb(2 nm)/SiO_2(8 nm) materials reaches 189℃. The reversible resistance transition is achieved by an electric pulse as short as 8 ns for Sb(3 nm)/SiO_2(7 nm). Compared with GST, the Sb(3 nm)/SiO_2(7 nm)-based PCM device has a lower power of 0.09 mW. The reversible switching of 3.0×10^6 cycles is achieved. The SLL Sb(3 nm)/SiO_2(7 nm) has a lower thermal conductivity of 0.13 W/(m·K). These results demonstrate that SLL Sb/SiO_2 materials are promising candidates for low power and high-speed PCM applications.

References

[1] Szkutnik P D, Aoukar M, Todorova V, Angelides L, Pelissier B, Jourde D, Michallon P, Vallee C and Noe P 2017 *J. Appl. Phys.* **121** 105301
[2] Zhu Y Q, Zhang Z H, Song S N, Xie H Q, Song Z T, Shen

L L, Li L, Wu L C and Liu B 2015 *Chin. Phys. Lett.* **32** 077302
[3] Lu Y G, Stegmaier M, Nukala P, Giambra M A, Ferrari S, Busacca A, Pernice W H P and Agarwal R 2017 *Nano Lett.* **17** 150
[4] Xia M J, Rao F, Song Z T, Ren K, Wu L C, Liu B and Feng S L 2013 *Chin. Phys. Lett.* **30** 037401
[5] Zhu C Q, Ma J, Ge. X M, Rao F, Ding K Y, Lv S L, Wu L C and Song Z T 2016 *Appl. Phys. Lett.* **108** 252102
[6] Mathias S, Hans W, Pál J, Yoshimi T, Tristan G A Y, Ivan K and Riccardo M 2016 *Sci. Rep.* **6** 27434
[7] Wang Q, Liu B, Xia Y, Zheng Y, Huo R, Zhang Q, Song S, Cheng Y, Song Z T and Feng S 2015 *Appl. Phys. Lett.* **107** 222101
[8] Hu Y F, Zou H, Zhang J H, Xue J Z, Sui Y X, Wu W H, Yuan L, Zhu X Q, Song S N and Song Z T 2015 *Appl. Phys. Lett.* **107** 263105
[9] Kim N H, Kim H K, Lee K M, Sohn H C, Roh J S and Choi D J 2011 *Thin Solid Films* **519** 5323
[10] He Z F, Wu P Z, Liu R R, Zhai J W, Lai T S, Song S N and Song Z T 2016 *CrystEngComm* **18** 1230
[11] Lu Y G, Song S N, Song Z T, Ren F, Wu L C, Zhu M, Liu B and Yao D N 2012 *Appl. Phys. Lett.* **100** 193114
[12] Zhu W L, Wen T, Hu Y F, Liu X Y, Gu D, Lai T S and Zhai J W 2017 *J. Alloys Compd.* **723** 936
[13] Loke D, Shi L P, Wang W J, Zhao R, Yang H X et al 2011 *Nanotechnology* **22** 254019
[14] Sandhu S, Kumar S, and Thangaraj R 2017 *Phase Transit.* **90** 1013
[15] Podpirka A, Lee W K, Ziegler J I, Brintlinger T H, Felts J R, Simpkins B S, Bassim N D, Laracuente A R, Sheehan P E and Ruppalt L B 2017 *Nanoscale* **9** 8815
[16] Guo T Q, Song S N, Li L, Ji X L, Li C, Xu C, Shen L L, Xue Y, Liu B, Song Z T, Qi M and Feng S L 2017 *Scr. Mater.* **129** 56
[17] Hu Y F, Zhu X Q, Zou H, Zhang J H, Yuan L, Xue J Z, Sui Y X, Wu W H, Song S N and Song Z T 2016 *Appl. Phys. Lett.* **108** 223103
[18] Rao F, Song Z T, Cheng Y, Xia M J, Ren K, Wu L C, Liu B and Feng S L 2012 *Acta Mater.* **60** 323
[19] Luo Y, Wang G X, Liu P, Wang Z L, Wang J X and Gu T 2017 *Vacuum* **141** 188
[20] Ji X L, Wu L C, Zhu M, Rao F, Song Z T, Hu Z G, Guo S, Xu L, Zhou X L and Feng S L 2015 *RSC Adv.* **5** 24966
[21] Hu Y F, Li S M, Lai T S, Song S N, Song Z T and Zhai J W 2013 *Scr. Mater.* **69** 61