Bias Dependence of Radiation-Induced Narrow-Width Channel Effects in 65 nm NMOSFETs *

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The bias dependence of radiation-induced narrow-width channel effects (RINCEs) in 65-nm n-type metal-oxide-semiconductor field-effect transistors (NMOSFETs) is investigated. The threshold voltage of the narrow-width 65 nm NMOSFET is negatively shifted by total ionizing dose irradiation, due to the RINCE. The experimental results show that the 65 nm narrow-channel NMOSFET has a larger threshold shift when the gate terminal is kept in the ground, which is contrary to the conclusion obtained in the old generation devices. Depending on the three-dimensional simulation, we conclude that electric field distribution alteration caused by shallow trench isolation scaling is responsible for the anomalous RINCE bias dependence in 65 nm technology.

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Scaling of the gate oxide in advanced technologies to thinner dimensions has eliminated the threshold voltage shift due to radiation induced charges trapped in the gate oxide.[1] Shallow trench isolation (STI) is thought to be the main issue when considering total ionizing dose (TID) effects for scale-down technologies.[2] TID-induced charges trapped in the lateral STI oxide induce a leakage path in NMOSFETs through parasitic transistors. Moreover, in a narrow-width channel device, the trapped charge in the STI sidewalls not only determines the threshold voltage of the lateral parasitic transistors, but also influences the electric field of the main transistor leading to a threshold shift, known as the radiation induced narrow channel effect (RINCE).[3–6] The RINCE plays a crucial role in TID responses of SRAM cells, because minimum or nearly minimum-geometry transistors are commonly used in SRAM cells.[7,8]

The threshold shift of narrow-width channel transistors induced by RINCE is bias-dependent. Bias dependences of RINCE for 180 nm and 130 nm NMOSFETs have been explored by Gaillardin *et al.*[3] and Gonella *et al.*[4] The experimental results show that NMOSFET biased ON during irradiation has a larger threshold shift than that biased OFF. Gate voltage leads to a strong electric field pointing to the Si-SiO_2 interface in the corner region between the gate oxide and STI under ON bias. More charges will be trapped in STI by the influence of the electric field pointing to the Si-SiO_2 interface, thus NMOSFET biased ON has a larger threshold shift. However, the conclusion derived from 180 nm and 130 nm technologies cannot apply to all technology nodes, because TID responses are closely associated with process conditions. Especially for nanometer devices, electric field distribution in STI will be altered by scaling of STI, which plays a key role in the bias dependence of RINCE. In this study, the bias dependence of RINCE in 65 nm MOSFETs is verified by the TID experiment. Interestingly, our experimental results show that the 65 nm narrow-channel NMOSFET has a larger threshold shift when the gate terminal is kept in the ground, which is contrary to the conclusion obtained in 180 nm and 130 nm NMOSFETs. A three-dimensional (3D) simulation is introduced to understand the mechanism of radiation effects under different bias configurations.

Table 1. Bias configurations during irradiation.

NMOSFET	ON	OFF	TG
V_D	0	V_{DD}	V_{DD}
V_G	V_{DD}	0	0
V_S	0	0	V_{DD}
V_{PWELL}	0	0	0

Elementary transistors were fabricated using a commercial bulk 65 nm process. An access NMOSFET of 6-T SRAM cell in process design kit (PDK) provided by foundry was chosen to explore the bias dependence of threshold shift induced by RINCE. The size of access NMOSFET is $W/L = 125\,\text{nm}/75\,\text{nm}$. The operating voltage is 1.2 V. Three different bias configurations were applied to the devices during irradiation: ON, OFF and TG. They are detailed in Table 1 where the bias applied to source, drain, gate, and Pwell terminals are referenced as V_S, V_D, V_G and V_{PWELL}, respectively. Transfer [I_{ds} (drain current)

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versus V_{gs} (gate to source voltage)] characteristics of transistors were measured by a Keithley 4200 parameter analyzer at room temperature. The threshold voltage of the transistor is extracted by the constant drain current ($I = (W/L) \times 10^{-7}$ A) method. The threshold voltage is evaluated as the gate voltage corresponding to the given current depending on the transistor size.[9] To eliminate the impact of differences between devices on conclusion, three devices were irradiated in every bias configuration and the 1σ error bar of the threshold shift was calculated. TID exposures were carried out with ^{60}Co gamma-ray in the Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy Sciences, with a dose rate of 299 rad(Si)/s.

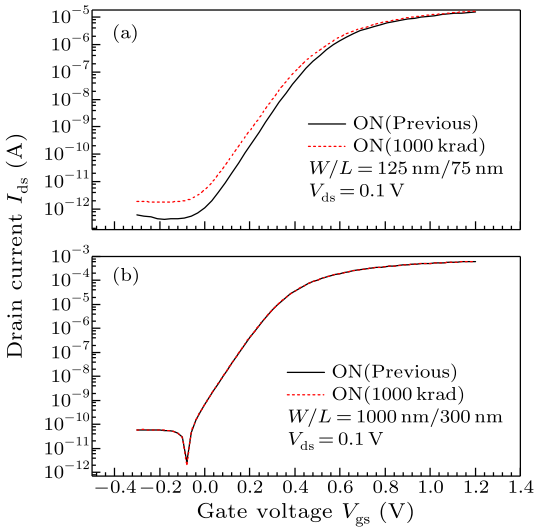

Fig. 1. The I_{ds}–V_{gs} curves for 65 nm NMOSFETs before and after 1000 krad(Si) of irradiation under ON bias: (a) narrow-width channel NMOSFET, and (b) wide-width channel NMOSFET.

Figure 1 shows the TID impact on the I_{ds}–V_{gs} characteristics of the 65 nm NMOSFET with different sizes. Obviously, a negative threshold shift is observed in the narrow-width channel NMOSFET, while the I_{ds}–V_{gs} curve of the wide-width channel device is unchanged after TID irradiation. The obtained experimental results agree with the previous studies of RINCE.

As shown in Fig. 2, at the STI corners, where the parasitic depletion regions ($X_{injection}$) meet the gate control depletion region (X_{dm}), the two regions overlap each other. The depletion charge under the gate is actually induced by the gate together with the two parasitic depletion regions, thus the channel charge can be considered to be 'shared' by the gate and charges trapped in the STI.[6] Threshold voltage of narrow-width channel NMOSFETs will be shifted by the above charge sharing, because $X_{injection}$ is comparable with W for them. Before irradiation, the charge Q_M (the total charge on the poly gate) balances Q_B (the total ionized impurity density in the depletion region). After irradiation, Q_n (TID induced charges trapped in STI) can also balance part, as shown in Fig. 2. Thus the charge that is needed to balance all the depletion charge is reduced. Consequently, the threshold voltage of the main transistor shifts negatively.

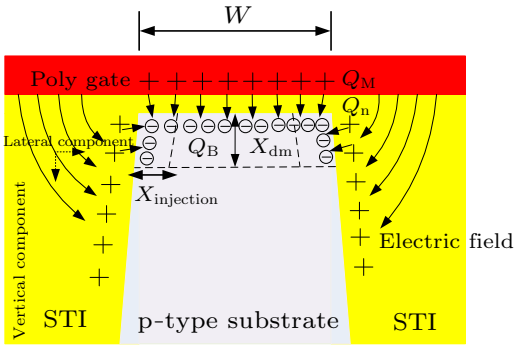

Fig. 2. Cross section of the NMOSFET under ON bias along the width.

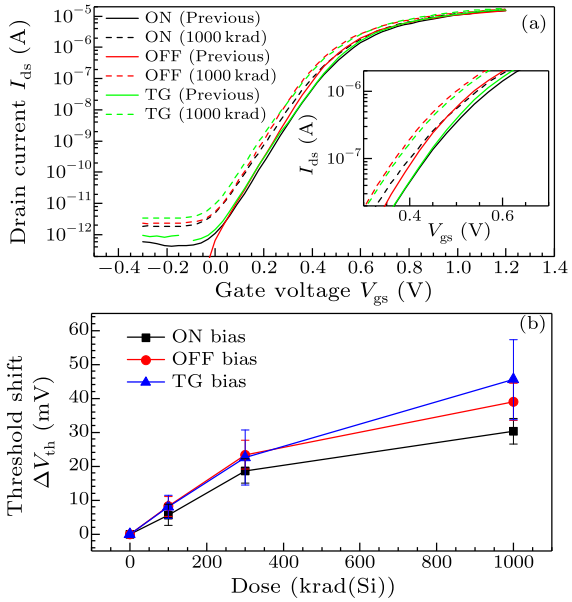

Fig. 3. Bias dependence of TID induced threshold shift in the 65 nm narrow-width channel NMOSFET. (a) The I_{ds}–V_{gs} curves before and after 1000 krad (Si) of irradiation under different bias configurations. (b) The extracted threshold shift from I_{ds}–V_{gs} curves changing with dose levels, with the error bar calculated by 1σ.

The bias dependence of TID induced threshold shift in the 65 nm narrow-width channel NMOSFET is shown in Fig. 3. As seen from Fig. 3(b), the 65 nm narrow-channel NMOSFET has a larger threshold shift when the gate terminal is kept in the ground (OFF and TG bias configurations). Previous works show that 180 nm and 130 nm NMOSFETs have larger threshold shift under the influence of an electric field pointing to the Si-SiO_2 interface when the gate terminal is kept in V_{DD}. The experimental results of this study reveal that the above analysis cannot apply to the 65 nm technology. In addition, the transistor un-

der TG bias has the largest threshold shift.

The mechanism of the anomalous bias dependence of threshold shift induced by RINCE in the 65 nm technology can be analyzed in two aspects. First, the vertical electric field component in STI is enhanced by the scaling of STI. Secondly, the electric field pointing from the drain or source to body is beneficial for charges trapped in STI under OFF and TG bias configurations.

The electric field in STI induced by the gate voltage under ON bias has both positive and negative influences on RINCE. Depending on the physical processes of the TID effect, we know that the position of trapped holes is controlled by the applied electric field. There are four major physical processes, which contribute to the radiation response of a CMOS device.[1] When radiation passes through a gate oxide, electron/hole pairs are created by the deposited energy. The second process is the transport of the holes to the Si-SiO_2 interface, and it is very sensitive to the applied electric field. Transport of the holes traces the electric field line. The third process is that when they reach the Si interface, some fractions of the transporting holes fall into relatively deep long-lived trap states. These trapped holes cause a remnant negative voltage shift. The fourth major component of the CMOS radiation response is the radiation-induced buildup of interface traps right at the Si-SiO_2 interface.

Because the electric field line in STI is circumferential, the electric field vector can be decomposed into a lateral component pointing to the Si-SiO_2 interface and vertical components pointing to the bottom of STI (seen in Fig. 2). On the one hand, TID induced charges are more inclined to be trapped near the Si-SiO_2 interface under the influence of the lateral electric field component pointing to the Si-SiO_2 interface,[10] having a larger effect on the threshold voltage of NMOSFET. On the other hand, TID induced charges will be pushed down and trapped in the bottom of STI by vertical electric field components coming from the positive gate bias,[11] where it has negligible influence on the threshold voltage shift. In general, the lateral electric field component plays a dominant role such that NMOSFET biased ON has a larger threshold voltage shift, as for 180 nm and 130 nm technologies. However, for the 65 nm technology, the vertical electric field component is enhanced by the scaling of STI, because it relies on the depth of STI. The depth of STI is decreased by the scaling of STI, but the supply voltage of device is not scaled in the same scale, thus the vertical electric field component is enhanced. In addition, the lateral electric field component is decreased by the scaling of the supply voltage, because it has no relationship with the size of STI. From the above analysis, we consider that the negative influence of the vertical electric field component will play a more important role in RINCE with the CMOS scaling.

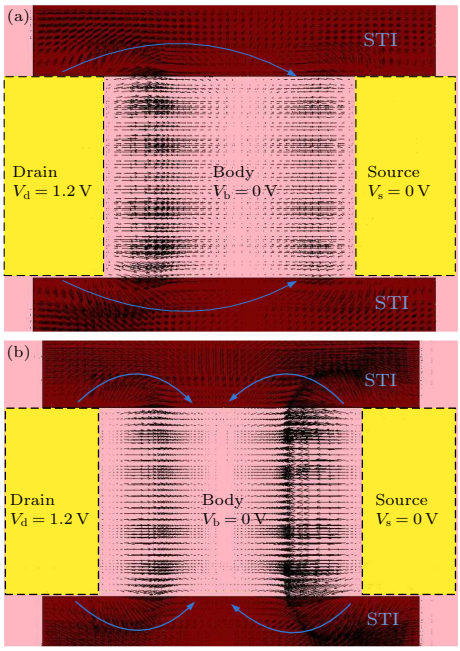

Fig. 4. Simulation of STI (deep red regions) electric field in the section from the drain to source of the transistor. Each black arrow represents a vector of total electric field. The direction of the electric field is indicated by blue lines with an arrow, since the direction of black arrows is hard to distinguish in the figure: (a) OFF bias, and (b) TG Bias.

Known from 3D TCAD simulation, the electric field in STI induced by the drain and source voltages is also relevant to the anomalous bias-dependence of the 65 nm NMOSFET threshold voltage shift. Figure 4 shows the simulation result of the electric field in the STI under OFF and TG bias. As for the OFF bias condition, the electric field line is pointed from the drain to the body through the STI region near the Si-SiO_2 interface resulting in an electric field pointing to the Si-SiO_2 interface. The above electric field induced by the drain voltage is beneficial for RINCE, since more TID induced charges will be trapped near the Si-SiO_2 interface. Due to the added impact of the source voltage, the STI electric field is larger under the TG bias than the OFF bias, indicating that the NMOSFET biased TG during irradiation has a larger threshold voltage shift. The above analysis is verified by bias dependence of the RINCE induced threshold voltage shift in NMOSFET.

In summary, we have presented the bias dependence of the RINCE induced threshold shift in the 65 nm technology. Contrary to old generation devices, our experimental results show that the 65 nm narrow-channel NMOSFET has a larger threshold shift when the gate terminal is kept in the ground. There are two reasons for the anomalous RINCE bias dependence of the 65 nm technology. First, the vertical electric field

component in STI is enhanced by the scaling of STI, and the lateral electric field component is decreased by the scaling of supply voltage, therefore less charge will be trapped in the upper region of STI. Secondly, there is an electric field pointing from the drain or source to the body in STI under OFF and TG bias configurations, which is beneficial for charges trapped in the Si-SiO_2 interface. The anomalous RINCE bias dependence should be considered in analysis of TID responses for circuits manufactured by the 65 nm technology.

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