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Ge Complementary Tunneling Field-Effect Transistors Featuring Dopant Segregated NiGe Source/Drain *

Junkang Li(李骏康), Yiming Qu(曲益明), Siyu Zeng(曾思雨), Ran Cheng(程然), Rui Zhang(张睿)**, Yi Zhao(赵毅)

College of Information Science & Electronic Engineering, Zhejiang University, Hangzhou 310027

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Ge complementary tunneling field-effect transistors (TFETs) are fabricated with the NiGe metal source/drain (S/D) structure. The dopant segregation method is employed to form the NiGe/Ge tunneling junctions of sufficiently high Schottky barrier heights. As a result, the Ge p- and n-TFETs exhibit decent electrical properties of large ON-state current and steep sub-threshold slope (S factor). Especially, $I_{\rm d}$ of 0.2 $\mu A/\mu m$ is revealed at $V_{\rm g} - V_{\rm th} = V_{\rm d} = \pm 0.5$ V for Ge pTFETs, with the S factor of 28 mV/dec at 7 K.

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Power consumption is becoming a fundamental problem for conventional Si metal-oxide-semiconductor field effective transistors (MOSFETs) with the increase in computational performance achieved by downscaling the dimensions of the MOSFET. Ge has been attracting interest as one of the high mobility channel materials for future MOSFETs, which could achieve a lower supply voltage ($V_{\rm dd}$) to keep the drive current constant, and thus the lower power density, compared with the Si MOSFET. Many efforts have been systematically focused on the issue of performance enhancement in the Ge MOSFET, including gate stack engineering, junction formation technique and device structure optimizing.[1–4] However, it is still difficult for MOSFETs to further scale down $V_{\rm dd}$ due to the minimum limitation of 60 mV/dec sub-threshold slope (S factor) at room temperature, arising from the thermionic carrier injection mechanism of the MOSFET. Alternatively, tunneling field effect transistor (TFET) could break through this bottleneck,[5–7] attributable to the quantum mechanical band-to-band tunneling (BTBT), which is considered to be one of the most promising candidates for low power logic devices. Nevertheless, Si TFETs still suffer from low ON-state currents since the indirect band gap and relatively large carrier effective mass of Si.[8–14] Ge is a promising channel material due to its narrower band gap and smaller carrier effective mass compared with those in Si.[15] Unfortunately, it is extremely difficult to fabricate Ge source/drain (S/D) junctions with steep doping profiles using the conventional techniques such as ion implantation. This phenomenon is attributed to the low solubility and the large thermal diffusion coefficients of dopants in Ge,[16,17] hence the severe degradation of S factors in Ge TFETs.

The NiGe Schottky junction is a promising S/D structure for Ge TFETs instead of the p–n junction, because the atomically sharp NiGe/Ge interface is beneficial to reduce the S factors in Ge TFETs.[18] Nevertheless, the Fermi levels of NiGe are usually pinned near the valence band side of Ge with a Schottky barrier height (SBH) of ∼0.3 eV for holes due to the metal-induced gap states.[19] This SBH of the NiGe/Ge junction is not sufficiently large for both hole and electron, thus inducing large amounts of junction leakage current and further degrading the OFF-state behaviors and S factors of NiGe metal S/D TFETs. Therefore, the realization of NiGe/p-Ge and NiGe/n-Ge Schottky junctions with large SBHs is the key issue to obtain superior NiGe metal S/D TFETs.

It has been reported that the SBHs in NiGe/Ge junctions can be modulated using the dopant segregation technique.[20–23] However, the effectiveness of these dopant segregated NiGe/Ge junctions serving as tunneling junctions in Ge TFETs is not yet clear, in spite of their importance. In this study, the Ge complementary TFETs have been demonstrated with the dopant segregated NiGe S/D structures. The small S factors of these devices indicate the feasibility of the dopant segregation technique in yielding superior Ge TFETs for the future low power CMOS technology.

To modulate the SBHs of NiGe/Ge junctions, the phosphorous and boron dopant segregations (P-DS and B-DS) were adopted, as shown in Fig. 1(a). The Ge p- and n-TFETs with the dopant segregated NiGe junctions were fabricated using a gate-last process (Fig. 1(b)). Subsequent to the pre-cleaning of the (100) p- and n-Ge substrates (resistivity: 1–10 Ω·cm), the 500-nm-thick SiO_2 was deposited using plasma enhanced chemical vapor deposition (PECVD) as field oxide and the active area was then defined by etching off the SiO_2. Afterwards, the dopant segregated S/D structures were achieved by ion implantation (phosphorous, 18 keV, 10^{15} cm^{-2} for P-DS and boron, 10 keV, 10^{15} cm^{-2} for B-DS), Ni deposi-

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**Corresponding author. Email: ruizhang@zju.edu.cn

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tion (30-nm-thick) and rapid thermal annealing (RTA) (400℃ for 1 min) in sequence. Following the removal of un-reacted Ni by HCl etching, the Ni/Al_2O_3 (10 nm)/GeO_x gate stacks (EOT∼6 nm) were fabricated by atomic layer deposition (ALD) and ozone post oxidation.[24] Finally, the Ni contact pads were formed by thermal evaporation. Here the NiGe metal S/D Ge pMOSFETs were also fabricated as control samples.

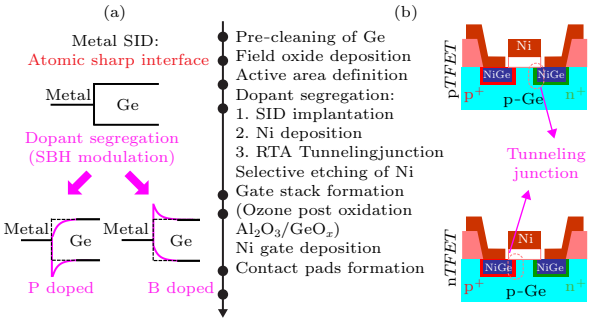

Fig. 1. (a) The band diagram of metal/Ge Schottky junctions after dopant (P and B) segregated modulation; and (b) the fabrication process and device structures of Ge p- and n-TFETs with DS NiGe metal S/D.

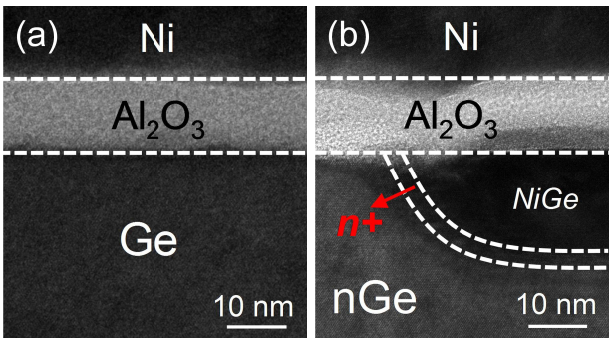

Fig. 2. The TEM images taken from the region of gate stack structure (a) and the source/channel edge (b) in the Ge TFET.

Figures 2(a) and 2(b) show the cross-sectional transmission electron microscopy (TEM) images taken from the channel region and the source/channel edge of a Ge pTFET. A smooth metal-oxide-semiconductor (MOS) interface and a 20-nm-thick NiGe junction can be confirmed for the Ge TFETs. The electrical properties of the dopant segregated S/D junctions were characterized, as shown in Fig. 3. It is found that the P-DS results in an Ohmic contact and the B-DS leads to a Schottky junction for NiGe/n-Ge. In contrast, for NiGe/p-Ge, the Schottky junction is formed by P-DS and the Ohmic contact is achieved using B-DS. The SBHs of B-DS NiGe/n-Ge and P-DS NiGe/p-Ge Schottky junctions were evaluated with the Arrhenius plots (Fig. 4).[25]

The significant linear $\ln(J/T^2) - (1/T)$ relationships in B-DS NiGe/n-Ge and P-DS NiGe/p-Ge junctions further confirm their feature of Schottky junctions. It is noted that the SBH for electron is 0.6 eV in the B-DS NiGe/n-Ge junction. Meanwhile, the SBH for hole is 0.69 eV in the P-DS NiGe/p-Ge junction.

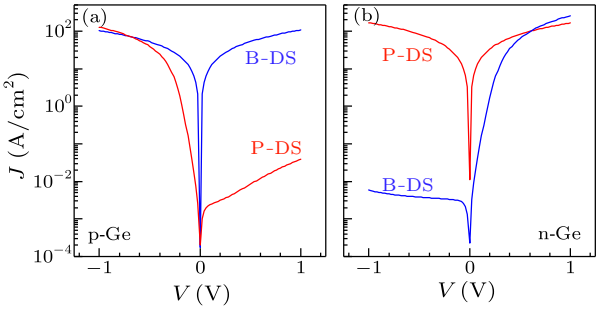

Fig. 3. The measured I–V characteristics of B-DS and P-DS NiGe/Ge Schottky junctions on p- (a) and n-Ge (b) substrates, respectively.

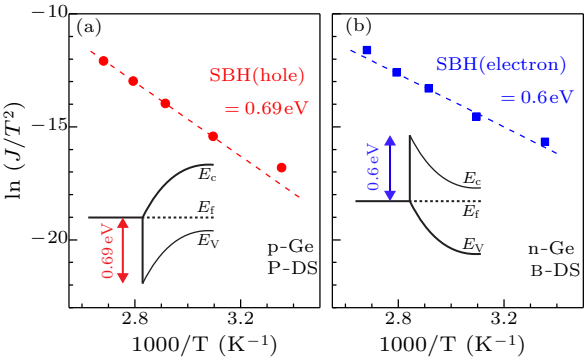

Fig. 4. The calculated Arrhenius plot of reverse bias current of B-DS and P-DS NiGe/Ge Schottky junctions on p- (a) and n-Ge (b) substrates, separately. The insets in (a) and (b) are the band diagrams of the B-DS and P-DS NiGe/Ge Schottky junctions, respectively.

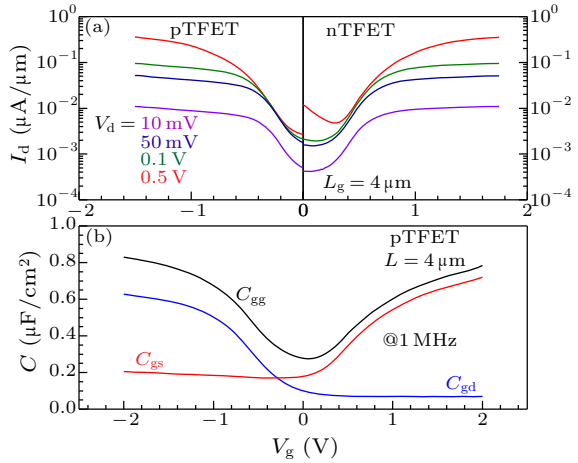

Fig. 5. (a) The measured I_d–V_g characteristics of Ge p- and n-TFETs with DS NiGe S/D. (b) The measured C–V behaviors (C_{gg}, C_{gd}, C_{gs}) of the Ge pTFET.

The n- and p-Ge substrates were used to fabricate the Ge p- and n-TFETs, respectively, in which the P-DS and B-DS NiGe/Ge junctions were employed as source and drain. Figure 5(a) shows the I_d–V_g characteristics of these devices (L_g = 4 μm). The normal operations are confirmed for both Ge p- and n-TFETs with the ON-state currents of ∼0.2 μA/μm at $V_g - V_{th} = V_d = \pm 0.5$ V and the ON/OFF ra-

tio of $\sim 10^3$. This decent TFET performance is attributable to the small carrier effective mass of Ge and the Schottky tunneling junctions with sufficiently high SBHs. In addition, the ON-state currents in the Ge p- and n-TFETs are independent of L_g (data not shown here), suggesting that the dominant current is tunneling through the Schottky barrier. The C–V behaviors (C_{gs}: gate-to-source capacitance, C_{gd}: gate-to-drain capacitance, C_{gg}: gate-to-channel capacitance) for a Ge pTFET were also investigated at the frequency of 1 MHz (Fig. 5(b)). The value of C_{gg} of the Ge pTFET is asymmetrically partitioned into C_{gs} and C_{gd}, which is a typical feature of TFET due to the asymmetric $n^+/n/p^+$ structure in the device.[26,27]

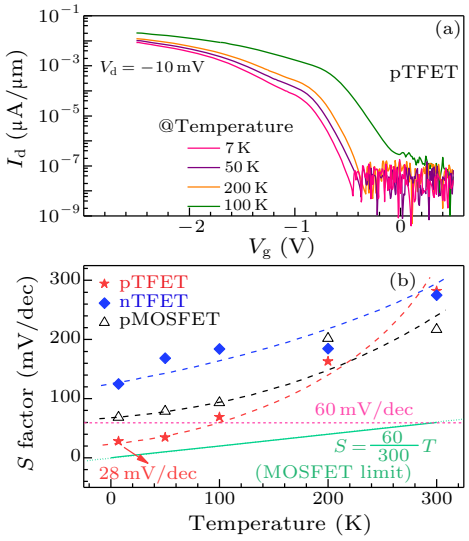

Fig. 6. (a) The temperature dependence of I_d–V_g characteristics for the Ge pTFET device. (b) The S factors of Ge p- and n-TFETs at different temperatures, compared with those in the Ge pMOSFET. T: temperature.

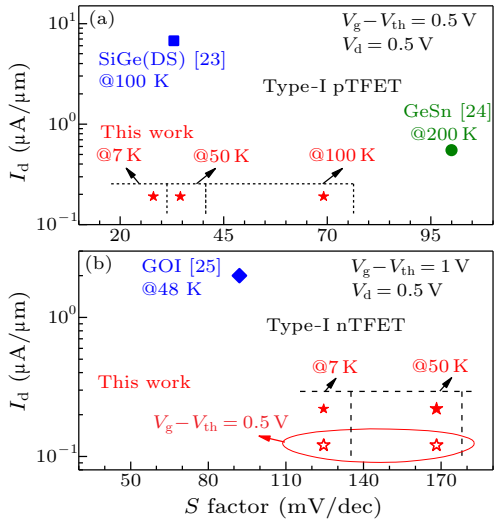

Fig. 7. Benchmarking of I_d and S factor for type-I planar p- (a) and n-TFETs (b) at low temperatures.

The low-temperature I_d–V_g curves were also examined for the Ge p- and n-TFETs. Figure 6(a) shows the I_d–V_g characteristics of a Ge pTFET device measured at $V_d = -10$ mV with the temperature ranging from 7 to 200 K. It was found that the OFF-state currents are significantly suppressed and the S factor is obviously decreased at a lower temperature. These phenomena suggest that the S factors of Ge TFETs are contaminated by the S/D junction leakage current and the further reduction of junction leakage current is effective to obtain a smaller S factor. Moreover, the decrease of S factor with the reduced temperature can also be attributed to the freezing of interface traps in the gate stack and NiGe/Ge tunneling junction. These interface traps may induce an increase in the trap-assisted-tunneling (TAT) current and severely degrade the S factors.[28,29] On the other hand, the ON-state current is also suppressed apparently at lower temperatures, which is mainly due to the suppression of TAT current and the increase of E_g in Ge. The S factors extracted from the I_d–V_g characteristics are summarized in Fig. 6(b) as a function of temperature. It is observed that the S factors for Ge pTFETs are 28 and 35 mV/dec at 7 and 50 K, respectively. The Ge pTFETs achieve much smaller S factors than Ge pMOSFETs at both room temperature and low temperature, indicating the feasibility of Ge pTFETs as candidates of future low power logic devices. It is also noted that the S factors in Ge nTFETs (120 mV/dec at 7 K, and 160 mV/dec at 50 K) are larger than those in Ge pTFETs, which is owing to the much larger interface trap density at the conduction band side than the valence band side for Ge MOS structures.[30]

Figures 7(a) and 7(b) benchmark the electrical properties of the type-I Si, Ge and GeSn p- and n-TFETs with the planar structure.[31–33] It is found that the Ge pTFET in this work exhibits I_{on} of $\sim 0.2\,\mu$A/μm at $V_g - V_{th} = V_d = -0.5$ V and the S factors of 28 and 35 mV/dec at 7 and 50 K. The S factor of 28 mV/dec at 7 K is the smallest value as compared with the reported results. Whereas the performance of Ge nTFETs with the dopant segregated NiGe S/D shows less superiority over the reference result including I_{on} and S factors, suggesting that the MOS interface passivation could be a key issue in yielding a superior Ge nTFET.

In summary, the Ge complementary tunneling field-effect transistors (TFETs) have been demonstrated using dopant segregated NiGe metal source/drain (S/D) structures. The Ge p- and n-TFETs exhibit the large I_{on} of $\sim 0.2\,\mu$A/μm at $V_g - V_{th} = V_d = -0.5$ V. Especially, the steep subthreshold slope of 28 mV/dec at 7 K is revealed for Ge pTFETs. These results indicate that the dopant segregated NiGe metal S/D is a promising structure for realizing the Ge TFETs with superior electrical properties.

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