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Temperature-Dependent Effect of Near-Interface Traps on SiC MOS Capacitance *

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A two-dimensional electrical SiC MOS interface model including interface and near-interface traps is established based on the relevant tunneling and interface Shockley–Read–Hall model. The consistency between simulation results and measured data in the different temperatures shows that this interface model can accurately describe the capture and emission performance for near-interface oxide traps, and can well explain the hysteresis-voltage response with increasing temperature, which is intensified by the interaction between deep oxide traps and shallow oxide traps. This also indicates that the near-interface traps result in an increase of threshold-voltage shift in SiC MOSFET with increasing temperature.

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Researchers have intensively studied 4H-SiC metal-oxide-semiconductor field effect transistors (MOSFETs) to replace conventional silicon devices in power switching applications owing to their high operating temperatures, high switching speeds, and normally-off operation characteristics.[1−5] They can be widely used in hybrid electric vehicles, photovoltaic (PV) inverters, power supplies uninterruptible power supply (UPS), industrial motor drives, traction, and wind turbine controls, and so on.[6−8] Though, SiC MOSFETs are beginning to be commercialized,[9] there are still a number of issues that need to be solved to improve the performance of SiC MOSFETs. The issues, attributed to the high density of SiC/SiO_2 interface traps and near-interface traps,[10,11] are a low inversion-channel carrier mobility[12] and threshold-voltage instability.[13,14] Due to the fact that the issue of low channel mobility has been solved by new processing techniques in recent years, the instability of the threshold voltage (V_{th}) is becoming the main issue for the applications of the SiC MOSFETs. Many studies were carried out for these issues, and it was thought that the shift of V_{th} is caused by oxide-trapped charges.[15] Lelis *et al.*[16] presented a two-way tunneling model, which depends on the electric field in the oxide and the distribution of charged and uncharged traps at a given spatial depth. Takuo and Ciappa built a two-dimensional TCAD model for studying the instability of V_{th}.[17] All the reported results show that the trapping and the releasing amounts of the oxide traps are directly proportional to the applied stress time and measured time, respectively. However, there are only a few investigations on the temperature-dependent effect of near-interface traps on the C–V characteristics. In this case, the current model cannot respond to the physical process of charge trapping and releasing under high temperature conditions and cannot explain the shift of V_{th} at high temperature. Hence, the establishment of a numerical simulation with the temperature-dependent effect of near-interface traps is necessary for better understanding the V_{th} shift of SiC MOS devices under high temperature.

In this Letter, a SiC MOS interface model containing oxide-traps and interface traps is established, and C–V characteristics are performed at high temperature. Compared with the numerical model reported in Ref. [17], a phonon assisted tunneling model is added, which influences the tunneling strength with different temperatures. Simulation results are in good agreement with experimental data, and the increase of hysteresis voltage (ΔV_{fb}) in C–V curves with temperature observed in the experiment could be explained by the trapping and releasing process of oxide traps.

The observed instability problems are due to charges trapping at and near the SiC/SiO_2 interface. Recently, results from density functional calculation (DFT) did show that the traps located in the oxide layer lie in a carbon-rich transition phase, which is several nanometers away from the interface.[18,19] As mentioned above, V_{th} instability is significantly affected by the near-interface traps. In this study, two types of near-interface oxide traps are considered in terms of their distances from the interface, in which shallow oxide traps are in a uniform distribution and deep oxide traps are in a single energy level. The main parameters of the traps used in the simulation are listed in Table 1. In addition, the distributions

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of interface traps are defined as the high-density exponential distribution below the conduction band and uniform distribution in the bandgap.[17]

Table 1. Main parameters used in the simulation model.

Trap location	Distance (nm)	Energy level (eV)	Concentration
SiC/SiO_2 interface (exponential)	0	0.1 (from SiC CB)	$5 \times 10^{12}\,cm^{-2}$
SiC/SiO_2 interface (uniform)	0	0.3 (from SiC CB)	$1 \times 10^{11}\,cm^{-2}$
Oxide (uniform)	1 (shallow)	2.0 (from SiO_2 CB)	$5 \times 10^{20}\,cm^{-3}$
Oxide (level)	3 (deep)	2.9 (from SiO_2 CB)	$5 \times 10^{20}\,cm^{-3}$

To simulate the capture and emission performances of the oxide traps, oxide is defined as the semiconductor, considering the Shockley–Read–Hall (SRH) recombination near the interface as well. The trap occupation dynamic processes near the interface are based on the relevant tunneling model from SiC to SiO_2.[17] In addition to the trap-assisted tunneling, the direct tunneling is involved during the electron injection into oxide. The tunneling probability Γ_C from the inversion layer at the position $z = 0$ (the interface of SiC/SiO_2) to an oxide trap at the position z is calculated from the solution κ of the Schrödinger equation under the Wentzel–Kramers–Brillouin (WKB) approximation at the position r and with energy E,[17] which is expressed as

$$\Gamma_C(z, E) = \exp(-2\int_0^z \kappa_C(r, E)dr). \quad (1)$$

The phonon-assisted tunneling process is also included to describe the temperature influence. The main parameters of phonon-assisted tunneling are listed in Table 2,[20] where S is the strength of the electron-phonon coupling. The mobile charges near the interface are affected by the condition of technology, which could not be obtained by fitting directly in the simulation and the shift of flat voltage in the CV curve is always equivalent to fixed charge density. Based on the technology now, the mobile charges are not considered, and fixed charges are used in this model with a concentration order of magnitude of $10^{12}\,cm^{-2}$.

Table 2. Phonon-assisted parameters.

Parameter	Symbol	Value	Unit
Huang Rhys	S	3.84	
Phonon energy	$\hbar\omega$	30	meV

In addition to the tunneling model, the model of carriers captured by the traps crossing the barrier of the MOS interface is considered using the Frenkel–Poole model, which is belonged to the thermionic emission model and related with temperature,[21] expressed as

$$J = CE_{ox} \exp\left[\frac{-q(\phi - \sqrt{qE_{ox}/\pi\varepsilon_i})}{\alpha kT}\right]. \quad (2)$$

Figure 1 shows the simulated MOS structure fabricated with oxidation at 1300° and post-oxidation annealing in NO atmosphere at 1175°. To measure the C–V characteristics, the scanning range of the applied gate voltage is from −10 V to 20 V with a sweeping up/down time of 30 s and a stress time of 1 s, respectively, as shown in Fig. 2. In addition, the range of temperature for the C–V measurement is from 300 K to 525 K.

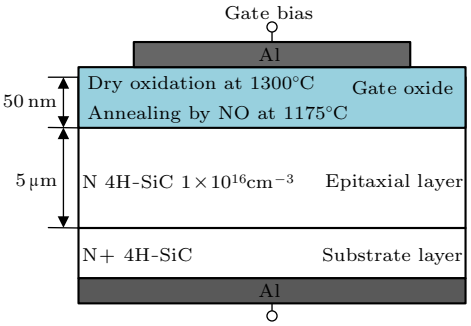

Fig. 1. The schematic diagram of MOS structure.

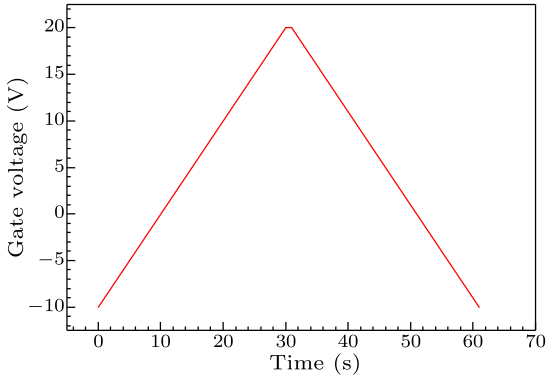

Fig. 2. Gate bias sequence.

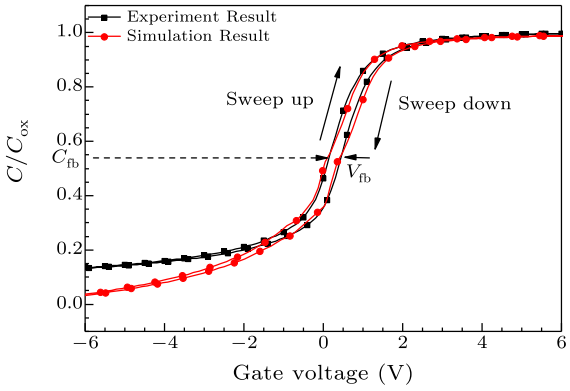

Fig. 3. The comparison between experimental and simulated C–V hysteresis curves at 300 K.

To verify the validity of the proposed model, C–

V characteristics of the fabricated MOS device are simulated at 300 K. The dispersion of the C–V characteristics is related to the fast interface traps. When the response times of the fast interface traps are quite to the ac signal in the CV test, different test frequencies lead to different interfacial capacitances. As the fast interface traps in this experiment are decreased by post-oxidation annealing in the NO atmosphere, the dispersions of C–V characteristics are almost unaffected by the frequency.[2] The simulations are carried out at the frequency of 10 kHz in this experiment. Figure 3 shows the comparison of simulated results with the experimental data. It can be seen from this figure that there is C–V hysteresis observed, and also simulated C–V curves are in good agreement with the experimental data, which proves the proposed model to be feasible. The near-interface oxide trap charges (Q_{NIOTs}) lead to the hysteresis and the interface trap charges (Q_{ITs}) cause the C–V curve extending along the gate voltage axis.

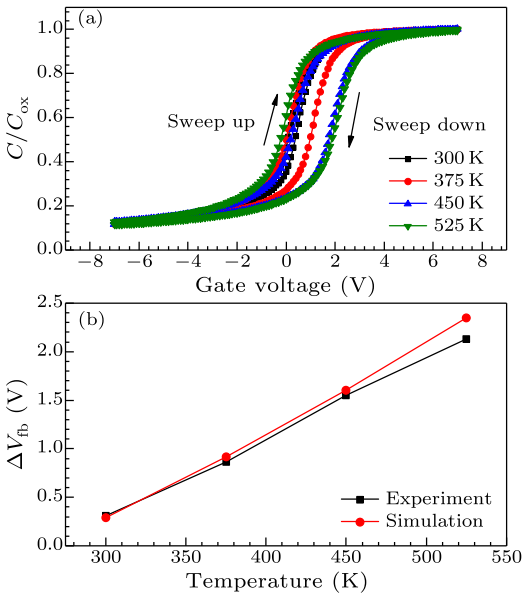

Fig. 4. (a) Experimental C–V curves under different temperatures, and (b) simulated and experimental results ΔV_{fb} versus temperature.

Figure 4(a) shows the normalized capacitance versus gate voltage with the temperature range from 300 K to 525 K. As shown in Fig. 4(b), $\triangle\ V_{\mathrm{fb}}$ is extracted from the experimental results in Fig. 4(a), the black solid square denotes the results from experiments and the red solid square presents the results from the simulations. It is clear that $\triangle\ V_{\mathrm{fb}}$ between the forward and backward C–V curve becomes larger from Fig. 4(b) as the temperature increases, which can be explained by Fig. 5. Figure 5 is Q_{NIOTs} including shallow oxide trap charges and deep oxide trap charges extracted from simulations.

Figure 5 is the relationship between Q_{NIOTs} and time, in which the shallow oxide trap charges and deep oxide trap charges are shown in Figs. 5(a) and 5(b), respectively. As temperature increases, the deep and shallow oxide traps capture more charges, but the shallow oxide trap charges are dominated. This is due to the fact that the thermal electron emission and tunneling effect are intensified at high temperature, which induce the oxide traps capturing more charges.

The part of shallow oxide trapped charges can be released in a short time while the deep oxide trapped charges cannot be released. However, the charging and discharging speed of shallow oxide traps cannot catch up with the scanning speed of dc voltage, leading to the left-right asymmetry in Fig. 5(a). The asymmetry is more obvious with the rising temperature, which causes the increase of hysteresis.

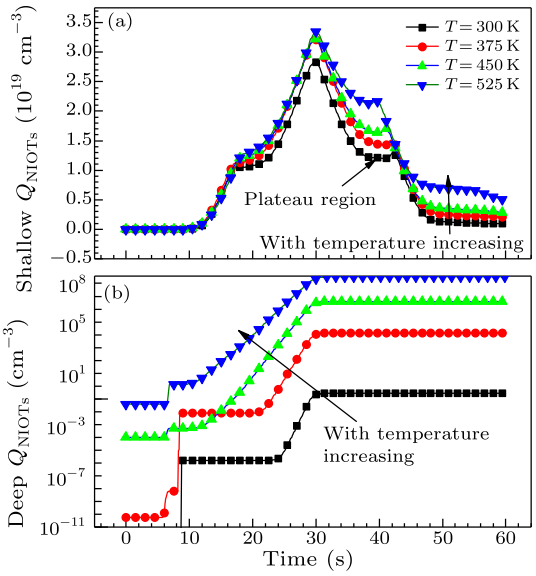

Fig. 5. The relationship between Q_{NIOTs} and time under different temperatures in simulation.

The dynamic balance between the capturing and releasing of the traps causes plateau regions to appear in Figs. 5(a) and 5(b). In addition, as the temperature rises, the width of the plateau decreases gradually. For shallow traps, it is easy to charge (swept-up stage) or discharge (swept- down stage) at a higher temperature. For deep traps, it can capture charges at a lower gate voltage, and the plateau region is influenced by the interaction of the deep and shallow traps.

The two kinds of near-interface oxide traps (the deep and shallow oxide traps) are settled to make the simulation model closer to the actual model. In an actual SiC MOS device, the charge will move to the deep oxide layer through trap-assisted tunneling and will be difficult to be released. The presence of deep oxide traps can describe this phenomenon. At a shorter stress time, shallow oxide traps are the main reason of flat-band voltage shifts. Deep oxide traps will in-

fluence on flat-band voltage at a longer stress times. Because the oxide charges are difficult to be released, flat-band voltage shifts caused by deep oxide traps are almost impossible to recover.

The agreement between the simulation and experimental results indicates that near-interface traps lead to the increase of threshold-voltage shift in the SiC MOSFETs with increasing temperature. Moreover, the interactions between oxide traps at different positions can further exacerbate the instability, which means that it is important to improve the process to reduce near-interface traps to enhance the stability of threshold voltage.

In summary, the temperature-dependent instability of SiC MOS devices has been studied by the C–V hysteresis curves, based on the proposed SiC MOS interface model with the interface SRH model and tunneling effect involving the influence of the near-interface trapped charges on the hysteresis voltages at different temperatures. The good agreement between simulation and experimental C–V results at different temperatures proves that this interface model can accurately describe the capture and emission procedures of near-interface oxide traps, and the increase of the C–V curve hysteresis-voltage measured with temperature rising has been well explained. From the simulation results, the main reason for the increase of C–V hysteresis voltage is that the oxide traps are more activated and the obvious asymmetry of capture and release for oxide traps appears as temperature increases, which is enhanced by the interactions between deep oxide traps and shallow oxide traps, leading to the increase of flat-band hysteresis voltage. This conclusion can also explain that the near-interface traps result in the increase of threshold-voltage shift in SiC MOSFETs with increasing temperature.

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