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Improved Operation Characteristics for Nonvolatile Charge-Trapping Memory Capacitors with High-κ Dielectrics and SiGe Epitaxial Substrates *

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A novel high-κ $Al_2O_3/HfO_2/Al_2O_3$ nanolaminate charge trapping memory capacitor structure based on SiGe substrates with low interface densities is successfully fabricated and investigated. The memory capacitor exhibits excellent program-erasable characteristics. A large memory window of ∼4 V, a small leakage current density of $\sim 2\times 10^{-6}$ Acm^{-2} at a gate voltage of 7 V, a high charge trapping density of 1.42×10^{13} cm^{-2} at a working voltage of ±10 V and good retention characteristics are observed. Furthermore, the programming ($\Delta V_{\rm FB}=2.8$ V at 10 V for 10 μs) and erasing speeds ($\Delta V_{\rm FB}=-1.7$ V at −10 V for 10 μs) of the fabricated capacitor based on SiGe substrates are significantly improved as compared with counterparts reported earlier. It is concluded that the high-κ $Al_2O_3/HfO_2/Al_2O_3$ nanolaminate charge trapping capacitor structure based on SiGe substrates is a promising candidate for future nano-scaled nonvolatile flash memory applications.

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With the continuous advance of modern electronics, the demand for nonvolatile memory rapidly grows. Memory devices with high program/erase speed and better endurance/retention characteristics are required for future nanoscale high-performance flash memory applications, especially in the 3D NAND flash memories.[1−5]

Among the family of nonvolatile flash memories, charge trapping memory (CTM) devices such as silicon-oxide-nitride-oxide-silicon (SONOS) type memory devices have attracted numerous attention for their lower power consumption, higher program/erase speed, improved retention and endurance characteristics as compared with their floating-gate counterparts.[2] However, the contradiction between program/erase speed and data retention is becoming much more serious with the scaling-down trend of device dimensions. Additionally, SONOS memory devices are susceptible to over-erase, in which the threshold voltage of the erased devices becomes more negative than the uncharged ones.

To confront the challenges faced by SONOS memories, high-κ dielectrics including Al_2O_3, HfO_2, HfAlO, etc. have been widely explored as the charge trapping layer (CTL) to replace oxide and nitride in the SONOS memory to achieve better performances.[2,3] Compared with nitride, the high-κ HfO_2 trapping layer can improve the P/E efficiency and can enlarge the programming window owing to its reduced equivalent oxide thickness (EOT) and higher charge-trapping density.[3] Furthermore, high-κ dielectric Al_2O_3 is chosen as the tunneling and blocking layers to enhance the electric field across the tunneling layer and to suppress the electric field across the blocking layer, thus leading to lower program/erase voltage and faster program/erase speed for the memory devices. The reduced electric field across the blocking oxide also resolves the over-erasing issue.

In recent years, poly-silicon (poly-Si) has already been adopted as the channel material for 3D vertical NAND flash applications.[4] However, poly-Si conduction is inhibited by scattering events at grain boundaries and charged defects, thus leading to degradation of device performance such as lower drive-current ($I_{\rm D}$) for reading operations and larger sub-threshold swing (SS). For the purpose of enhancing memory performances, such as higher program/erase efficiency and lower power consumption, high-mobility channel materials such as SiGe,[4] epi-Si[4] and InGaAs[5] have caused widespread concern and become alternative choices to replace current poly-Si channel for memory devices, owing to their high electron/hole mobility and tunable energy bandgaps. For instance, a strained pseudomorphic SiGe channel acting as a high mobility channel has attracted a great deal of interest and has been investigated for a long time. For programming, the drain current of flash memory devices can be significantly increased in virtue of the mobility enhancement from the strain effect of the SiGe channel. In addition, the bandgap of the SiGe channel can be modulated by tuning Ge contents. The electron/hole injection rate is exponentially inversely proportional to the SiGe band gap.[6] Thereafter, the tunneling current increases dramatically with the shrinkage of the SiGe band gap by increasing the Ge content in the SiGe channel. Furthermore, the tunneling electric-field strength for memory devices increases with the Ge content in the channel.[7]

Liu *et al.*[6] have reported charge-trapping flash memory devices with a SiGe-buried channel, and their experimental results proved to have a significant improvement on programming and erasing speed by employing the SiGe-buried channel. Moreover, Zhang *et al.*[8] have also investigated the remarkable charge-

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trapping behavior of $HfO_2/Al_2O_3/HfO_2$ multi-layered structure based on a molybdenum disulphide channel.

However, experimental studies on flash memory devices based on high-κ dielectrics and SiGe channel (not buried channel) are rarely reported. To further improve the performance for future nonvolatile memory, in this Letter we propose a novel memory structure with a combination of high-κ $Al_2O_3/HfO_2/Al_2O_3$ nanolaminate and SiGe channel. With the consideration of preventing electron back tunneling during erase operation, tungsten is chosen as the metal gate with a high work function of 4.6 eV. Furthermore, our fabrication processes are compatible with the modern flash memory technology. We mainly investigate the memory characteristics of the fabricated memory capacitors. As is expected, our fabricated capacitors exhibit high program/erase speed, a large memory window and excellent data retention characteristics.

In this work, the $[W/TiN]/Al_2O_3/HfO_2/Al_2O_3$ /SiGe MOSCAP is denoted by M-A-H-A-SG. This type of structure is based on the SONOS charge trapping memory structure.

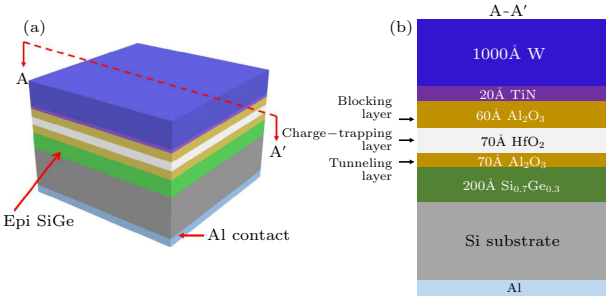

Fig. 1. (a) Schematic view of the capacitor fabricated on the SiGe substrate. (b) Schematic view of the cross-section of the M-A-H-A-SG capacitor structure.

M-A-H-A-SG capacitors with SiGe-buried channel, as shown in Fig. 1, were fabricated on p-type Si (100) wafer with resistivity of 8–12 Ω·cm. Prior to SiGe epitaxial growth, p-type wafer was cleaned by the standard RCA method, and the surface oxide was removed using a dilute HF 1% solution. Then a 20-nm-thick SiGe epi-layer with 30% Ge content was deposited by an ultra-high vacuum chemical molecular epitaxial (UHVCME) system. After SiGe epitaxial growth, a 3 nm Al_2O_3 film was deposited by atomic layer deposition (ALD) as the tunneling layer using $Al(CH_3)_3$ (TMA) and H_2O as precursors. Subsequently, the 7 nm HfO_2 film as the charge trapping layer was deposited by ALD using $Hf[N(C_2H_5)(CH_3)]_4$ (TEMAHf) and H_2O as precursors. Finally, another Al_2O_3 layer of 6 nm in thickness was deposited by ALD as the blocking layer. The ALD tool is TFS200 fabricated by Beneq, the reactor is cross-flow type, and N_2 was supplied as the purge and carrier gas. After the above processes, a post-deposition anneal was carried out at 450℃ for 15 s in a nitrogen atmosphere of 50 Torr to improve the quality of the dielectric films and to reduce the interface state densities. Then a 2-nm-thick TiN and a 100-nm-thick tungsten were deposited as the control gate electrode by ALD and patterned by a photolithography process. The backside of the Si substrate was coated with 700 nm aluminum for back contact after removal of native oxide by argon cleaning. After fabrication, the MOSCAPs were sintered in forming gas (5% H_2, 95% N_2) for 15 min. Control samples without HfO_2 layer were also fabricated using an identical procedure. The resulting structure is shown in Fig. 1.

Several identical test capacitors with square gate areas of 200×200, 100×100, $50 \times 50\,\mu m^2$ were used in this study.

Electrical capabilities including high frequency capacitance-voltage (C–V) hysteresis characteristics, constant current stress (CCS), program/erase speed, and retention time were measured by a Keithley 4200 semiconductor characterization system (Keithely 4200 SCS) in the air ambient at room temperature. In addition, the I–V leakage current characteristics were measured with an Agilent 4156C semiconductor analyzer.

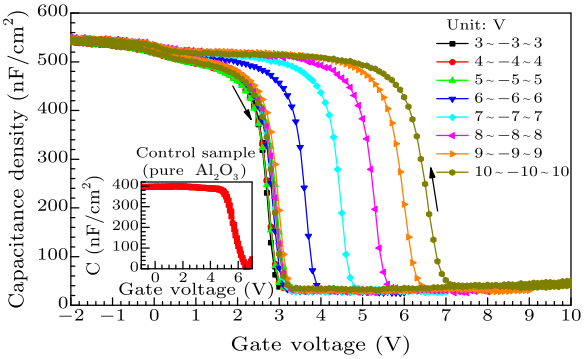

Fig. 2. High frequency (800 kHz) C–V curves of the memory capacitor under different gate voltage sweeping ranges. The inset shows the C–V curve of the control sample without the HfO_2 layer in the gate stack. The hysteresis feature of the control sample is negligible.

The C–V characteristics were measured in the parallel test mode at an AC signal frequency of 800 kHz. The sweep voltage step was set as 0.1 V and the voltage sweep speed was set as the normal speed mode. Figure 2 presents the capacitance-voltage (C–V) curves of the M-A-H-A-SG memory structure.

The C–V memory characteristics were measured by forward (from inversion (positive V_g) to accumulation (negative V_g)) and backward (from accumulation (negative V_g) to inversion (positive V_g)) voltage sweeps. During the forward voltage sweep, the capacitor undergoes a positive voltage stress at an initial sweep stage, which is equivalent to a program operation. In this status, electrons can tunnel through the Al_2O_3 tunneling layer via the mechanisms of Fowler–Nordheim (F-N) tunneling. Then the electrons will be trapped in the defects states of HfO_2 CTL, as shown in Fig. 4(a). The accumulation of electrons in HfO_2 CTL screens the top-gate electric field to reach the SiGe channel, thus leading to the positive shift of V_{FB}. During the backward voltage sweep, the capacitor undergoes a negative voltage stress at an initial sweep stage, which is equivalent to an erase operation, thus leading to a shift of the C–V curve to the reverse direction. In this status, the pre-trapped electrons in the CTL are transferred back to the SiGe substrate by the same F-N tunneling mechanism, also shown in Fig. 4(a). The different flat-band voltages under different operations can be defined as '1' or '0' for a memory device.

There is no obvious flat-band voltage shift in

the voltage sweep of ±3 V (defined as a quasi-neutral state), indicating that charge trapping and de-trapping hardly take place in this voltage sweep range, and the corresponding flat-band voltage is labeled as the initial flat-band voltage, which is defined as $V_{\rm FBN}$. From Fig. 2, an initial flat-band voltage of $V_{\rm FBN} = 2.9$ V is observed. When the voltage sweep range increases to ±6 V, the flat-band voltage shift is obvious. The memory window increases by increasing the sweeping gate voltages, as shown in Fig. 3(a).

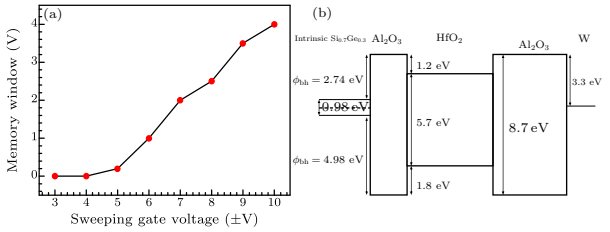

Fig. 3. (a) The memory window of the fabricated capacitor with different sweeping voltages. (b) Band alignments of the fabricated memory capacitor without external electrical field.

In a voltage sweep range of ±10 V, a large memory window of about 4 V can be obtained, as indicated in Fig. 3(a). However, after the sweeping voltage of −10 V–10 V is applied, the C–V curve is still on the positive axis. This means that holes can hardly tunnel through the Al_2O_3 tunneling layer and become trapped in the HfO_2 layer due to large valence band offset between SiGe and HfO_2 (∼4.98 eV in Fig. 3(b)). This could become a potential advantage to tackle the over-erase issue.

The energy band diagram of the implemented memory gate stack is illustrated in Fig. 3(b). The barrier height $\phi_{\rm Be}$ for electron injection from the SiGe channel to the HfO_2 layer is about 2.74 eV, which is slightly smaller than that of the normal Si-SiO_2 system (3.25 eV). This means that a higher charge tunneling probability and program efficiency have occurred in the studied memory structure. In addition, to show a better understanding of the memory characteristics, the energy band diagrams of the M-A-H-A-SG memory capacitor during programming and erasing operations are also depicted in Fig. 4(a).

It is crucial to demonstrate that the large memory window observed in Fig. 2 is mainly owing to the presence of large quantities of trap sites in the HfO_2 layer. In recent years, it has become clear that most of the charge trapping phenomena occurring into hafnium based dielectrics are related with oxygen vacancies.[9] To confirm that the memory effect is really from HfO_2, we have specifically fabricated an M-A-SG capacitor without the HfO_2 layer in the gate stack, and the corresponding hysteresis feature of the control sample shown in the inset of Fig. 2 is negligible within the voltage sweeping range of 7 V–−1 V–7 V, which demonstrates that the memory effect mainly comes from the HfO_2 charge trapping layer instead of defects in the Al_2O_3 layer or the interface states. From another point of view, interface state densities ($D_{\rm it}$) for our memory capacitor are comparatively low with the benefit of N_2 annealing after high-κ dielectrics deposition. It should be mentioned that the interface state densities for our memory capacitor can be estimated to be 3.4×10^{12} eV^{-1}cm^{-2} by the conductance method provided by Nicollian and Brews.[10] In addition, according to the experimental results reported by Ando *et al.*,[11] the interface quality of SiGe/Al_2O_3 could be significantly improved by *in-situ* O_3 treatment. We will continue our efforts to improve the interface quality between SiGe and Al_2O_3 gate stack.

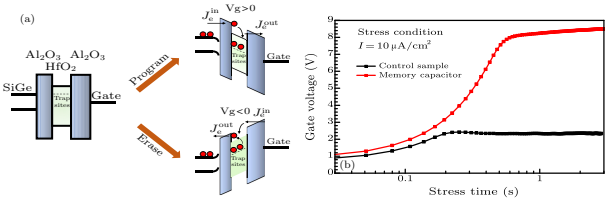

Fig. 4. (a) Energy band diagrams of the M-A-H-A-SG memory capacitor during programming and erasing operations. (b) Charge trapping characteristics for the M-A-H-A-SG memory capacitor and the control sample under constant current stress.

To further ascertain that the memory effect is primarily resulted from the HfO_2 layer, the constant current stress (CCS) method was carried out. Figure 4(b) shows the charge trapping characteristics of the M-A-H-A-SG memory capacitor. A constant current of 10 μA/cm^{-2} was applied to the gate electrode. The voltage drop at the gate stacked layer was measured as the gate voltage shift varied with increasing the stress time. The shift in gate voltage is attributed to the charge trapping in the HfO_2 trap layer. From Fig. 4(b), it can be found that the M-A-H-A-SG memory capacitor shows a large voltage shift and better charge trapping characteristics, while the control sample (M-A-SG) without the HfO_2 trap layer shows an insignificant voltage shift owing to slight charge trapping in the Al_2O_3 layer.

Thereafter, the equivalent oxide thickness (EOT) of the memory capacitor is calculated from

$$\mathrm{EOT} = \frac{\varepsilon_{\rm ox}}{C_{\rm total}}, \tag{1}$$

where $\varepsilon_{\rm ox}$ is the dielectric constant of SiO_2, $C_{\rm total}$ is the normalized capacitance in the accumulation region.[12] The EOT is found to be 6.2 nm. It is important to note that the small EOT of our memory capacitors possess great potential for future nanoscale nonvolatile memory device applications.

Or, EOT can be theoretically deduced precisely from the following equation[13]

$$\mathrm{EOT} = \frac{\varepsilon_{\rm OX}}{\varepsilon_{\rm Al_2O_3}} X_{\rm TL} + \frac{\varepsilon_{\rm OX}}{\varepsilon_{\rm HfO_2}} X_{\rm CTL} + \frac{\varepsilon_{\rm OX}}{\varepsilon_{\rm Al_2O_3}} X_{\rm BL}, \tag{2}$$

where $X_{\rm TL}$ (3 nm), $X_{\rm CTL}$ (7 nm) and $X_{\rm BL}$ (6 nm) represent the thickness of the tunneling layer, charge trapping layer and blocking layer, respectively, $\varepsilon_{\rm OX}$ (3.9), $\varepsilon_{\rm Al_2O_3}$ (7) and $\varepsilon_{\rm HfO_2}$ (25) correspond to the relative dielectric constants of SiO_2, Al_2O_3 and HfO_2, respectively. The calculated EOT by Eq. (2) is 6.1 nm, which is quite close to the value derived from Eq. (1).

The total width of the hysteresis curve is the sum of flat band shifts $\Delta V_{\rm FB}$ due to electron and hole trapping. Then the hysteresis memory window is defined as

$$\Delta V_{\rm FB} = V_{\rm FB}^{\rm forward} - V_{\rm FB}^{\rm backward}, \tag{3}$$

where $V_{FB}^{forward}$ is the flat-band voltage during forward voltage sweep (programming status), and $V_{FB}^{backward}$ is the flat-band voltage during backward voltage sweep (erasing status).

The charge trapping density of the memory capacitor can be estimated from[14]

$$N_t = \frac{C_{total} \times \Delta V_{FB}}{q}. \quad (4)$$

At the sweep voltage of ±6 V, ΔV_{FB} is 1 V. Here ΔV_{FB} at a gate sweep voltage of ±10 V is ∼4 V, and C_{total} is ∼570 nF/cm^2. A high charge storage density of ∼1.42×10^{13} cm^{-2} has been obtained, indicating that the HfO_2 charge trapping layer exhibits strong potential for multi-level data storage.

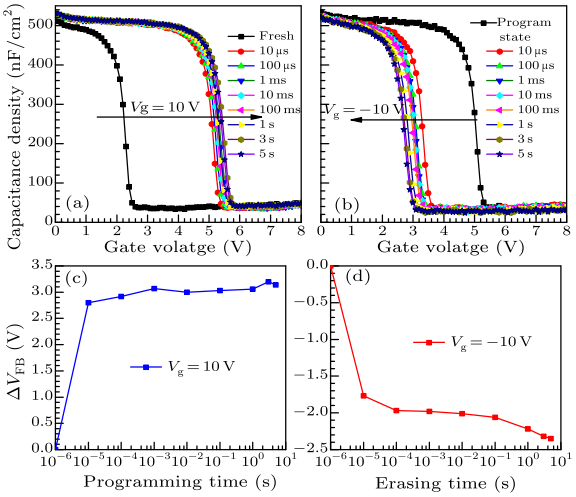

Fig. 5. (a) The C–V curves of M-A-H-A-SG capacitor as a function of programming time for a constant gate voltage of 10 V, (b) the C–V curves of the M-A-H-A-SG capacitor as a function of erasing time for a constant gate voltage of −10 V, and (c) programming transient and erasing transient characteristics of the M-A-H-A-SG capacitor.

The programming characteristics of the M-A-H-A-SG under a gate voltage of 10 V are shown in Figs. 5(a) and 5(c). The C–V curve exhibits a significant flat-band voltage shift (ΔV_{FB} = 2.8 V) in the positive direction after 10 μs programming. With prolonging the program time, a small increase in ΔV_{FB} is observed, which suggests that the electron trapping occurs dominantly within a program time of 10 μs. Compared with the programming characteristics reported by Liu *et al.*[6] ($t_{program}$ > 10 ms), our M-A-H-A-SG memory structure displays a faster programming efficiency. The improved programming efficiency comes from the electrical field enhancement in the tunneling layer by adopting Al_2O_3 instead of conventional SiO_2. Moreover, the erasing C–V curve exhibits the same fast erasing characteristics (ΔV_{FB} = −1.7 V after erasing at −10 V for 10 μs after programming at 10 V for 10 μs, as shown in Figs. 5(b) and 5(d). In summary, the enhanced P/E efficiency should be mainly ascribed to the high relative dielectric constant of HfO_2 (∼25) and Al_2O_3 (∼7), which results in a higher electric field across the tunneling oxide layer.[2,3] It should be mentioned that the field enhancement effect also comes from the surface SiGe channel.[7]

From Figs. 5(c) and 5(d), we also notice that the erase speed is slightly slower than the program speed. The asymmetrical program/erase characteristics can be ascribed to two reasons. According to band offsets of Al_2O_3 and SiGe in Fig. 3(b), the tunneling barrier height ϕ_{Bh} (4.98 eV) of the hole is larger than the electron tunneling barrier height ϕ_{Be} (2.74 eV), this will result in a smaller erase current than program current at the same gate voltage. Furthermore, the back tunneling of electrons from control gate (J_e^{in} at V_g < 0) during erase operation will also slow down the erase speed, as shown in Fig. 4(a).[15]

For non-volatile flash memory, the retention property and leakage current density are also very essential to evaluate their future prospects.[16]

Figure 6 shows the data retention characteristics of our M-A-H-A-SG memory capacitors. Firstly, the memory capacitor is programmed at a gate voltage of 10 V for 5 s. Then the capacitance is measured under sweeping gate voltages from +8 V to −5 V. The initial flat-band voltage is 5.7 V after the C–V measurement. The C–V curve has been measured with different time intervals, up to 1 × 10^4 s of retention time. To evaluate the erasing characteristic with retention time, the memory capacitor is again programmed at a gate voltage of 10 V for 5 s and then erased under a gate voltage of −10 V for 5 s. The capacitance is measured under a sweeping gate voltage from −5 V to 5 V. The initial flat-band voltage is 2.9 V after the C–V measurement. The C–V curve has also been measured with different time intervals, up to 1 × 10^4 s of retention time. The initial memory window is 2.8 V, and the initial memory window is reduced to 2.7 V after 10^4 s. A small charge loss of 3.5% after 10^4 s of retention is observed due to the excellent charge confinement of the A-H-A band structure.

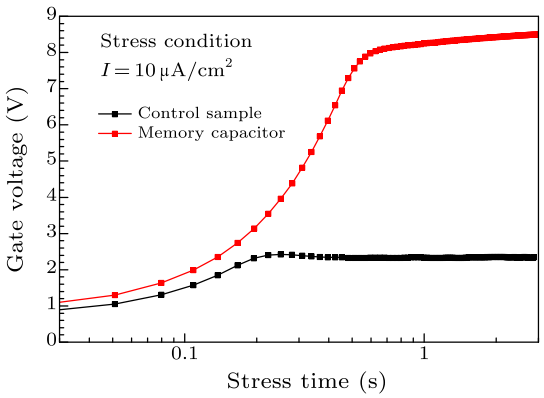

Fig. 6. The room-temperature retention characteristics of the fabricated memory capacitor.

Shi *el al.*[17] reported that the loss of trapped electrons in the CTL layer is possibly owing to the direct tunneling from the traps to the interface states, and the decrease in the interface states would consequently reduce the charge-loss rate. Thus the reduction of interface states between SiGe channel and Al_2O_3 gate stack is meaningful to improve the retention characteristics.

Figure 7 presents the I–V characteristics of the fabricated capacitor for various program times. It can be found that the memory capacitor programmed for 100 μs exhibits lower leakage current than the fresh one, especially in the range of 4–9 V. This is owing

to the extra energy barrier caused by the trapped electrons in the HfO_2 layer after the program,[18] which can be seen from the inserted band diagram in Fig. 7. Moreover, when the program time increases up to 100 ms, the reduction of leakage current is very small, indicating that a small quantity of electrons are trapped in the HfO_2 layer at the later stages of programming.

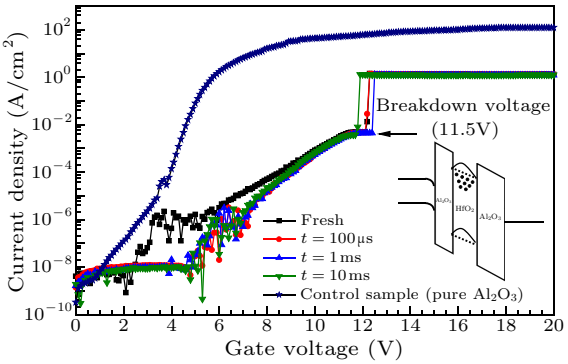

Fig. 7. The I–V curves of the memory capacitor under the program voltage of 10 V as a function of the program time and the control sample with a pure Al_2O_3 layer. The inset shows the band diagram corresponding to the fresh capacitor (dashed line) and the programmed capacitor (solid line) with trapped electrons (black dots).

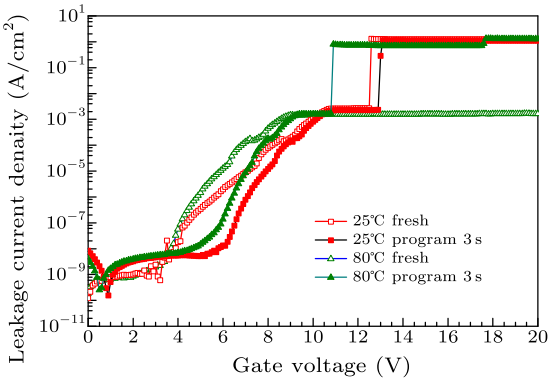

Fig. 8. Comparisons of gate leakage current of the fabricated capacitor under different temperature conditions.

After the capacitor is programmed with a pulse width of 10 ms, a small leakage current density of $\sim 2 \times 10^{-6}\,\mathrm{Acm}^{-2}$ at a gate voltage of 7 V is observed during the I–V sweep. Owing to the small gate leakage current, the retention characteristics can be improved for our memory structure. A high breakdown voltage of 11.5 V is also observed for all memory capacitors. When the memory capacitor breaks down, it reaches a current density of $1\,\mathrm{A/cm}^2$, where $1\,\mathrm{A/cm}^2$ is set as the compliance of the parameter analyzer. When the gate voltage is further increased to 9 V, the leakage current of the programmed capacitor is the same as that of the fresh capacitor. In this high gate voltage stage, the F-N tunneling takes place and becomes the dominant leakage current mechanism. The electrons are injected into the HfO_2 charge-trapping layer and trapped there within this high positive gate voltage, thus forming a virtual programmed capacitor. It is also believed that smaller current leakage should be realized by moderately increasing the thickness of the tunneling layer (Al_2O_3).

From Fig. 7, we can also find that the leakage current density of the memory capacitor is much smaller than the control sample. The reason lies in that the EOT of the high-κ dielectric layer in the memory capacitor is thicker than the control sample. Analogously, this observation was also reported by Qiu *et al.*[19]

When the I–V test temperature is increased to 80℃, the I–V curves shift to a higher current level at an elevated temperature, as shown in Fig. 8. During this high-temperature stage, the Schottky emission or thermal excitation may take place and become the dominant leakage current mechanism. However, under high-voltage range ($V_g > 10$ V), the F-N tunneling takes place and the leakage current is less dependent on temperature. This is ascribed to the weak temperature dependence of the F-N tunneling at this high electric field.[20] The leakage current is $8.8 \times 10^{-6}\,\mathrm{Acm}^{-2}$ at a gate voltage of 7 V under 80℃ I–V sweep, which is small enough to meet the requirements of current flash memory devices.

In summary, we have realized a novel memory capacitor structure based on SiGe channel and high-κ gate nanolaminate and found that all the memory capacitors exhibit the best memory characteristics. During the process flow, the interface state densities of the memory capacitor can be well controlled through a post-deposition anneal in nitrogen atmosphere. It is worth noting that the memory capacitor exhibits a large memory window of ~4 V, high program/erase speed and reliable charge retention property. Meanwhile, this kind of memory structure can suppress over-erase effectively. From measurements, it is confirmed that the high-κ dielectric HfO_2 layer acts as an effective charge-storage layer. Furthermore, the fabrication process is simple and fully compatible with conventional CMOS technology. In brief, this study provides a promising route of future nano-scaled flash memory operation, utilizing high-mobility channels and high-κ materials.

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