Total Ionizing Dose Response of Different Length Devices in 0.13 μm Partially Depleted Silicon-on-Insulator Technology *

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An anomalous total dose effect that the long length device is more susceptible to total ionizing dose than the short one is observed with the 0.13 μm partially depleted silicon-on-insulator technology. The measured results and 3D technology computer aided design simulations demonstrate that the devices with different channel lengths may exhibit an enhanced reverse short channel effect after radiation. It is ascribed to that the halo or pocket implants introduced in processes results in non-uniform channel doping profiles along the device length and trapped charges in the shallow trench isolation regions.

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Silicon-on-insulator (SOI) technology has great advantages over bulk substrates such as latch-up immunity, single event and transient radiation effects due to the complete dielectric isolation of transistors. However, the buried oxide (BOX) adds the sensitivity to total ionizing dose (TID) that radiation-induced charge will be trapped in this region. With device scaling, radiation-induced threshold voltage shifts in metal-oxide-semiconductor field effect transistors (MOSFETs) become negligible with gate oxides less than 5 nm in thickness,[1] because of less charges trapped in the thin oxide due to hole tunneling.[2] However, the shallow trench isolation (STI) for advanced commercial technologies will still be relatively thick and may still be very soft to ionizing radiation.[3] Hence, the existence of the thick BOX and STI makes the total ionizing effect of the SOI devices more complicated than its bulk-silicon counterpart.[4] Reduction of threshold voltage, otherwise called threshold voltage roll-off, which is one of short channel effects (SCEs), inherently exists with the dimensional downscaling of MOSFETs.[5] However, doping changes with device scaling down induce reverse short channel effect (RSCE) due to enhanced diffusion in MOSFETs of oxidation[6] or implantation damage.[7] For over a decade, most studies on SCEs focused on the normal application, studies on RSCE in application specific integrated circuits (ASICs) were not sufficient. In this Letter, we focus on the radiation responses along with the change of channel length in partially depleted silicon-on-insulator (PDSOI) n-type MOSFETs. Firstly, experimental results indicate that the long-length devices show an enhanced TID susceptibility. The 2D technology computer aided design (TCAD) process simulations show that the doping of mid-body is susceptible to the halo or pocket implants as device length scaled. Furthermore, the 3D TCAD process and device simulations are applied to investigate variants of the I–V characteristics by placing sheet charge in the STI and BOX interfaces. The results indicate that the short channel device tends to mitigate the sensitivity to TID due to higher body doping. In the end, the response of channel width was demonstrated by 3D TCAD simulations.

All the devices used in our experiments were fabricated in a 0.13 μm PDSOI Core NMOSFETs with DIP ceramic packaging. Processing was performed on a 200 mm diameter UNIBOND® wafer from SOITEC. The top Si film is 100 nm and the buried oxide is 145 nm. As shown in Fig. 1, the T-shape gate is introduced as the body contact. The STI connects with the BOX at the bottom for isolation. The gate oxide thickness is relatively thin about 1.8 nm and the operating voltage VDD is 1.2 V. Devices of four different channel lengths (L = 10, 1.2, 0.5 and 0.13 μm) with the same channel width (W = 10 μm) were selected as samples in our study. The experiments were conducted in Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences and ^{60}Co γ-ray was used as the radiation source. The dose rate was typically around 200 rad(Si)/s. During radiation exposure, the devices were under ON bias condition ($V_{\rm gate}$=VDD, $V_{\rm drain}$ = $V_{\rm source}$ = $V_{\rm body}$ = $V_{\rm substrate}$ = 0 V). The temperature was kept at room temperature. The I–V characteristics were measured by using a Keithley 4200B parameter analyzer before and after every irradiation step, such as 100, 300 and 500 krad(Si). All devices are tested under constant drain bias ($V_{\rm ds}$ = 0.1 V and 1.32 V). The times of measurements were limited in half an hour after exposure to avoid annealing.

Figure 2 shows the front gate I–V characteristic curves of T-shape gate devices with different channel lengths before and after ON bias radiation at low

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and high drain voltages ($V_{ds} = 0.1$ and 1.32 V). Interestingly, there is no obvious radiation-induced leakage current for all devices at 500 krad(Si). However, subthreshold hump which is known as the STI corner leakage[8] appears in the $W/L = 10/10$ transistor and becomes more significant with increasing the dose. It is worth noticing that subthreshold hump decreases gradually with the channel length scaling. As the channel length decreases to 0.13 μm, nothing changes in the front gate I–V characteristic curve. The most notable aspect of this result is that, contrary to the literature,[9–11] the long channel device is susceptible to TID.

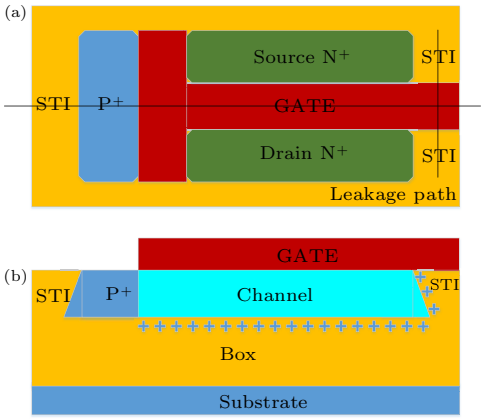


Fig. 1. (a) T-shape layout of PD SOI NMOSFETs with external body contact and (b) cross section illustration of the PD SOI NMOSFETs with STI joints with buried oxide.

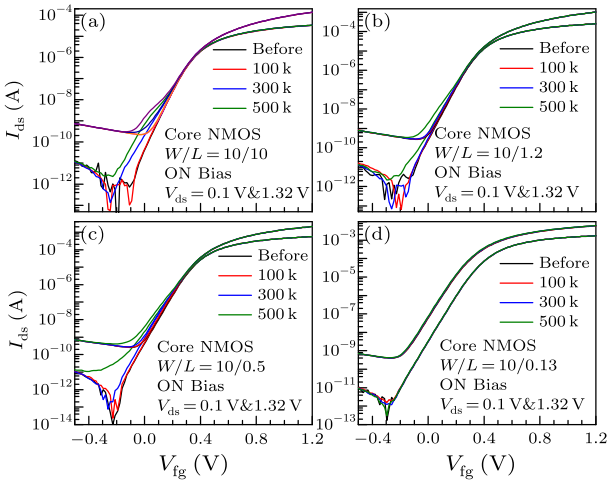


Fig. 2. Experimental front gate transfer characteristic curves of PDSOI core NMOSFETs with (a) $W/L = 10/10$, (b) $W/L = 10/1.2$, (c) $W/L = 10/0.5$ and (d) W/L=10/0.13 before and after ON bias radiation, respectively, at low and high voltages ($V_{ds} = 0.1$ and 1.32 V).

Figure 3 shows the front gate threshold voltage as a function of the channel length for various doses. The values of V_{TH} of the NMOSFETs are defined as a critical gate voltage as the drain current reaches $(W/L)\times10^{-7}$ A and the values of V_{TH} are extracted at the drain bias of 0.1 V. No noticeable threshold voltage shift is observed even when the total dose level is accumulated to 500 krad(Si) for the short channel device ($W/L = 10/0.13$). However, the long channel device ($W/L = 10/10$) shows a shift of 6 mV at the same dose. Since the gate insulator is very thin (<3 nm), a very small V_{TH} shift (<1 mV) would be expected with regard to the top gate stack.[12] Furthermore, the very small V_{TH} shift is due to the subthreshold hump which is related to trapped charge in the surrounding insulators. What is more, body doping concentration is also an important factor for TID response. Note that the well-known reverse short channel effect (RSCE) is shown in Fig. 3, which means that the longer channel devices have lighter body doping.

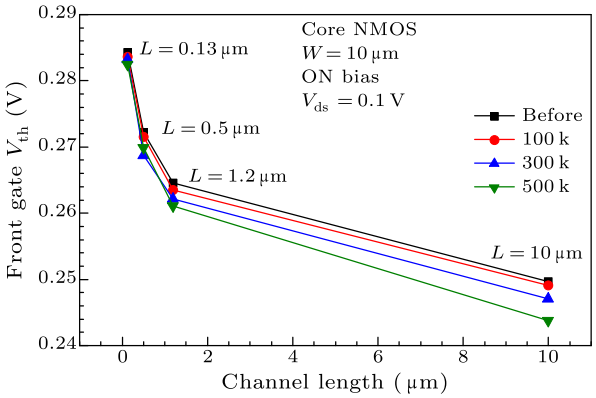


Fig. 3. Front gate threshold voltage as a function of the channel length for various doses.

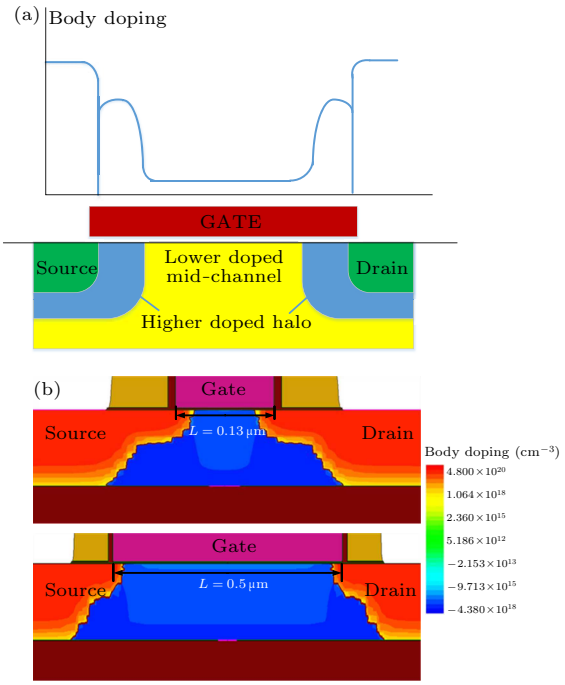


Fig. 4. (a) Illustration of non-uniform channel doping resulting from typical halo processes.[13] (b) The 2D cross section of the 0.13 μm gate length (top) and 0.5 μm gate length (bottom) devices. Here color and shapes represent doping.

The Sentaurus 2D simulator was performed to determine the influence of the channel length on the body doping. The process parameters were obtained from the foundry and applied to the structures with different channel lengths. The halo or pocket implants

are introduced in processes for improving scaling and controlling of short channel effect, which can result in non-uniform channel doping profiles along the device length as illustrated in Fig. 4(a).[13] The halo or pocket implants affect the mid-body region beneath the V_{TH} doping, and have less impact with increasing the channel. In other words, the body doping of a short channel is susceptible to the halo or pocket implants. Figure 4(b) shows the 2D cross section of both the 0.13-μm and 0.5-μm-long devices. Color and shades represent doping, and the lighter blue color can be seen as the lighter-doped body region. In the 0.5-μm-long device, the lighter blue region is more pronounced than the 0.13-μm one. The region of lighter doping requires a lower radiation-induced charge density to deplete even invert. Consequently, devices with lightly doped body show enhanced TID susceptibility.

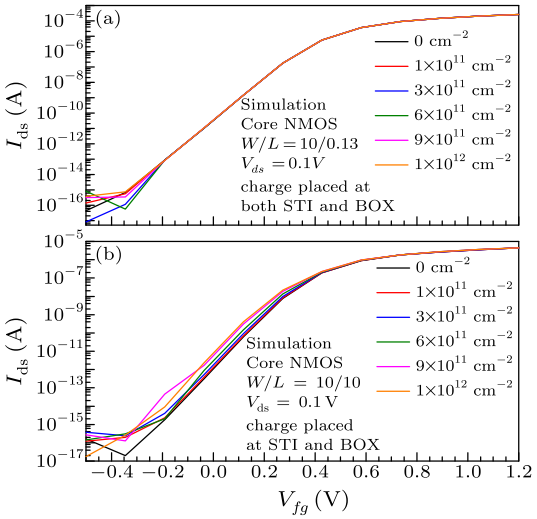


Fig. 5. The 3D TCAD simulations of uniform sheet charge placed at both the silicon/STI and silicon/BOX interfaces for (a) 0.13 μm and (b) 10 μm channel devices.

Sentaurus 3D TCAD device simulations were performed to investigate the impact of trapped charge in the STI and BOX. The 3D structures were constructed according to the process flow by Synopsys Sprocess. The same process parameters were applied to both the short (L = 0.13 μm) channel and long (L = 10 μm) channel devices. Both the STI oxide and the buried oxide can possibly affect the TID response in SOI transistors. Thus uniform sheets of charge were placed at the top silicon/BOX and the top silicon/STI interfaces as shown in Fig. 1(b) to evaluate the relative impact of radiation-induced charge on the front gate transfer characteristics of devices. Figure 5 shows the simulated results of the 0.13 μm and 10 μm channel length devices. Comparing the two cases, the longer channel device shows more sensitivity to the interface charge due to the lighter body doping. Figure 5 just takes into account the sheet charge distributed at the silicon/BOX and the silicon/STI interfaces uniformly. However, the actual distribution of radiation-induced charge is a very complex function of material properties (trap densities in the oxides) and bias (electrical field).[14,15] The trapped charge trends to be placed at an area with a high electric field. Hence, it is a critical issue to distinguish degradation between STI-related and BOX-related in SOI technology under different bias conditions.

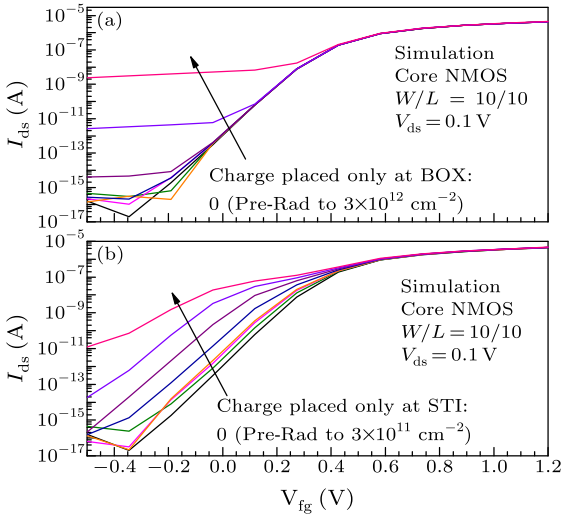


Fig. 6. The 3D TCAD simulations of uniform sheet charge placed at (a) only the silicon/BOX and (b) silicon/STI interfaces for W/L = 10/10.

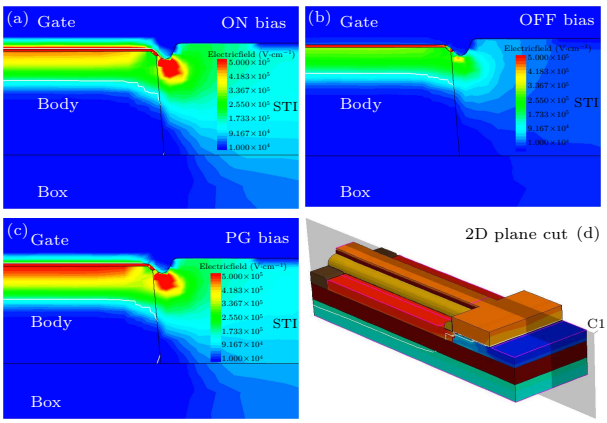


Fig. 7. Pre-Rad 3D TCAD simulations of electric field magnitude under (a) ON bias, (b) OFF bias and (c) PG bias. The 2D cut is taken along the device width at the same plane shown in (d).

To evaluate the relative sensitivity of the STI and BOX, simulations were performed placing the sheet charge at only the STI or BOX interfaces for the lighter doping device (W/L = 10/10). The simulated results are exhibited in Fig. 6, and the variation trends with increasing charge for two cases are obviously different. The increasing BOX charge just makes leakage grow quickly while the STI charge causes a true V_{TH} shift, and then increases leakage at high charge density. As mentioned above, the distribution of trapped charge strongly depends on the electric field. Generally, the irradiation bias conditions are consistent with transistors in digital circuits, corresponding to on-state (ON, the gate is VDD with other terminals grounded) and off-state (OFF, the drain is VDD with other terminals grounded) in inverter gate and transmission-gate (PG, the drain and source are VDD with other terminals grounded) like access transistors

in memory cells. Figure 7 shows the simulated electric field magnitude for the ON, OFF and PG biases. It can be clearly observed that the field distributed in the top half of the silicon and STI is strongest, whereas the field in the lower portion of the STI and the top BOX near the body is weaker for all irradiation bias cases. Hence, we can infer that the radiation-induced charges are mainly trapped near the top half of STI. Additional insight into the worst bias for the STI can be gained by comparing the relative electric field strength in all bias cases before irradiation. The electric field strength of the ON bias case is the strongest, then the PG bias, finally the OFF bias. This result indicates that the ON bias is the worst case for the STI, which is consistent with the published results.[15] Figure 8 shows the simulated transfer characteristic curves for the lighter device ($W/L = 10/10$), whose sheet charge density of 1.5×10^{12} cm^{-2} is placed at only the top half of the STI sidewalls, the bottom half of the STI sidewalls and the entire STI sidewalls. These results indicate that the response of the upper portion of the STI is most sensitive to trapped charge, which is further supported by Fig. 7.

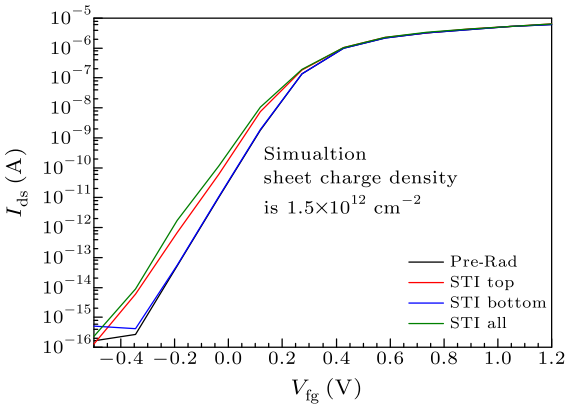


Fig. 8. The 3D TCAD simulated results of $W/L = 10/10$ device with sheet charge density placed at different areas, including only the top half of the STI sidewalls, the bottom half of the STI sidewalls and the entire STI sidewalls.

It is well known that the trapped charge will have a strong impact on the response of the narrow width device. The 3D TCAD devices of $W/L = 0.15/1.2$ and $W/L = 1/1.2$ were performed to investigate the impact of width on the radiation response. The sheet charge density of 2.5×10^{12} cm^{-2} is placed at only the silicon/STI interface, the silicon/BOX interface and both. As shown in Fig. 9, the wide device shows the higher saturation current as expected in all the cases and the higher leakage current in the pre-radiation curve. For the STI charge case, both wide and narrow devices show higher leakage than pre-radiation, whereas the narrow one shows a larger $V_{\rm TH}$ shift. For the BOX charge case, the simulated result is unexpected in that the wide device shows higher leakage though the body doping is the same as the narrow one. This result may be related to the pre-radiation case that the wide device also shows a higher subthreshold current. There is an interesting phenomenon that the leakages of the wide and the narrow devices are overlapped under the stronger compound effect of the STI and BOX charges, which makes the devices trend to fully depleted.

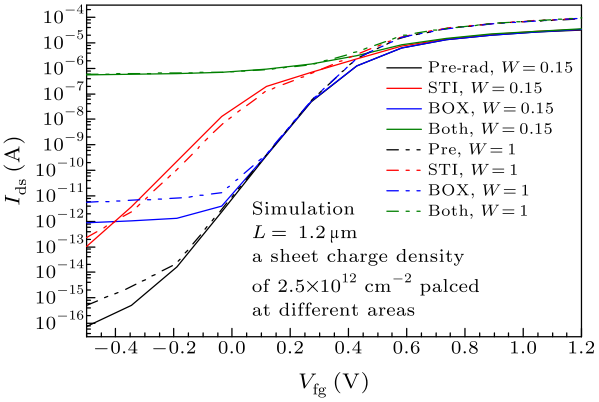


Fig. 9. Simulated results of pre-rad, charge of 2.5×10^{12} cm^{-2} trapped at the STI only, the BOX only, and both the STI and BOX interfaces for $W/L = 0.15/1.2$ and $W/L = 1/1.2$ devices.

In summary, the sensitivity to TID of 0.13 μm PDSOI NMOSFETs increases with the device length. The TCAD simulated results indicate that, due to the halo or pocket implants, the mid-body doping of the long device is lighter than the short one, resulting in non-uniform channel doping profiles along the device length. The charge trapped only at the Silicon/BOX interface will increase leakage, whereas the charge only at the STI sidewalls will cause a $V_{\rm TH}$ shift, which is dominated by the charge trapped in the upper region. The trapped charge in the upper region of STI can couple to the front channel and can produce a stronger impact on the I–V curve. The presence of charge at both interfaces has a compound effect that the BOX charge may imply the impact of the STI charge. In practice, the response of single transistor to TID is dependent on physical dimensions, irradiation bias, body doping levels and trap densities in the insulators.

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