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Experimental I–V and C–V Analysis of Schottky-Barrier Metal-Oxide-Semiconductor Field Effect Transistors with Epitaxial $NiSi_2$ Contacts and Dopant Segregation *

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We present an experimental analysis of Schottky-barrier metal-oxide-semiconductor field effect transistors (SB-MOSFETs) fabricated on ultrathin body silicon-on-insulator substrates with a steep junction by the dopant implantation into the silicide process. The subthreshold swing of such SB-MOSFETs reaches 69 mV/dec. Emphasis is placed on the capacitance-voltage analysis of p-type SB-MOSFETs. According to the measurements of gate-to-source capacitance C_{gs} with respect to V_{gs} at various V_{ds}, we find that a maximum occurs at the accumulation regime due to the most imbalanced charge distribution along the channel. At each C_{gs} peak, the difference between V_{gs} and V_{ds} is equal to the Schottky barrier height (SBH) for $NiSi_2$ on highly doped silicon, which indicates that the critical condition of channel pinching off is related with SBH for source/drain on channel. The SBH for $NiSi_2$ on highly doped silicon can affect the pinch-off voltage and the saturation current of SB-MOSFETs.

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Schottky-barrier metal-oxide-semiconductor field effect transistors (SB-MOSFETs) with metallic contacts are expected to have lower parasitic source/drain (S/D) resistances.[1] Since it is easy to form with a silicon compatible process, silicide has been used as an alternative of doped S/D junctions.[2−11] NiSi has been widely employed for SB-MOSFETs.[12−18] However, thicker NiSi contacts at S/D cause large encroachment of NiSi into the channel due to the fast diffusion of Ni in Si, which hinders down scaling of SB-MOSFETs. Ultrathin silicides may be a solution as they show greatly improved line edge uniformity.[19] Furthermore, epitaxial silicides, which form atomically flat silicide/silicon (111) aligned interfaces along ⟨110⟩ directions even over a few micrometers, provide uniform contacts at S/D.[20]

The performance of SB-MOSFETs is strongly dependent on the Schottky barrier height (SBH). A large SBH degrades the device performance resulting in low on-current, poor subthreshold swings and ambipolar switching. Therefore, low SBHs should be used to improve the device performance. SBH amounting to 0.65 eV for NiSi on n-Si and 0.35 eV for epitaxial $NiSi_2$ were achieved experimentally.[21−24] To reduce the effective SBH, dopant segregation (DS) at source and drain were applied.[25−31] The scaling behavior and improved properties of SB-MOSFETs caused by dopant segregation using the implantation into the silicide (IIS) method have been characterized.[32,33] However, the impact of dopant segregation on the capacitance of SB-MOSFET is still missing and unclear.

In this Letter, we present the experimental results of long channel SB-MOSFETs on ultra-thin body silicon-on-insulator (SOI) substrates with boron segregation using the IIS method. Particular emphasis is placed on the capacitance-voltage (C–V) characterization of devices. The gate-to-source capacitance C_{gs} and gate-to-drain capacitance C_{gd} with respect to V_{gs} at different frequencies and various V_{ds} are measured and analyzed.

In experiment, the SB-MOSFETs were fabricated on 20-nm-thick SOI substrates with a 145 nm buried oxide (BOX) layer. The schematic device structure and main process steps are shown in Fig. 1(a). After mesa isolation and RCA cleaning, a 5-nm-thick HfO_2 layer as gate dielectric was grown by atomic layer deposition (ALD), followed by atomic vapor deposition (AVD) of 60 nm TiN as the metal gate. The gate was defined with the length varied from 11 μm to 3 μm by optical lithography. The UV6^{TM} positive DUV photoresist was used in the photolithography process. The photoresist was spin coated on the sample at a rotation speed of 4000 rpm, thus the thickness of the photoresist was about 1 μm. The exposure intensity was 3.8 mW/cm^2 and the exposure duration is 5.6 s. The exposed portion of the photoresist was dissolved in the Megaposit MF24A Developer for 45 s. The exposed area was etched back to the sili-

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con using dry and wet etching. After gate patterning, an ultrathin Ni layer of about 2.7 nm was deposited by sputtering on the clean and oxide-free Si surface. Silicidation was performed in forming gas (N_2/H_2) at 700℃ for 30 s to form single crystalline $NiSi_2$,[19] while the excessive Ni was removed by a selective wet etching in diluted H_2SO_4. After silicidation, boron ions were implanted into source and drain at 1.5 keV to a dose of $2 \times 10^{15}\,\mathrm{cm}^{-2}$ with the angle of 45° and 135°, respectively. During a short rapid thermal annealing (RTA) at 500℃ for 10 s boron dopants diffuse to the silicide/silicon interface, generating a steep source/channel and drain/channel junction by DS. Finally, a 5 nm adhesion layer Cr followed by 150 nm Pt was deposited as metal contacts for the source, drain and gate. The microstructure of the fabricated device was characterized by a cross-sectional transmission electron microscope (TEM). The TEM image of the source/channel junction, as shown in Fig. 1(b), indicates good gate alignment without encroachment of silicide into the channel region. Figure 1(c) shows the TEM image of the semiconductor/insulator interface. The uniform and flat Si/HfO_2 interface layer reveals the good interface quality.

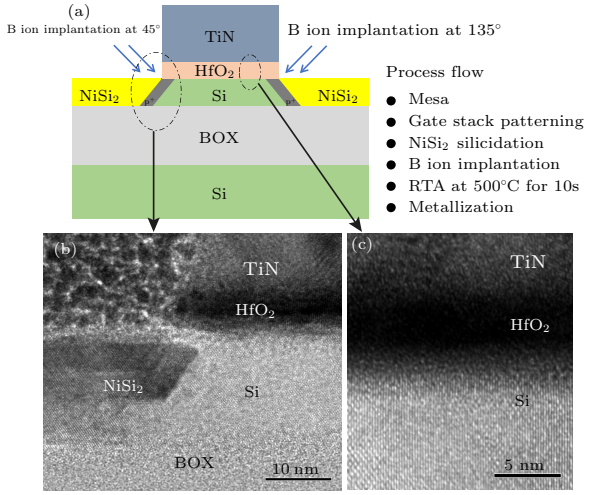

Fig. 1. (a) The schematic structure and main process flow of the fabricated SB-MOSFETs. (b) TEM cross-sectional image of source/channel junction. Ultrathin Ni layer deposited and single crystalline $NiSi_2$ was formed by silicidation with no encroachment into the channel region. (c) TEM image of the semiconductor/insulator interface showing the good interface quality.

The schematic band diagram of an SB-MOSFET with and without boron segregation is shown in Fig. 2. The band of the channel bends upward strongly at the interfaces of silicon and silicide due to the highly boron doped segregation pocket. The Schottky barrier of p-type silicon and silicide became much thinner and the effective SBH for holes was lower than that of intrinsic silicon and silicide junction. Thus the extremely thin SB is almost transparent to the carriers, and the device behaves as a conventional MOSFET.

Due to the different band bendings between the devices with and without DS as shown in Figs. 2(a) and 2(b), the ambipolar behavior is significantly suppressed. For example, when V_{gs} is positive, electrons inject into the conduction band by tunneling through the Schottky barrier at the drain contact, resulting in a much less electron current because of a higher barrier in the DS case (as shown by the green arrow in the figure). Reducing V_{gs} to values in the subthreshold regime, the injection of electrons from the drain is suppressed and the injection of holes from the source by thermionic emission is enabled. Thus the subthreshold slope in this regime is close to the thermal limit of 60 mV per decade. With a further decrease of negative V_{gs}, holes inject into the valance band by tunneling through the Schottky barrier at the source contact, resulting in a much higher holes current because of a thinner barrier in the DS case (as shown by the red arrow in the figure).

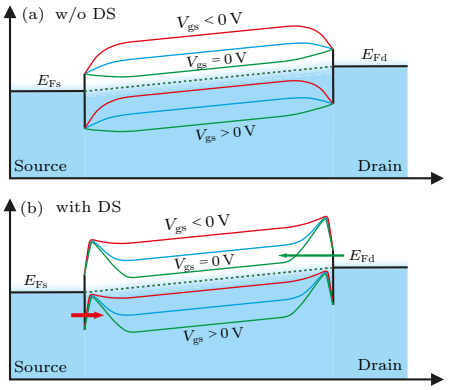

Fig. 2. Schematic views of (a) the band diagram of an SB-MOSFET at different gate-voltages without DS. (b) The band diagram of fabricated SB-MOSFET at different gate-voltages with DS. The highly boron doped segregation pockets at S/D lead to a strong upward band bending at the silicon/silicide interface. The effective SBH for electrons at the drain becomes higher while for holes at the source it becomes lower.

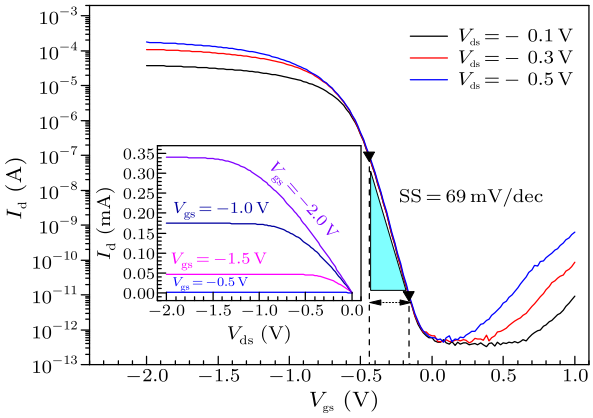

Fig. 3. Transfer characteristics of 3μm-gate SB-MOSFET at room temperature with different V_{ds}, showing an SS = 69 mV/dec and a high I_{on}/I_{off} ratio ~10^8. The output characteristics (inset) reveal a linear onset at small V_{ds} and a good saturation.

The transfer characteristics of the fabricated DS SB-MOSFET with a gate length of 3 μm measured at room temperature are presented in Fig. 3. A sub-

threshold swing (SS) of about 69 mV/dec is achieved. A high I_{on}/I_{off} ratio up to 10^8 is obtained for this transistor at $V_{ds} = -0.5$ V. The ambipolar switching behavior is suppressed by more than 5 orders of magnitude due to the high barrier height for electrons tunneling through at the drain caused by high dose of boron implantation. With V_{ds} reducing from -0.1 V to -0.5 V, the lowered barrier height at the drain is easier for electrons tunneling, which results in the increase of the n-branch current for about two orders of magnitude. The corresponding output characteristics of this device are shown in the inset of Fig. 3, which reveal a perfectly liner onset at small V_{ds} and a good saturation.

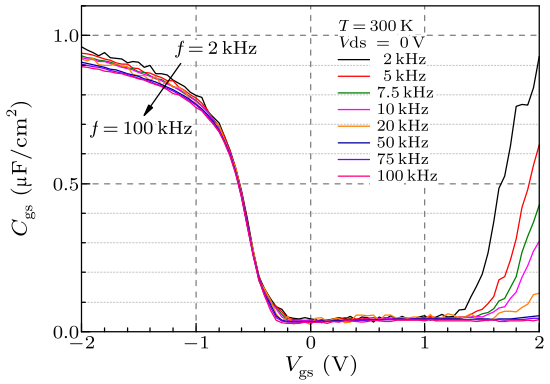

Fig. 4. Gate-to-source capacitance C_{gs} with respect to V_{gs} of p-type SB-MOSFET at different frequencies. Here C_{gs} decreases with the increase of frequency at the inverse regime for the channel.

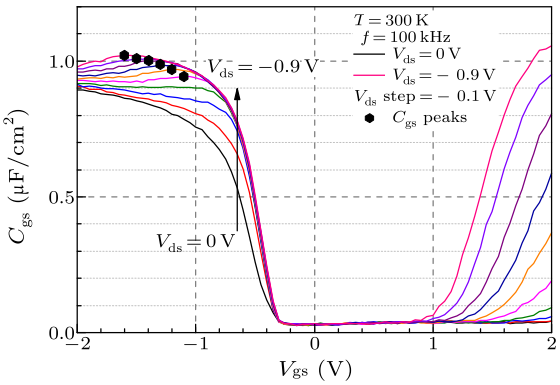

Fig. 5. Gate-to-source capacitance C_{gs} of p-type SB-MOSFET with respect to V_{gs} at different V_{ds}. The voltage step of the drain to source is -0.1 V. Here C_{gs} increases with the decrease of V_{ds} at the inverse and accumulation regimes for the channel. The peak of C_{gs} at the accumulation regime is marked as a black hexagon.

The capacitance of the SB-MOSFET with the gate length of 11 μm was systematically measured in this work. Regarding the C_{gs} measurement, the source and the gate are connected to the LCR meter, and the drain is connected to a dc bias. However, for the C_{gd} measurement, the connections to the source and drain are just exchanged. The capacitance between gate to source at $V_{ds} = 0$ V with the frequency differing from 2 kHz to 100 kHz is shown in Fig. 4. At $V_{gs} > 1$ V, C_{gs} is decreased nearly to zero when the frequency goes upward to 100 kHz, similar to an MOS capacitor under depletion and inversion. At $V_{gs} < 0$ V, the small dispersion of C_{gs} curves among varied frequencies reveals the low density of interface states at the semiconductor/insulator interface.

The capacitance C_{gs} is also significantly affected by the voltage of the drain and source, as shown in Fig. 5. With V_{ds} varying from 0 V to -0.9 V, C_{gs} increases in both forward and reverse directions, while the physical explanation differs.

At $V_{gs} > 0$ V, the channel is inversed to n-type. Since the silicon was p-type at the edge of the channel due to dopant segregation, a p–n junction is created at the reverse bias state. With decreasing the drain voltage, the reverse bias voltage of the p–n junction reduces leading to the decrease of the depletion layer thickness and the increasing capacitance of the depletion layer. Since the capacitance between gate and source can be approximatively regarded as the series connection of the plate capacitance of the gate to channel and the capacitance of the p–n junction, the capacitance C_{gs} increases with the decreasing drain-to-source voltage.

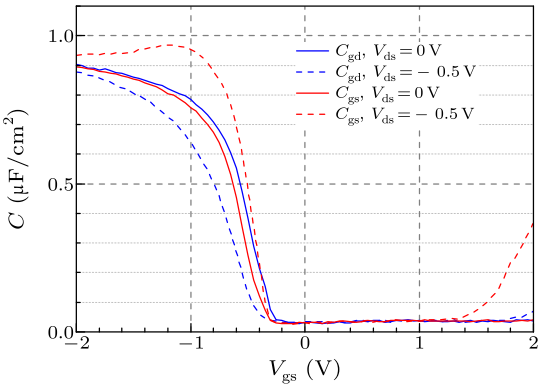

Fig. 6. The comparison of C_{gs} and C_{gs} with varied V_{ds}. In the reverse direction when the drain-to-source voltage reduces from zero, the gate-to-source capacitance C_{gs} becomes larger while the gate-to-drain capacitance C_{gd} becomes lower. In the forward direction the gate-to-source capacitance increases with reducing V_{ds} due to the capacitance increment of the reverse-biased p–n junction.

At $V_{gs} < 0$ V, the lightly p-doped top silicon is accumulated to the p-type channel due to the reduction of surface potential. When the drain voltage decreases, the potential of the channel is redistributed. The accumulated channel near the drain becomes thinner, while the channel becomes thicker near the source, resulting in the imbalance of the carrier distribution along the channel. Thus the gate-to-drain capacitance is decreased while the gate-to-source capacitance is increased when the drain-to-source voltage reduces from 0 V to -0.9 V. The different variation trends of C_{gs} and C_{gd} are compared in Fig. 6. However, with decreasing V_{gs}, C_{gs} obtains a maximum and then decreases at the accumulation regime. Since $C_{gs} + C_{gd} = C_{gg} \approx C_{ox}$ at higher $|V_{gs}|$, the increase of C_{gd} can lead to C_{gs} reducing due to the partition.

The maximum of capacitance C_{gs} at various V_{ds} is marked as a black hexagon in Fig. 5. A strong linear relationship between V_{gs} and V_{gd} of peaks is shown in Fig. 7 and it can be simply expressed as $V_{gs} = V_{ds} - 0.7\,\text{V}$. This reveals at the accumulation regime when the drain voltage is higher than the gate voltage for about 0.7 V, the distribution of the accumulation area of the channel leads to a maximum C_{gs}. For any given semiconductor and metal combination, the sum of the barrier heights on n-type and p-type substrates is expected to be equal to the bandgap.[34] Since the SBH amounts 0.35 eV for epitaxial $NiSi_2$ on n-Si and the bandgap is 1.12 eV for Si, the SBH on p-Si for holes should be about 0.77 eV. A strong upward band bending at the interface between highly doped silicon and $NiSi_2$ (shown in Fig. 2) results in about 0.7 V voltage droop of the p^+ region for S/D. When $V_{gd} = -0.7\,\text{V}$, there are almost no holes accumulated near the p^+ region of the drain while the channel of the source side gains much. Thus the most imbalanced carriers distribution of the channel occurs and C_{gs} becomes the maximum. Furthermore, in this situation the channel will be pinched off near the drain and the transistor will work in the saturation region if $|V_{ds}|$ becomes larger. This indicates that dopant segregation and SBH can tune the build-in voltage for Schottky S/D contacts, thus can affect the pinch-off voltage and saturation current for SB-MOSFETs. On the other hand, when $|V_{ds}|$ is less than 0.4 V, C_{gs} monotonically increases with a negative V_{gs} decreasing, and the curves of C_{gs} and C_{gd} are more similar to C_{gg}.

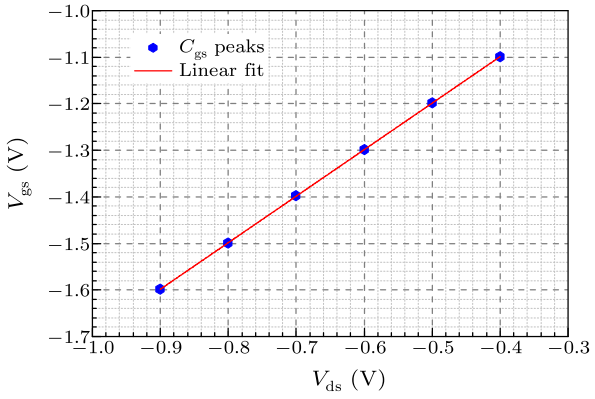

Fig. 7. The strong linear relationship between V_{gs} and V_{ds} of C_{gs} peaks.

In summary, p-type SB-MOSFETs with epitaxial $NiSi_2$ for S/D contacts and dopant segregation have been fabricated on ultrathin SOI substrates. Good SS of 69 mV/dec and relative high I_{on}/I_{off} ratio have been achieved for SB-MOSFETs. The C–V analysis of the accumulation regime reveals that C_{gs} obtains a maximum with decreasing V_{gs} due to the imbalanced redistribution of the channel. By extracting V_{gs} and V_{ds} at C_{gs} peaks we find that the difference of them has a strong relationship with SBH, which indicates that the SBH for $NiSi_2$ on silicon and dopant segregation can affect pinch-off voltage and saturation current of the SB-MOSFETs.

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