Radio-Frequency Characteristics of Partial Dielectric Removal HR-SOI and TR-SOI Substrates

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High-resistivity silicon-on-insulator (HR-SOI) and trap-rich high-resistivity silicon-on-insulator (TR-SOI) substrates have been widely adopted for high-performance rf integrated circuits. Radio-frequency loss and non-linearity characteristics are measured from coplanar waveguide (CPW) transmission lines fabricated on HR-SOI and TR-SOI substrates. The patterned insulator structure is introduced to reduce loss and non-linearity characteristics. A metal-oxide-semiconductor (MOS) CPW circuit model is established to expound the mechanism of reducing the parasitic surface conductance (PSC) effect by combining the semiconductor characteristic analysis (pseudo-MOS and C–V test). The rf performance of the CPW transmission lines under dc bias supply is also compared. The TR-SOI substrate with the patterned oxide structure sample has the minimum rf loss (<0.2 dB/mm up to 10 GHz), the best non-linearity performance, and reductions of 4 dB and 10 dB are compared with the state-of-the-art TR-SOI sample's, HD2 and HD3, respectively. It shows the potential application for integrating the two schemes to further suppress the PSC effect.

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The applications of 5G communication and internet of things (IOT) demand for integrating more system components. Systems on chip (SOC) and systems in package (SIP) are foreseen as promising solutions due to fully integrated logic processors, mix-signal processors, baseband, DSP, MEMS, memory, PMU and rf front-ends.[1] Only the Si-CMOS-based technologies could provide a feasible and cost-effective integration. Because of the low rf loss, high-resistivity (HR) silicon is preferred for the rf applications. The silicon-on-insulator (SOI) technologies have been developed for high speed, high frequency applications for many years.[2] The SOI substrates can effectively suppress the parasitic effects by isolating the active and passive devices fabricated on top silicon from the handle wafer. SOI with high-resistivity handle wafer substrate (HR-SOI) provides both HR properties and CMOS compatibility.[3] Hence, SOI is becoming more and more popular in modern communication systems.

Even the HR-SOI satisfies most of the requirements of the rf applications, the inherent properties of oxide-semiconductor (OS) structure induce a highly conductive layer at the Si surface close to the Si–SiO_2 interface named the parasitic surface conductive (PSC) effect. PSC is more pronounced for the surface resistivity decrease and the rf performance degeneration.[4,5] Three mainstream techniques have been developed to reduce these parasitic effects and to enhance the HR properties of Si, including proton implantation,[6] partial dielectric removal or surface trenched,[7] and surface stabilization.[8−13] To further enhance the rf performances, it may be necessary to integrate multiple solutions.

In this work, we investigate the impact of a trap-rich layer and partial dielectric removal on the rf performance of HR-SOI substrates. The rf loss and substrate non-linearity characteristics are studied with 50 Ω CPW transmission lines fabricated on HR-SOI substrates with different structures. The results are analyzed with the pseudo-MOS *I-V* test[14] and the high-resistivity silicon quasi-static *C–V* test.[20−21] Finally, the mechanisms of the action of the trap-rich layer and partial dielectric removal are explained.

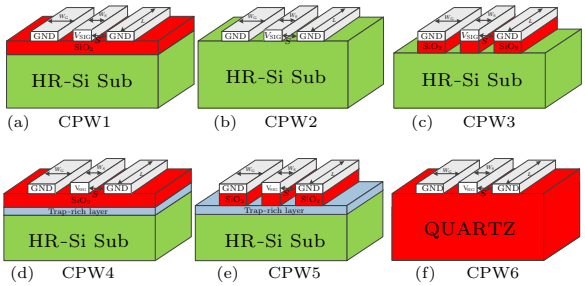

Fig. 1. Schematic diagram of CPW lines: (a) CPW1, (b) CPW2, (c) CPW3, (d) CPW4, (e) CPW5 and (f) CPW6.

The schematic diagrams of the structures used in this work are shown in Fig. 1, and the material information is summarized in Table 1. The HR-SOI and TR-SOI wafers are fabricated by the ion-cut technique. The top silicon layers of the SOI substrates are completely removed by TMAH in this study. The metal layers consist of 0.5 μm aluminum and 0.5 μm gold. The CPW lines were designed for a characteristic impedance of 50 Ω with $W = 30\,\mu m$, $S = 12\,\mu m$, $W_g = 208\,\mu m$, and the conductor length $L = 2176\,\mu m$.

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A normal MOS CPW circuit model is shown in Fig. 2(a). Here C_{ox} (oxide capacitance) and C_{air} (air capacitance) are constants, $R_s(V_{Sig})$ and $C_s(V_{Sig})$ express the semiconductor surface resistance and the capacitance below to the signal line, $R_s(V_{GND})$ and $C_s(V_{GND})$ express the R and C underneath ground lines, which are subject to signal voltage V_{Sig}, R_s and C_s express the R and C between $R_s(V_{Sig})$ and $R_s(V_{GND})$. Space charge region resistance and capacitance are represented as $R_{deep}(V_{Sig})$ and $C_{deep}(V_{Sig})$. The state of the above R and C changed with the longitudinal electric field, and the above R and C changed significantly. The properties of silicon substrate (region below the maximum depletion region) are not considered to be affected by the bias voltage and the fixed oxide charges, in other words, $R_a \approx R_b \approx R_c$. The $R(V)$ functions are calculated from carrier distributions, and quasi-static R_s and R_{deep} functions are obtained from MOS substrates (Fig. 2(b)) and follow the basic principle $R_{fb} \gg R_{dep} \gg R_{acc}, R_{inv}$, where R_{dep} is the depletion region resistance, R_{acc} is the accumulation region resistance, R_{inv} is the inversion region resistance, and R_{fb} is the flat band resistance.

Table 1. Material information.

	Substrates	ρ of bulk Si (kΩ·cm)	t_{ox} (μm)	t_{poly} (μm)	t_{Si} (μm)
CPW1	HR-SOI	3.3	0.4	None	725
CPW2	HR-SI	3.3	None	None	725
CPW3	HR-SOI pattern box	3.3	0.4	None	725
CPW4	TR-SOI	3.3	0.4	1.9	725
CPW5	TR-SOI pattern box	3.3	0.4	1.9	725
CPW6	Quartz	None	800	None	None

In addition, the pseudo-MOS transistors were fabricated on HR-SOI and TR-SOI wafers with square Si islands of 5 mm×5 mm using an STS HRM.[14] The top Si film behaved as the transistor and drain/source simultaneously, whereas the Si substrate and the box serve as the back gate and the gate oxide, respectively. This structure functions as an upside-down MOS transistor that is useful for characterizing the box fixed charge and the box/Si interface charge density. Electrical measurements were performed at room temperature with a drain bias of 0.1 V.

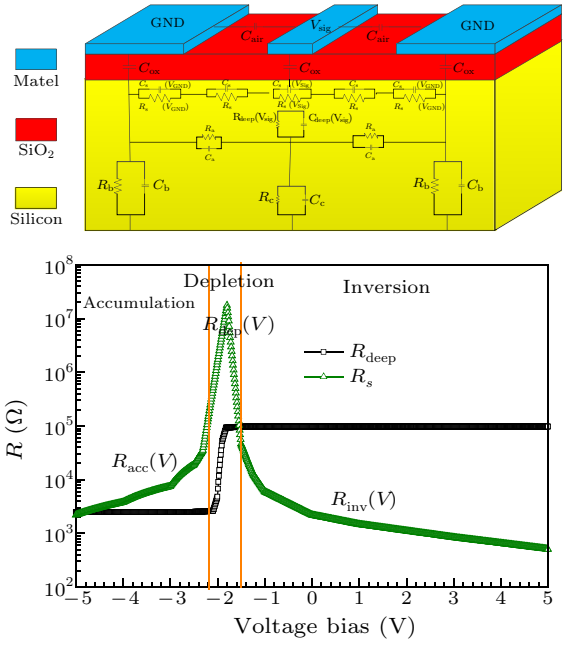

Fig. 2. (a) CPW circuit model, and (b) voltage dependent equivalent resistances function.

For the rf small signal measurement, the CPW lines are considered as a simple 2-port linear network, and S-parameters were measured from 10 MHz to 10 GHz with an Agilent N5242 vector network analyzer. Both the signal and ground lines were dc biased using a constant voltage source. Under all conditions, the electrical properties are independent of the signal ($P = -12$ dBm) and only vary with the applied dc bias voltage. TRL calibration is used as the de-embedding method.[15]

Figure 3(a) shows the extracted attenuation coefficient of the CPW lines. The substrate dissipation loss is dependent on the leakage conduction current distribution and the electric-field distribution. The rf loss of the CPW lines can be explained by combining the microwave loss mechanisms with the semiconductor theory. CPW2 (HR-SI) exhibits a low rf loss due to the fact that the Schottky barrier diodes pin the surface potential. The surface resistance can be divided into two types, with $R_s(V_{GND}) = R_s(V_{Sig}) = R_{dep}$ or without $R_s \approx R_{fb}$ metal coverage. The space charge region resistance $R_{deep}(V_{sig})$ equals to R_{dep} (Fig. 8(a)). However, without the passivation layer, the leakage current is significant at 20 μA at a dc bias of 0.3 V.[16] When dc biased, the significant variation of rf loss is caused by the current injection (Fig. 3(b)). To avoid the dc current injection, an isolating layer must be placed between the silicon and metal.

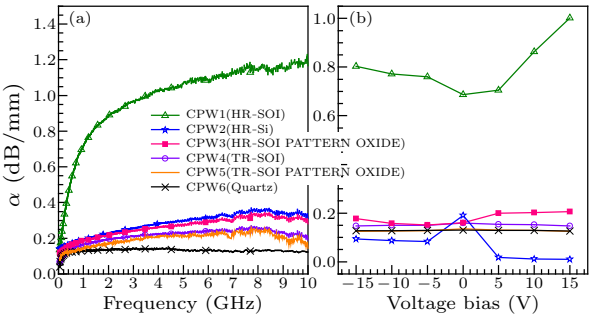

Fig. 3. Attenuation coefficients α of CPW lines on various substrates: (a) 0 dc bias versus frequency, (b) 900 MHz versus dc bias.

Unfortunately, the isolating oxide layer drastically

increases the loss, as found in Fig. 3(a) by comparing CPW1 (HR-SOI) with CPW2 (HR-SI). In CPW1 (HR-SOI), the semiconductor surface is covered with silicon dioxide, such that the distribution of surface carriers is influenced by the fixed oxide charge. Without the applied dc bias voltage, the parasitic conduction channel is formed in the Si-SiO_2 interface, Si surface inversion, $R_s(V_{sig}) = R_s = R_{inv}(0)$, $R_{deep}(V_{sig}) = R_{dep}$ (Fig. 8(b)). A low impedance path is formed from the signal line to ground (Fig. 5). For forward bias voltage, the inversion charges density is increased, the surface resistivity is reduced, $R_s(V_{sig}) = R_s = R_{inv}(V_{dc}) < R_{inv}(0)$, and $R_{deep}(V_{sig}) = R_{dep}$ (Fig. 8(c)). The reduction of the total surface resistivity causes the attenuation to deteriorate. For reverse bias voltage larger than the flat band voltage V_{fb}, the analyses of the simulated $R(V)$ functions (Fig. 2(b)) and the MOS C–V (Fig. 4(a)) reveal that the flat band voltage V_{fb} approaches to -2 V, and majority carriers are accumulated in the semiconductor surface, $R_s(V_{sig}) = R_s = R_{deep}(V_{sig}) = R_{acc}$ (Fig. 8(d)). In addition, $R_{deep}(V_{sig})$ in this case is biased in accumulation status, which is much smaller than depletion status, hence the attenuation caused by $R_{deep}(V_{sig})$ is larger than that in the weak inversion. Therefore, the total attenuation of -5 V dc bias (accumulation) is larger than 5 V dc bias. Attenuation coefficient has a minimum value when the applied voltage equals the flat-band voltage.

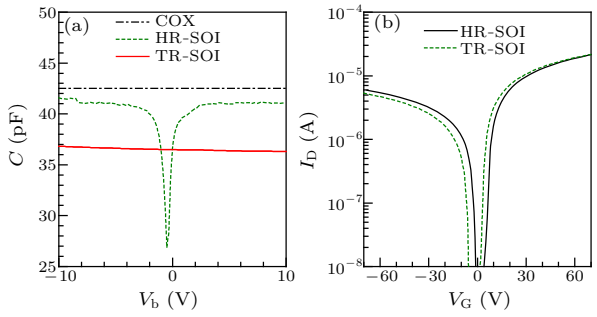

Fig. 4. (a) Quasi-static C–V characteristic of HR-TR sub-box capacitors results, and (b) I–V characteristic curves for the pseudo-MOS transistors.

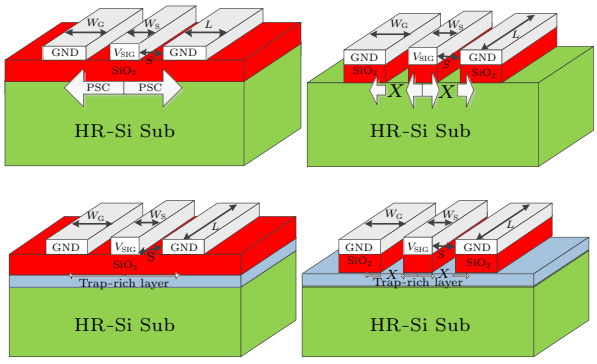

Fig. 5. PSC effect of different substrates.

Compared with CPW1 (HR-SOI), CPW3 (HR-SOI PATTERN OXIDE) presents extremely low attenuations, because partially removing the dielectric leads to a reduction of the surface charge. In this case, the surface resistivity without oxide-covered region is very high ($R_s \approx R_{fb}$), although the oxide-covered surface area still suffers from the PSC effect, and the total surface resistivity depends on the overall series resistance. The parasitic conductor channel in the HR-SOI sample is cut off in the partial dielectric removal sample (Fig. 5), hence the total surface resistivity is high, and no low impedance path exists. In addition, the dielectric constant of the substrate at the edges of the signal line and ground conductors is reduced, the skin effect can be reduced, and hence the conductor loss is reduced.[17] However, the behavior of oxide covered area under dc bias is similar to the HR-SOI substrate, residual bias-dependence $R_s(V_{sig}) = R_s(V_{GND}) = R_{inv}$ (Fig. 8(e)). Figure 6(a) shows the extracted attenuation versus different sizes of CPW lines. When the ratio of S/W is increased, the attenuations of the CPW3 reduce faster than the other samples. As the ratio of S/W is increased, the oxide etched areas increase, the high surface resistivity area increases, so that the total surface resistance increases. Similarly, for CPW3, the dc bias effect decreases when the bias voltage controlled region shrinks.

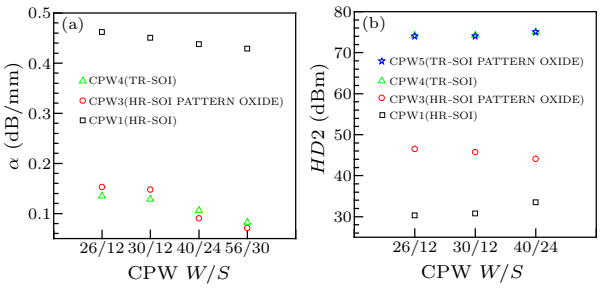

Fig. 6. (a) Attenuation coefficients α of different dimensions CPWs, and (b) HD2 of different CPW sizes.

Compared with GaAs[18] and SOS[19] technologies, CPW4 (TR-SOI) has a similar substrate loss and bias independence. The poly-silicon layer creates a high density of carrier traps distributed across the energy band gap due to grain boundaries and the defects to capture the free carriers. That is to say, fixed oxide charges in the box cannot induce the inversion layer in the silicon surface. We can consider the behavior of the surface resistance using the quasi-static C–V test. From Fig. 4(a), the HR-SOI sample indicates a typical low-frequency MOS-capacitance characteristic. The TR-SOI sample has no bias dependence and is lower than the capacitance of the oxide layer C_{ox}. This phenomenon is similar to the MOS capacitance with a large value of D_{it} (interface trap dencity) where C_{it} (interface trap capacitance) will shield the effect of C_s (silicon surface capacitance). Comparing C_{TR-SOI} with C_{HR-SOI}, the doping concentration of the substrate and C_{ox} are identical, C_{TR-SOI} is equal to C_{HR-SOI} bias in the depletion region, and it is revealed that TR-SOI maintains the depletion status constantly, neither inver-

sion carriers nor accumulation carriers exist. That is to say, the silicon surface potential is pinned and $R_s(V_{GND}) = R_s(V_{Sig}) = R_s \equiv R_{dep}R_{deep}(V_{sig}) = R_{dep}$ (Fig. 8(f)). The whole components of the surface resistance are high, the total surface resistivity is apparently high, the parasitic surface current is small (Fig. 5), and the PSC effect is eliminated. It is an efficient solution to reduce the insertion loss along CPW and the dc bias dependence.

The role of the trap-rich layer can also be proved by the pseudo-MOS test. Figure 4(b) illustrates the I–V characteristic curves of the HR-SOI and TR-SOI pseudo-MOS transistors. A small negative shift has been observed between the HR-SOI and the TR-SOI samples, indicating that the trap-rich layer charge plays a role of the back gate threshold voltage. It can be attributed to the trap-rich layer capturing the free electrons and compensating for fixed positive oxide charge effect of the MOS structure's threshold voltage.[24]

CPW5 (TR-SOI PATTERN OXIDE) combines the function of partial dielectric removal and trap-rich layer, both 'weak' and 'cut' (Fig. 5). Hence, it obtains a minimum value of the attenuation coefficient. It enables the performance to move forward a step, and we obtain a lower rf loss in this sample.

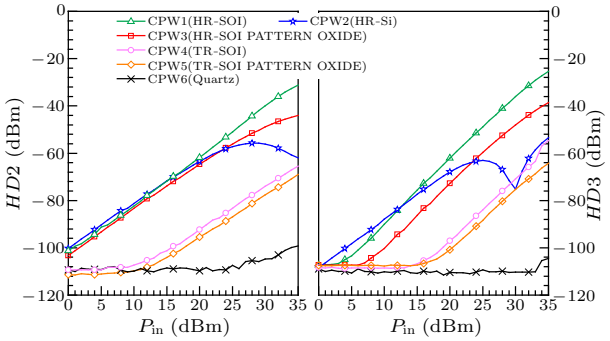

Fig. 7. Measured 2nd and 3rd harmonic distortions.

Another key performance of rf is the harmonic distortion. The output signal waveform of a nonlinear system excited at a modulated input signal will contain high-order harmonics. It has been reported that the generation of harmonic distortion in matched transmission lines placed on HR-SOI substrates mainly comes from the substrate.[22] Fixed charges in the HR-SOI box induce a conductive channel below the box, and the carriers in this channel layer will respond to the signal. At a high frequency, the carriers do not have enough time to achieve their equilibrium distribution, any changes in V_{SIG} resulted in the change of $R_s(V_{Sig})C_s(V_{Sig})$ and $R_{deep}(V_{Sig})C_{deep}(V_{Sig})$. Assuming that the relaxation time of the RC is τ, a larger than $1/\tau$ frequency signal will mean the carriers cannot reach a stable state. Combining the $R(V)$ functions (Fig. 2(b)), the state of the resistor will be changed significantly when the amplitude of the signal over the flat-band voltage V_{fb}, and the parasitic RC circuit cannot follow the variation which further results in a distorted output signal. It had been demonstrated that the nonlinear behavior mainly depends on the variation of R with the voltage rather than the variation of C.[23]

The 2nd and 3rd harmonics are measured from CPW lines at 900 MHz fundamental frequency to analyze the non-linear characteristics. The amplitude of the signal is from −15 dBm to 20 dBm with 1 dBm interval. The 20 dB power amplifier adjusts the power of the input signal applied to the DUT upper to 35 dBm. The low-pass pre-filter was set to 935 MHz, and the high-pass post-filter was set to 1860 MHz. The harmonics measurement is presented in Fig. 7.

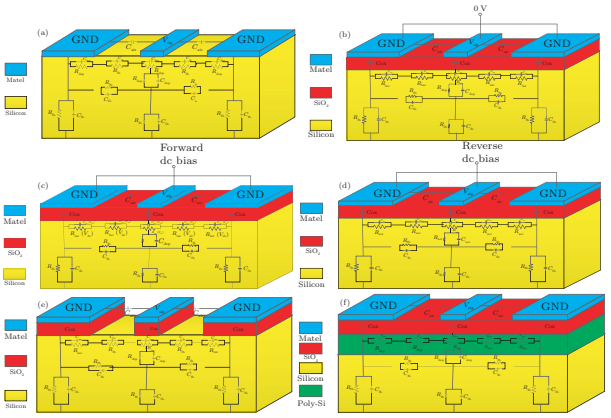

Fig. 8. Differently structured CPW circuit models of (a) CPW2 (HR-SI), (b) CPW1 (HR-SOI 0 V), (c) CPW1 (HR-SOI forward bias), (d) CPW1 (HR-SOI reverse bias), (e) CPW3 (HR-SOI PATTERN OXIDE), and (f) CPW4 (TR-SOI).

A series of results have been obtained. (i) HD2 and HD3 of CPW4 (TR-SOI) are much lower than that of CPW1 (HR-SOI). The trap-rich layer reduces the harmonic distortion remarkably. For TR-SOI, the silicon surface potential pinned and the external dc bias or large rf signal applied to the CPW lines do not impact the carrier distribution profiles in the Si–SiO_2 interface, which means that both R and C are almost constant. (ii) The impact of partially removing the dielectric on the harmonic distortion is limited. It is demonstrated that partially removing the dielectric cannot eliminate the bias-dependence effects in the previous section. The values of R and C of the signal metal covered region change with the external dc bias, and will change with a large rf signal. Therefore, it is not an efficient way to reduce the harmonic distortion. However, it is interesting to see in Fig. 6(b) that the trends of CPW1 (HR-SOI) and CPW3 (HR-SOI PATTERN OXIDE) are reversed. For different CPW sizes, the higher the line width W is, the more deteriorative the harmonic distortion is. Note that it is different from the conclusion in small signal test; the key point is the line width W not W/S. The reason is only the R and C underneath or close to the signal line ($R_s(V_{Sig})C_s(V_{Sig})$ and $R_{deep}(V_{Sig})C_{deep}(V_{Sig})$ in Fig. 2(a)) suffered from the modulated effect under the large rf signal. (iii) Even if the impact of partially removing the dielectric is limited, compared with the

trap-rich layer, it is a useful method to integrate the two schemes to improve the non-linear performance. Compared with the CPW4 (TR-SOI) wafer, reductions of 4 dB and 10 dB are measured on CPW5 (TR-SOI PATTERN box), HD2 and HD3.

It should be mentioned that in this study, multiple frequencies are used for characterizations, and we only use the data at 900 MHz for demonstration purpose. The conclusions are valid on other frequencies as well.

In summary, the rf loss and harmonics distortion characteristics of HR-SOI, TR-SOI and partial dielectric removal HR-SOI/TR-SOI substrates used for radio-frequency applications have been studied. We have evaluated the small and large signal results of the total substrates, and the quasi C–V analysis and pseudo-MOS test are compared. Both introducing a trap-rich layer and partially removing the dielectric can obtain a reduction of attention coefficient. However, it has been demonstrated that introducing a trap-rich layer can also eliminate the harmonic distortion when the impact of partially removing the dielectric is limited. For different device sizes, the impacts of two solutions are quite different due to different mechanisms. Then the mechanisms of introducing a trap-rich layer or partially removing the dielectric to improve the rf performances are analyzed using an MOS CPW model. As a consequence, by including a patterned SiO_2 structure in the state of the art TR-SOI, excellent performance can be achieved.

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