Positive Bias Temperature Instability Degradation of Buried InGaAs Channel nMOSFETs with InGaP Barrier Layer and Al_2O_3 Dielectric *

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(Received 30 November 2016)

Positive bias temperature instability stress induced interface trap density in a buried InGaAs channel metal-oxide-semiconductor field-effect transistor with a InGaP barrier layer and Al_2O_3 dielectric is investigated. Well behaved split C–V characteristics with small capacitance frequency dispersion are confirmed after the insertion of the InGaP barrier layer. The direct-current I_d–V_g measurements show both degradations of positive gate voltage shift and sub-threshold swing in the sub-threshold region, and degradation of positive ΔV_g in the on-current region. The I_d–V_g degradation during the positive bias temperature instability tests is mainly contributed by the generation of near interface acceptor traps under stress. Specifically, the stress induced acceptor traps contain both permanent and recoverable traps. Compared with surface channel InGaAs devices, stress induced recoverable donor traps are negligible in the buried channel ones.

PACS: 73.40.Qv, 71.55.Eq, 77.55.D− DOI: 10.1088/0256-307X/34/5/057301

Continuous Si complementary metal-oxide-semiconductor (CMOS) scaling and performance improvements meet a great challenge. To maintain Moore's law, great efforts have been devoted to alternative channel materials beyond Si, such as germanium, and InGaAs.[1–3] One promising solution is to integrate InGaAs channels for NMOS and Ge channels for PMOS for CMOS applications. Recently, Ge thin films with high quality have been successfully integrated on lattice matched GaAs substrates,[4] and high performance Ge PMOS using $HfO_2/Al_2O_3/GeO_x$ gate stack has been reported.[3] However, compared with Ge channel devices, InGaAs channel metal-oxide-semiconductor field-effect transistors (MOSFETs) still need further study. The main obstacle for InGaAs MOSFETs is the lack of high-quality thermodynamically stable gate dielectrics. Recently, surface channel InGaAs MOSFETs with atomic layer deposited (ALD) Al_2O_3,[2] HfO_2,[5] ZrO_2[6] have demonstrated improved interface passivation and stability, while the effective channel mobility is still relatively low compared with that of the bulk InGaAs due to the high defect density between the InGaAs channel and the high-k gate dielectric, which may cause a severe reliability problem. The surface channel InGaAs MOSFET has been proved by Franco *et al.*, showing poor reliability when compared with Si-MOSFET, in line with GeO_x/high-k nMOS.[7] For surface channel InGaAs MOSFETs, the positive bias temperature instability (PBTI) relaxation behavior does not obey the single-log(t) trend, suggesting multiple defect types in Al_2O_3/InGaAs stacks.[7] Moreover, surface channel InGaAs MOSFETs under positive bias temperature instability (PBTI) stress and recovery have been systematically investigated by Li *et al.*,[8] and they have revealed that there are high densities of fast interface traps and slow oxide border traps near the interface between InGaAs and Al_2O_3. The border traps are more fragile under stress, and therefore the stress mainly induces border traps.

Compared with surface channel InGaAs MOSFETs, InGaAs channel MOSFETs with a barrier layer are obtained and have renewed attention for n-type devices because a barrier layer helps to move the InGaAs channel away from the high-k oxide interface, therefore higher electron mobility can be achieved.[9,10] Moreover, by selecting the barrier layer material, it is able to obtain a high quality gate stack with low interface trap density D_{it} and border traps. For example, our previous research has demonstrated very

*Supported by the National Science and Technology Major Project of China under Grant No 2011ZX02708-003, the National Natural Science Foundation of China under Grant No 61504165, and the Opening Project of Key Laboratory of Microelectronics Devices and Integrated Technology of Institute of Microelectronics of Chinese Academy of Sciences.

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low D_{it} in the level of $2 \times 10^{11}\,cm^{-2}eV^{-1}$ and very small accumulation capacitance frequency dispersion in an Al_2O_3/InP stack by carefully tuning the thermal treatment and pre-dielectric surface passivation process.[11] Although high performance is expected in buried channel InGaAs MOSFETs, its reliability research is still in the infant stage, few reports have been published for the buried channel case. Therefore, to understand the reliability of buried channel InGaAs NMOSFETs, in this work, we investigate the degradation under PBTI stress and recovery behavior by experiments and physical interpretations.

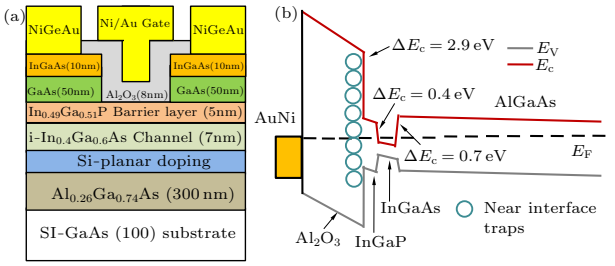

Fig. 1. (a) Cross-sectional schematic structure of the planar buried channel $In_{0.4}Ga_{0.6}As$ n-MOSFET with 5 nm $In_{0.49}Ga_{0.51}P$ barrier layer and 8-nm-Al_2O_3 dielectric, and (b) the band diagram and traps distribution in the nMOSFET.

Figure 1(a) shows the cross-sectional schematic of the $In_{0.4}Ga_{0.6}As$ MOSFET structure. The layer structure was grown on a semi-insulating GaAs substrate by metal-organic chemical vapor deposition (MOCVD) and consisted of a 300 nm $Al_{0.26}Ga_{0.74}As$ buffer layer (with Si planar doping at 3 nm below the InGaAs channel), a 7 nm $In_{0.4}Ga_{0.6}As$ strained quantum well channel layer, a 5 nm $In_{0.49}Ga_{0.51}P$ barrier layer, and an n^+ contact layer including a 50 nm GaAs cap layer and a 10 nm $In_{0.54}Ga_{0.46}As$ cap layer. The sheet resistance was 100 Ω/sq, and the room-temperature Hall mobility was larger than $8000\,cm^2/(V{\cdot}s)$. The n^+ contact layer was selectively removed by phosphate acid solution (H_3PO_4:H_2O_2:H_2O=3:1:50). The $In_{0.49}Ga_{0.51}P$ barrier layer was removed by hydrochloric acid solution (HCl:H_3PO_4=1:4). After a recess, the wafers were pretreated by diluted hydrochloric acid solution and ammonia-based solution. Then, 8 nm Al_2O_3 was deposited by ALD as the gate dielectric. The Ni/Au gate metal, Ni/Ge/Au/Ge/Ni/Au source, and drain Ohmic contacts were then deposited by e-beam evaporation, respectively, after selectively etching Al_2O_3 using a buffered oxide etch (BOE). Finally, a rapid thermal annealing (RTA) process at 270℃ for 3 min in an N_2 ambient was carried out. The sheet resistance and the contact resistance of the source and drain regions were determined to be only 100 Ω/sq and 0.1 Ω·mm, respectively. Figure 1(b) shows the energy band diagram for $In_{0.4}Ga_{0.6}As$ channel MOSFETs with an $In_{0.49}Ga_{0.51}P$ barrier layer.

HP 4284 LCR and Keysight B1500A meters, as well as Lakeshore probe station, were used for the capacitance-voltage (C–V) and current-voltage (I–V) measurements, at room temperature. In the C–V measurements, split C–V curves were measured by connecting the source and drain for low terminal, the gate for high terminal, and grounding the substrate. In the I_d–V_g measurements, V_d is set to 50 mV, while the source and the substrate are grounded. During the PBTI stress phase, the gate stress voltage is set as V_g = 1–5 V, while $V_s = V_d = V_b = 0$ V. During the recovery phase, all the electrodes are grounded. For the fresh transistors used in this work, the threshold voltage V_{th} is in the range of +0.3–+0.4 V. The subthreshold swing (S-factor) is around 145 mV/decade. All the above measurements were performed at room temperature (300 K).

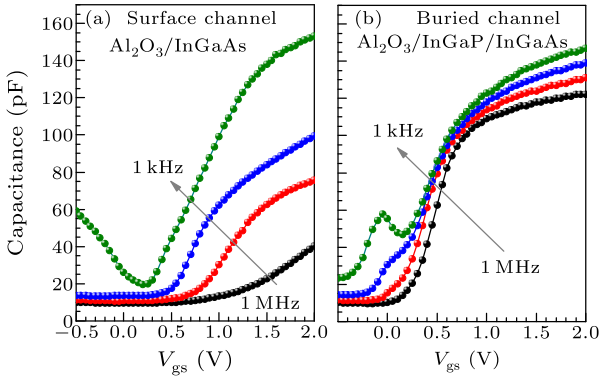

Fig. 2. Split C–V characteristics of (a) surface channel InGaAs nMOSFETs and (b) buried channel InGaAs MOSFETs with the $In_{0.49}Ga_{0.51}P$ barrier layer.

Figures 2 illustrates the multi-frequency split C–V curves at room temperature for the surface channel InGaAs MOSFET and the buried channel InGaAs MOSFET with an InGaP barrier layer. For the surface channel case, huge capacitance frequency dispersion is observed, especially in the on-state region. The origin of the capacitance frequency dispersion in the on-state region is ascribed to the large amount of oxide border traps. Compared with the surface channel MOSFET, the buried channel one shows much improved C–V characteristics with significantly less frequency dispersion near V_{th} and at on-state, indicating that the insertion of an InGaP barrier layer is effective in reducing the interface and border traps. Note that quantitative evaluation of the D_{it} profile is impossibly present, because it is difficult to accurately subtract the coupling capacitance from the substrate and source/drain sides from the structure in Fig. 1(a).

According to the investigation by Li *et al.*,[8] the reductions of interface and border traps are beneficial to device reliability. Therefore, dc I_d–V_g measurements were performed under PBTI stress. Figure 3 shows the dc I_d–V_g curves measured for the fresh

device before stress (initial state, I lines), after 500 s PBTI stress (S lines), and with additional 500 s recovery (R lines). Comparing S lines with I lines, the V_g shift ΔV_g at constant current I_d is positive in both the sub-threshold region and at high I_d in the on-current region, indicating that net negative charge is created after the PBTI stress. Compared with S lines, R lines demonstrate a negative shift at high I_d in the on-current region, indicating that recovery happens. Compared with I lines, R lines demonstrate a positive shift, indicating that the stress induced traps are not fully recoverable. Moreover, the results in Fig. 3 show a permanent degradation in S factor, suggesting that the stress induced interfacial traps are dominated by permanent traps. Therefore, on the basis of the results in Fig. 3, it is possible for us to conclude that permanent and recoverable traps coexist.

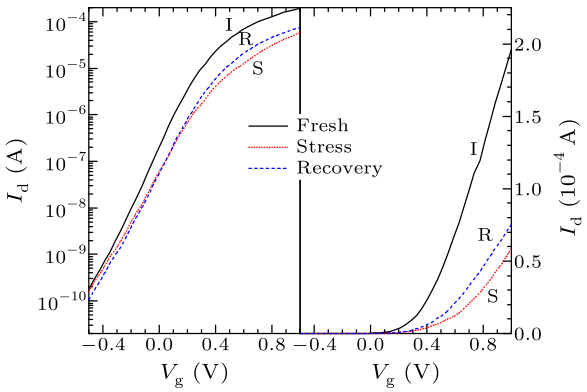

Fig. 3. The I_d–V_g curves for the fresh buried channel InGaAs n-MOSFET (denoted by I lines), after 500 s PBTI stress (V_g = 5.0 V) (denoted by S lines), and then after 500 s recovery (V_g = 0 V) (denoted by R lines), with V_d = 50 mV, and W/L = 400 mm/2 mm. The left figure shows the I_d–V_g behavior in the sub-threshold region on the right one shows the behavior at high I_d in the on-current region.

Although the similar trend of shift of I–V curves has been reported in InGaAs surface channel nMOSFETs in the on-current region,[8] the recoverable donor traps in the present work are believed to be responsible for the negative ΔV_g in the sub-threshold region. According to the simulation results by Varghese *et al.*,[12] donor traps at the interface induce negative V_g shift of the I–V curves, and larger shift with lower I_d current level. Acceptor traps at the interface induce positive shift of the I–V curves, larger shift with higher I_d current level. Concerning the different trends in the sub-threshold region, we infer that the InGaP/Al_2O_3 may contain less donor traps than the InGaAs/Al_2O_3 interface, which is reasonably consistent with the split C–V characteristics in Fig. 2.

To further understand the PBTI degradation in the sub-threshold region, PBTI stress in the range of V_g = 1–5 V is applied for 10 s to the buried channel InGaAs nMOSFETs, as shown in Fig. 4. In Fig. 4(a), the S-factor is found to degrade from 145 mV/dec to 184 mV/dec after +5 V stress for 10 s and shows a positive ΔV_g, implying the degradation of interface with interface net acceptor trap generation. Since stress induced donor traps may also exist, the stress induced acceptor traps are dominant when compared with donor traps, and we are not able to distinguish the donor traps from acceptor traps at present, thus we use the 'net' acceptor trap here. This is different from the results of surface channel InGaAs MOSFETs. Moreover, in Fig. 4(b), the I_d–V_g curves at on-state shift positively, indicating that the oxide traps are gradually filled by electron injection in terms of forming negative charge.

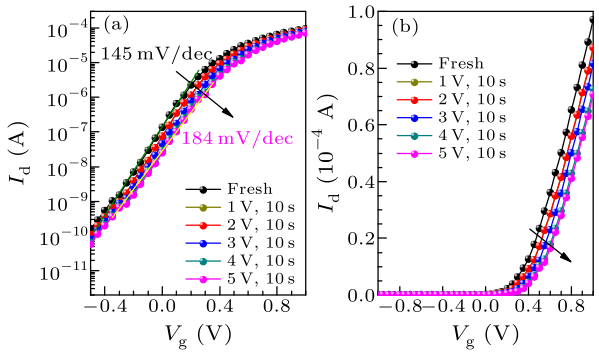

Fig. 4. The I_d–V_g curves for the fresh InGaAs n-MOSFET, after 10 s PBTI stress (V_g = 1–5 V), V_d = 50 mV. Comparing S lines with I lines, the V_g shift ΔV_g at constant current I_d is positive (a) in the sub-threshold region and (b) at high I_d in the on-current region.

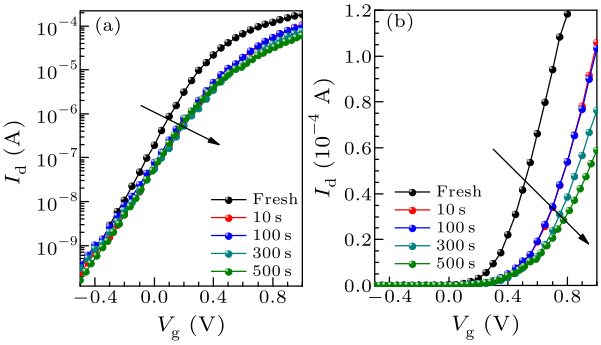

Fig. 5. The I_d–V_g curves for the fresh InGaAs n-MOSFET, after 10–500 s PBTI stress (V_g = 5 V), V_d = 50 mV (a) in the sub-threshold region, and (b) at high I_d in the on-current region. The degradation of interface is attributed to the interface net acceptor trap generation.

Figure 5 shows the I_d–V_g curves for the fresh InGaAs nMOSFETs, and the ones after 10–500 s PBTI stress (V_g = 5 V). In the sub-threshold region, the S factor degrades and becomes saturated even after 10 s stress. However, in the on-current region, degradation occurs gradually until 500 s stressing, indicating that the S factor and on-current (transconductance G_m or high-field mobility) degradation come from different sources. To further probe the traps behavior, NBTI

stress measurements were performed. Figure 6 shows the I_d–V_g curves for fresh InGaAs nMOSFETs, after 300 s −3 V NBTI stress, and the recovery curve after 1200 s. After the NBTI stress, the I_d–V_g curve shifts to the negative side, indicating the generation of positive charge. However, in the recovery phase, the I_d–V_g curve is almost fully recovered, suggesting the existence of recoverable donor traps. This phenomenon is similar to that in the surface channel case. Concerning the position of the recoverable donor traps, since the S factor does not degrade during the NBTI stress phase, we obtain that the recoverable donor traps are not localized at the Al_2O_3/InGaP interface but inside the Al_2O_3 dielectrics.

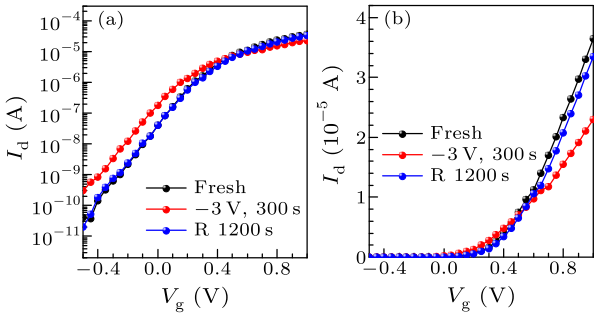

Fig. 6. The I_d–V_g curves for the fresh InGaAs nMOSFET, after 300 s NBTI stress ($V_g = -3$ V), and recovery curve $V_d = 50$ mV (a) in the sub-threshold region, and (b) at high I_d in the on-current region.

By using the similar method proposed by Li *et al.*, the distribution of stress induced border traps could be estimated from ΔV_g among the I lines, S lines and R lines under the assumptions of (1) during PBTI tests, at the end of 500 s stress, there are both stress induced donor traps and acceptor traps in the devices. (2) At the end of 500 s recovery, the stress induced donor traps fully recover while the acceptor traps are partially recoverable and partially permanent. (3) During NBTI tests, there are both stress induced donor traps and acceptor traps in the devices. The extraction procedure is as follows: in the PBTI test, ΔV_g is extracted from the I (initial) and R (after 500 s recovery) lines as a function of I_d for all the current range shown in Fig. 3. The result is denoted by $\Delta V_g^{IR}(I_d)$, since only the permanent acceptor traps remain after 500 s recovery, the density of negatively charged permanent acceptor traps $\Delta N_{ox}^{AP}(I_d)$ as a function of I_d can be obtained by[8]

$$\Delta N_{ox}^{AP}(I_d) = (C_{ox}/q)\Delta V_g^{IR}(I_d), \quad (1)$$

where C_{ox} is the gate oxide capacitance per unit area and is 10^{-6} F/cm^2 estimated by an 8 nm Al_2O_3 gate dielectric. On the other hand, the density difference of negatively charged acceptor traps and positively charged donor traps, $\Delta N_{ox}^{AP}(I_d)+\Delta N_{ox}^{AR}(I_d)-\Delta N_{ox}^{DR}(I_d)$, can be extracted from the I and S (after 500 s stress) lines, as shown in Fig. 3, by

$$\Delta N_{ox}^{AP}(I_d) + \Delta N_{ox}^{AR}(I_d) - \Delta N_{ox}^{DR}(I_d) = (C_{ox}/q)\Delta V_g^{IS}(I_d), \quad (2)$$

where $\Delta V_g^{IS}(I_d)$ is the V_g difference between the S and I lines at the same I_d, $\Delta N_{ox}^{AR}(I_d)$ is the density of negatively charged recoverable acceptor traps, and $\Delta N_{ox}^{DR}(I_d)$ is the density of positively charged recoverable donor traps. From Eqs. (1) and (2), the density of net-negatively charged recoverable acceptor traps $\Delta N_{ox}^{AR}(I_d) - \Delta N_{ox}^{DR}(I_d)$ can be obtained from

$$\Delta N_{ox}^{AR}(I_d) - \Delta N_{ox}^{DR}(I_d) = (C_{ox}/q)\Delta V_g^{IS}(I_d) - (C_{ox}/q)\Delta V_g^{IR}(I_d). \quad (3)$$

Combining Eqs. (1) and (3), we obtain $\Delta N_{ox}^{AP}(V_g)$, and $\Delta N_{ox}^{AR}(V_g) - \Delta N_{ox}^{DR}(V_g)$ as a function of the gate bias V_g, as shown in Fig. 7. Compared with the density of border traps in the surface channel InGaAs case, permanent acceptor traps with similar magnitude in the order of 1×10^{12} cm^{-2} have been obtained in our buried channel device while the density and type of recoverable traps are quite different. In buried channel InGaAs MOSFETs, recoverable traps induced by PBTI stress are mainly acceptor traps and with the maximal density level below 4×10^{11} cm^{-2}, while the recoverable traps induced by PBTI stress for the surface channel case are dominated by donor traps with the maximal density level of 1.5×10^{11} cm^{-2}.

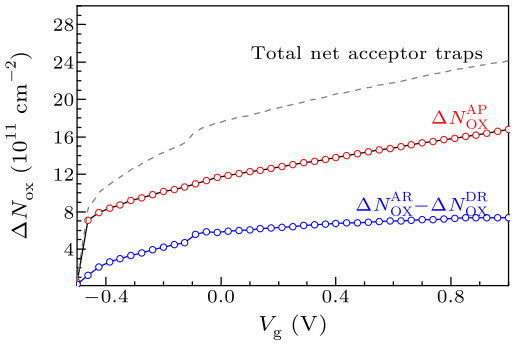

Fig. 7. The charged permanent acceptor $\Delta N_{ox}^{AP}(I_d)$ and net recoverable acceptor $\Delta N_{ox}^{AR}(I_d) - \Delta N_{ox}^{DR}(I_d)$ border trap area density as a function of gate bias V_g extracted from ΔV_g.

By considering the study of Li *et al.* and our experimental results, together with simulation results by Varghese *et al*,[12] impacts of PBTI stress on surface channel and buried channel InGaAs nMOSFETs are summarized as follows: (1) similar to Si-nMOSFETs, both surface channel and buried channel InGaAs nMOSFETs show positive V_{th} shift after PBTI stress, and this results in the reduction of on-state current. However, the positive shift in surface channel and buried channel InGaAs nMOSFETs is not only related to the fixed negative oxide charge

but also affected by the stress induced acceptor traps. (2) Albeit PBTI stress does not change the S-factor in Si-nMOSFETs because of the electron-trap-free nature in high-k/SiO_2/Si stack, and PBTI stress induces severe S-factor degradation and off-current increment in surface channel InGaAs nMOSFETs by generating recoverable donor traps while S-factor and off-current are only slightly degraded for the buried channel InGaAs case. The origin of S-factor degradation is mainly ascribed to the generation of net-acceptor traps, because recoverable donor traps are much less than those in surface channel devices and can be neglected. (3) For low-power applications, buried channel InGaAs MOSFETs are better to maintain the low off-state current and steep S-factor than the surface channel case from the viewpoint of reliability. However, for high-performance applications, both buried channel and surface channel InGaAs MOSFETs are suffering a severe reliability problem when compared with Si-nMOSFETs. Gate stack engineering still has a long way to go to overcome the generation of acceptor traps for InGaAs nMOSFETs.

In summary, for buried channel InGaAs nMOSFETs with the InGaP barrier layer, degradations of positive $\Delta V_{\rm g}$ and S factor in the sub-threshold region and degradation of positive $\Delta V_{\rm g}$ in the on-current region occurs after PBTI stress. The $I_{\rm d}$–$V_{\rm g}$ degradation is mainly contributed by the generation of permanent acceptor traps in the order of $10^{12}\,{\rm cm}^{-2}$ and net recoverable acceptor traps in the order of $4\times10^{11}\,{\rm cm}^{-2}$ under PBTI stress. Compared with surface channel InGaAs nMOSFETs, stress induced recoverable donor traps are negligible for the buried channel case.

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