A CMOS Compatible MEMS Pirani Vacuum Gauge with Monocrystal Silicon Heaters and Heat Sinks *

Le-Min Zhang(张乐民)[1], Bin-Bin Jiao(焦斌斌)[1**], Shi-Chang Yun(云世昌)[1], Yan-Mei Kong(孔延梅)[1], Chih-Wei Ku(辜志伟)[2], Da-Peng Chen(陈大鹏)[1]

[1]*Smart Sensing R&D Center, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029*
[2]*Company of Jiangsu Atmems, Wuxi 214000*

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We present a micro-Pirani vacuum gauge using the low-resistivity monocrystal silicon as the heaters and heat sinks fabricated by the post complementary metal oxide semiconductor (CMOS) microelectromechanical system (MEMS) process. The metal interconnection of the device is fabricated by a 0.5 μm standard CMOS process on 8-inch silicon wafer. Then, a SiO_2–Si low-temperature fusion bonding is developed to bond the CMOS wafer and the MEMS wafer, with the electrical connection realized by the tungsten through silicon via process. Wafer-level AlGe eutectic bonding is adopted to package the Pirani gauge in a non-hermetic cavity to protect the gauge from being damaged or contaminated in the dicing and assembling process, and to make it suitable for actual applications. To increase the accuracy of the test and restrain negative influence of temperature drift, the Wheatstone bridge structure is introduced. The test results show that before capping, the gauge has an average sensitivity of $1.04 \times 10^4\,K{\cdot}W^{-1}\,Torr^{-1}$ in dynamic range of 0.01–20 Torr. After capping, the sensitivity of the gauge does not decrease but increases to $1.12 \times 10^4\,K{\cdot}W^{-1}\,Torr^{-1}$.

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With the wide application of the vacuum technology,[1–3] the vacuum measure becomes more and more important, and all kinds of micro-Pirani vacuum gauges[4–17] have been widely investigated because of their wide measurement range, high sensitivity, and low power consumption.[15] Compared with other pressure measurements, such as the helium leak test and the monitoring of Q-factor variation,[18] the Pirani gauge is convenient and has higher pressure sensitivity. The MEMS Pirani gauge also makes it possible to integrate with the complementary metal oxide semiconductor (CMOS) processing circuit to reduce size and cost.

A number of micro-Pirani gauges have been reported as summarized in Table 1. Firstly the structure of Pirani gauges are mainly based on Pt, poly-Si, Ni, or W resistors on a dielectric membrane, or the poly-Si microbridge. Li *et al.*[17] presented a Pirani gauge fabricated on the silicon-on-insulator (SOI) wafer with 1.4 μm silicon. However, most of these processes are not compatible with the other MEMS devices that work in a vacuum environment and need *in situ* vacuum measurement, such as inertial and resonator sensors fabricated by the thick-layer process. In 2005, Chae *et al.*[14] presented a silicon-on-glass (SOG) structure and a monocrystal silicon heater Pirani gauge with dual heat sinks fabricated by the dissolved wafer process (DWP). However, the SOG structures are not compatible with the CMOS process. Moreover, the Pirani gauges mentioned above are all difficult to utilize because the fragile comb structure is usually damaged and contaminated in the wafer-dicing and assembling process.

In this study, we present a thick silicon-on-insulator (SOI) structure Pirani gauge with monocrystal silicon as the suspended heaters and heat sinks fabricated by the post-CMOS MEMS process. To resolve the damaging and contaminating issue, AlGe eutectic bonding was developed to bond a cap wafer to the device wafer to package the gauge in a non-hermetic cavity and to protect the MEMS structure. In addition, to increase the accuracy of the test and reduce the effects of temperature drift, a Wheatstone bridge structure was introduced and the heaters were used as the arms of the bridge.

The working principle of the Pirani vacuum gauge is that its heat-sensitive resistance is influenced by the thermal conductance, which varies with the vacuum pressure. The total thermal conductance $G_{\rm Total}$ of the heater includes that from the heater to the heat sink through gas $G_{\rm Gas}$, that from the heater to the substrate through the anchor of heater ($G_{\rm Solid}$), and the thermal radiation through the surface of the heater ($G_{\rm Radiation}$).[7,17] The curve of thermal conductance G versus pressure P is shown in Fig. 1. The test sensitivity and the low limit of the dynamic range are determined by the slope of the curve of G versus P and ratio of $G_{\rm Gas}$ to $G_{\rm Solid}$, respectively.[6,8]

The Wheatstone bridge structure with four meander-shaped monocrystal silicon resistors is shown in Fig. 2. The total length of a meander-shaped resistor is 2528 μm. The width and thickness of the

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**Corresponding author. Email: jiaobinb@ime.ac.cn
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resistors are designed as 4 μm, and 30 μm, respectively. The thickness of the resistors is determined by the MEMS wafer thinning process. The resistivity of wafer adopted for the MEMS structure fabrication is 0.02 Ω·cm. The resistance of the heaters at atmosphere and temperature coefficient of resistance (TCR) were measured to be 4.6 kΩ and 0.0015℃$^{-1}$, respectively. Suspended heaters (R_T) and dual lateral heat sinks with 2 μm gap to heaters were designed to increase the ratio of G_{Gas} to G_{Solid} to improve the performance of the gauge. By contrast, R_0 is positioned on the substrate, which leads to the large thermal conductance, thus its temperature varies slightly and its resistance is nearly unchanged.

Table 1. Summary of previous Pirani gauges.

Researchers	Structure	Material	Size	CMOS compatible	Thick layer MEMS Compatible	Packaged
Shie *et al.*[4]	dielectric membrane	platinum	Area 325 μm×325 μm	No	No	No
Stark *et al.*[5]	dielectric membrane	platinum	Area 100 μm×100 μm	No	No	No
Wang *et al.*[6]	dielectric membrane	platinum	Area 571 μm×280 μm	No	No	No
Zhang *et al.*[7]	dielectric membrane	Poly-Si	Area 88 μm×88 μm	Yes	No	No
Grau *et al.*[8]	dielectric membrane	Nickel	Area 300 μm×88 μm	No	No	No
Wang *et al.*[9]	dielectric membrane	Tungsten	Area 40 μm×40 μm	Yes	No	No
Mastrangelo *et al.*[10,11]	Microbridge	poly-Si beam	$L \times W \times D$ 400 μm×3 μm×1 μm	Yes	No	No
Stark *et al.*[12]	Microbridge	poly-Si beam	L 1000 μm	Yes	No	No
Mitchell *et al.*[13]	Microbridge	poly-Si beam	L 150–1000 μm	Yes	No	No
Chae *et al.*[14]	Microbridge (SOG)	p++ silicon coil	Area 2 mm×2 mm No L, W and D	No	Yes	No
Jiang *et al.*[15]	Microbridge (SOG)	p++ silicon coil	$L \times W \times D$ 3.5 mm×25 μm×80 μm	No	Yes	No
Topalli *et al.*[16]	Microbridge (SOG)	p++ silicon coil	$L \times W \times D$ 40 mm×28 μm×100 μm	No	Yes	No
Li *et al.*[17]	Microbridge (SOI)	p++ silicon	$L \times W \times D$ 336 μm×3 μm×1.4 μm	Yes	No	No
Presented	Microbridge (SOI) Wheatstone bridge	p++ silicon coil	$L \times W \times D$ 2528 μm×4 μm×30 μm	Yes	Yes	Yes

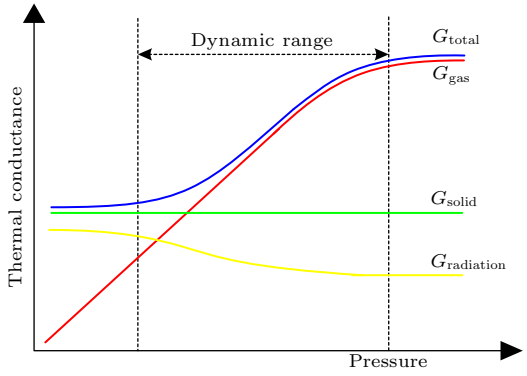

Fig. 1. Thermal conductance G versus pressure P. The scales of the X, Y coordinate axes are logarithmic.

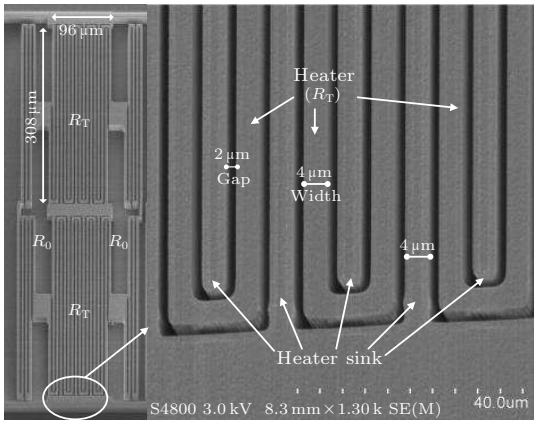

Fig. 2. SEM image of the Pirani gauge.

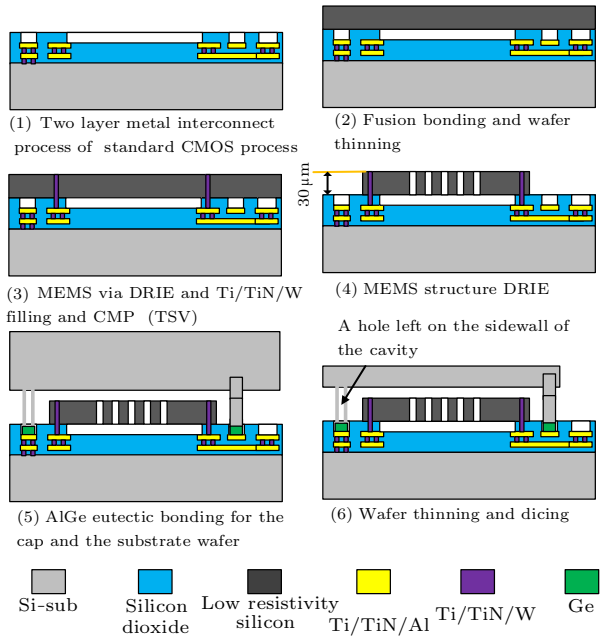

Fig. 3. Fabrication process of the Pirani gauge.

The sensor was fabricated with the post-CMOS MEMS process, as shown in Fig. 3. (1) The two-layer metal interconnection process of the standard CMOS process was used. Each layer metal interconnection process includes silicon oxide deposition, contact via hole patterning and etching, Ti/TiN/W filling and chemical mechanical polishing (CMP), Ti/TiN/Al metal sputtering and patterning, and si-

licon oxide deposition and CMP. Then, the top layer oxide was patterned to open the regions for the bonding ring, test pad, contact via, and through silicon via (TSV) etching stop layer. The first contact via to the substrate was used for electrostatic shielding. The first metal layer was used only as an electrical interconnection, and the second metal layer was used for many purposes, such as eutectic bonding material, test pads and some interconnect lines, and TSV etching stopping layer. (2) The SiO_2–Si fusion bonding process was developed to bond the CMOS wafer and the low electrical resistivity wafer (0.02 Ω·cm) used for the MEMS structure fabrication. Then, the top silicon was ground down to 30 μm. (3) The 3 μm TSV holes were made by the deep reactive etching process (DRIE). Then, the via holes were filled with Ti/TiN/W and polished by CMP on the top silicon. (4) The MEMS structure was fabricated with the trenches defined by the DRIE process. The 8 inch wafer after the DRIE etching is shown in Fig. 4. (5) The substrate wafer was further bonded to a cap wafer to package the gauge in a small non-hermetic chamber with a hole left on the bonding ring with the wafer-level AlGe eutectic bonding. The upper cap wafer was ground down to 200 μm. The test pad area was opened by the dicing and peeling process. Then the die was diced to 1.2 mm×1.4 mm square as shown in Fig. 5. Finally, the die was assembled on the printed circuit board (PCB).

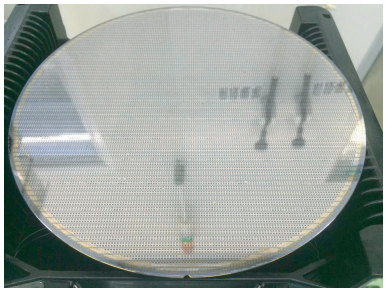

Fig. 4. Photograph of the 8 inch wafer of Pirani gauges before wafer level packaging.

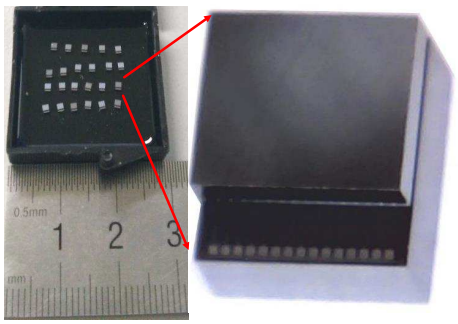

Fig. 5. Photograph of Pirani gauges after packaging and dicing.

The gauge was tested both before and after capping with the TTPX vacuum probe station (Lake Shore Cryotronics Inc.) and an Agilent semiconductor parameter 4155B. The schematic diagram of the test system is illustrated in Fig. 6. The curves of thermal impedance ($R_{\rm thermal} = \Delta T/P$) and the relative change of heater resistance ($R_{\rm T}/R_{\rm T0}$) versus vacuum pressure are presented in Fig. 7. Because $R_{\rm T}/R_{\rm T0}$ is proportional to temperature increase (ΔT), the curves of $R_{\rm T}/R_{\rm T0}$ versus pressure and $R_{\rm thermal}$ versus pressure have similar tendency. In the dynamic range (0.01–20 Torr), the resistances of $R_{\rm T}$ with a cap ($R_{\rm cap}$) and without a cap ($R_{\rm n-cap}$) change by 38.7% and 34.8%, respectively, and the average sensitivities, obtained at the middle of the dynamic range, are $1.12\times10^4\,{\rm K\cdot W^{-1}Torr^{-1}}$ and $1.04\times10^4\,{\rm K\cdot W^{-1}Torr^{-1}}$, respectively. Therefore, after wafer level packaging, the Pirani gauge has a greater sensitivity. As shown in Fig. 1, the thermal conductance $G_{\rm Total}$ consists of $G_{\rm Gas}$, $G_{\rm Solid}$, $G_{\rm Radiation}$. At low pressure, $G_{\rm Radiation}$ cannot be ignored, because the temperature of the heater is very high. After the wafer level capping, the thermal radiation can be reflected by the cap and returns to the heater, and the cap can also radiate heat to the heater. In other words, the thermal impedance through the thermal radiation increased, thus the total thermal impedance increased, which leads to the increase of measure sensitivity and dynamic range, as shown in Fig. 7.

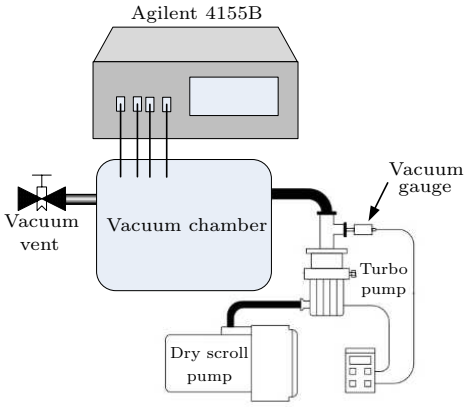

Fig. 6. Schematic diagram of the test method.

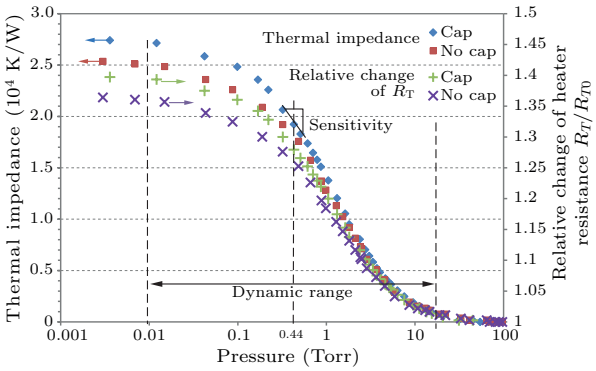

Fig. 7. Thermal impedance and relative change of the heater resistance versus the pressure of the Pirani gauge with and without a cap.

In summary, we have presented a micro-Pirani vacuum gauge with the low-resistivity monocrystal si-

licon as the heaters and heat sinks fabricated using a CMOS-compatible MEMS process. A Wheatstone bridge structure is designed to amplify the measurement signal to achieve high test accuracy. The Si–SiO_2 fusion bonding and AlGe eutectic bonding are developed to bond the CMOS substrate wafer and the cap wafer to the MEMS wafer, respectively. The tungsten TSV process is developed to realize the electrical connection of the CMOS wafer and the MEMS wafer. With this process, the IC process circuit can be fabricated on the CMOS wafer, thus greatly reducing the cost and the size of the chip. Another advantage of this process is that the MEMS structure is packed in a chamber, and thus it could undergo the wafer-dicing process without damage or contamination. Therefore, this device is a promising one to be utilized in practical application.

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