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Controllable Fabrication of GeSi Nanowires in Diameter of About 10 nm Using the Top-Down Approach *

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Ordered GeSi nanowires with a ∼10 nm cross section are fabricated utilizing top-down and Ge condensation techniques. In transmission electron microscopy measurements, the obtained GeSi nanowires exhibit a single-crystal structure and a smooth Ge/SiO_2 interface. Due to the linear relationship between the cross-section area and the initial pattern size under the self-limited oxidation condition, the cross-section size of GeSi nanowires can be precisely controlled. The Raman spectra reveal a high Ge fraction (up to 97%) and a biaxial strain of the GeSi nanowires. This top-down technique is promising for fabrication of high-performance GeSi nanowire based optoelectronic devices.

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Low-dimensional semiconductor structures with their size comparable with the Bohr radius of excitons can exhibit a quantum confinement effect and have come through a true revolution in the development of high-performance semiconductor materials and devices.[1,2] Recently, GeSi nanowires have attracted much attention not only for novel fundamental physics,[3] but also for their promising device applications, such as photodetectors,[4,5] field-effect transistors[6,7] and spin-orbit qubit for long-distance quantum communication.[8,9] In these applications, a strong and precise coupling between GeSi nanowire and optoelectronic structure is necessary to magnify the internal physical interaction. To realize the precise coupling between GeSi nanowire and optoelectronic structure, enormous effort has been devoted to the fabrication of well-controlled GeSi nano structures.

There are mainly two ways towards the well-controlled GeSi nanowires. One is the ordered nanostructure grown by self-assembled techniques on patterned substrates. Shan *et al.* demonstrated that Si nanowires can be grown with a nanochannel-template-guided 'grow-in-place' approach and used in-place for resistor and transistor fabrication.[10] However, the fabrication process of these silicon nanowires is not compatible with the sophisticated Si integration technology. The other is to fabricate these nanostructures using the top-down approach. Ilya *et al.* reported small Si quantum dots created by electron beam lithography (EBL), inductively coupled plasma (ICP) etching and subsequent oxidation.[11] Tezuka *et al.* proposed a Ge condensation technique based on high-temperature oxidation of a GeSi layer on a silicon-on-insulator (SOI) layer, wherein Ge atoms from the GeSi layer were condensed into the SOI layer to form a GeSi layer with higher Ge content.[12–14] GeSi nanowire structures with Ge content ∼92% and diameter ∼35 nm were fabricated utilizing a Ge condensation technique by Irisawa *et al.*[15] However, the lateral size of nanowires is still larger than the Bohr radius (∼24 nm) of excitons in Ge materials. Thus the quantum confinement effect in these structures is hard to observe.

In this study, we focus on the controllable fabrication of small diameter GeSi nanowires using top-down and Ge condensation techniques. The site and shape of GeSi nanowires are defined by electron beam lithography and plasma etching. Ordered GeSi nanowires with a ∼10 nm cross section are fabricated. The cross-section size of GeSi nanowire can be precisely controlled by appropriately choosing the initial wall width and oxidation time. The Raman spectra show that the Ge fraction in ordered nanowires can be up to 97%.

The fabrication process of ordered GeSi nanowires is shown in Figs. 1(a)–1(c). An SOI wafer with a 50-nm top Si layer and a 3000-nm-thick buried oxide (BOX) layer is used as the starting substrate. Then a 10-nm-thick Si buffer layer and a Ge_xSi_{1-x} layer (15-nm-thick for sample A with $x = 0.1$ and 30-nm-thick for sample B with $x = 0.2$) are grown using a molecule beam epitaxy (MBE) system. Finally, a 10 nm Si cap layer is deposited to prevent the Ge element running off during the subsequent thermal oxidation. The array line patterns are fabricated on GeSi/SOI substrates using EBL (Vistec EBPG 5000 Plus) and ICP etching (Oxford PlasmaLab 100). The width of fabricated GeSi walls varies from ∼10 nm to ∼90 nm, and the etch depth of the GeSi walls is ∼95 nm. The GeSi walls are put through the cyclic oxidation (20 min) /annealing (20 min) process at 900℃ (6 cycles for sample A and 12 cycles for sample B). According to the Ge condensation theory, thermal oxidation will induce

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a shrinking of the GeSi cores inside the walls and an increase of Ge concentration of the GeSi cores because Ge atoms are rejected from the oxide while Si is still not fully oxidized. Figure 1(d) shows the SEM image of lateral ordered nanowires covered by oxide.

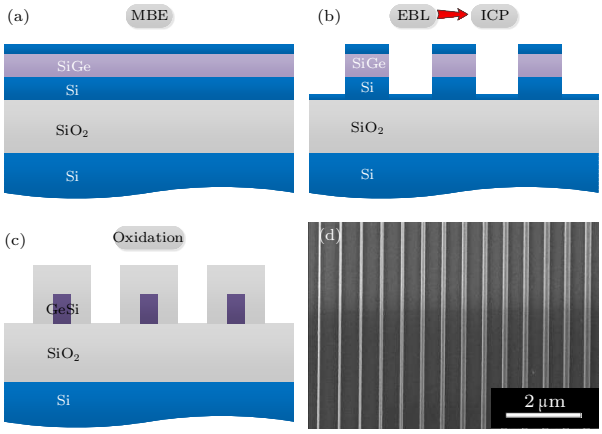

Fig. 1. The fabrication process of GeSi nanowires. (a) Growth of GeSi quantum well structure using molecule beam epitaxy (MBE). (b) Definition of GeSi walls using EBL and ICP etching. (c) The cyclic oxidation/annealing process at 900℃. (d) The SEM image of lateral ordered nanowires covered by oxide.

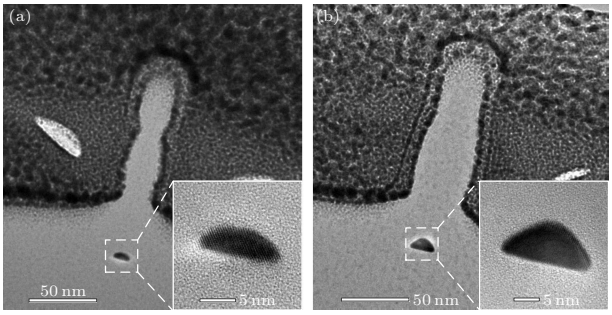

Fig. 2. HRTEM images of the cross section of GeSi nanowires from sample A. The structures are covered by gold and platinum layers prior to cutting. The initial widths of GeSi walls before oxidation are 15 nm (a) and 29 nm (b), respectively. The insets in (a) and (b) show the enlarged HRTEM images of nanowires.

The cross sections of the oxidized GeSi walls from sample A are visualized using a high-resolution transmission electron microscope (HRTEM, Tecnai G2 20 U-TWIN), as shown in Figs. 2(a) and 2(b). The GeSi walls turn into an oxide wall after the oxidation, with a shrinking GeSi core located at the bottom of the oxide wall. The insets in Figs. 2(a) and 2(b) show cross sections of triangle-shaped nanowires. The GeSi core exhibits a lattice image of a single crystal and smooth GeSi/SiO_2 interfaces. It is also confirmed from the electron-beam diffraction that the crystal orientation of the GeSi lattice is the same as that of the initial SOI lattice. The approximate dimensions of cross section of GeSi nanowires in Figs. 2(a) and 2(b) are 11 nm × 4 nm and 17 nm × 8 nm, respectively. The area of the shrinking GeSi core is about 3% of the area of GeSi walls' cross section before the oxidation process.

Figure 3 shows the HRTEM images of the cross section of arrays of nanowires from sample B, which are covered by a layer of oxide and platinum. All GeSi cores shrink to the bottom part of the oxidized GeSi walls and exhibit a perfect single crystal line of GeSi alloy. During the Ge condensation process, Ge atoms are ejected from the interface between the surface oxide and the SiGe layers into the SiGe substrate. The Ge atoms in the pileup regions diffuse rapidly into the Si layer and are effectively blocked by the buried oxide layer. The GeSi and Si on insulator are merged into a uniform GeSi region by interdiffusion between Si and Ge during the thermal oxidation/annealing processes. As a result, the Ge content in the nanowire increases while the cross section area of the nanowire shrinks.

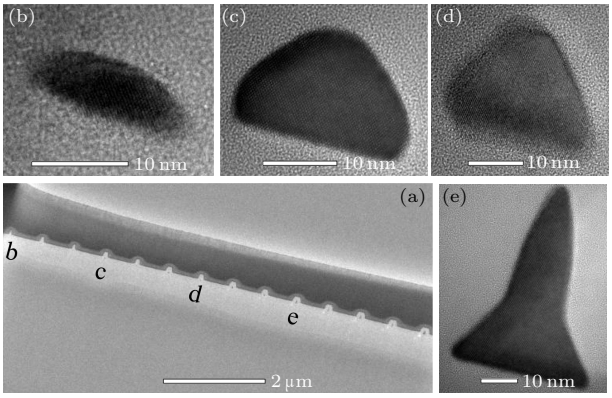

Fig. 3. (a) The HRTEM images of a cross section of arrays of nanowires from sample B, which are covered by a layer of oxide and platinum. The initial walls' width in (a) are 24 nm (b), 55 nm (c), 60 nm (d) and 74 nm (e), respectively. The fuzzy interface of (d) may be due to the measurement error.

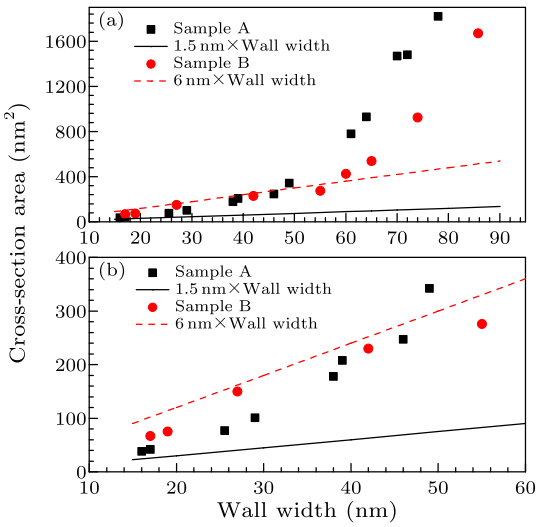

Fig. 4. (a) The cross-section area of GeSi nanowires as a function of initial width of GeSi walls. (b) The enlarged graph in (a) for nanowires with small initial wall width. The dashed lines represent the ideal cross-section area of GeSi nanowires in samples A and B after a sufficient oxidation.

Figure 4(a) shows the cross-section area of GeSi nanowires as a function of the initial width of GeSi

walls before oxidation. For small nanowires with small initial wall width (wall width $W \leq 55\,\text{nm}$), there is a linear relationship between the cross-section area and the initial wall width. A sudden increase of the cross-section area is observed when the initial wall width becomes larger. Notice that sample B experienced twice the oxidation time of sample A, but the cross-section area of small nanowires in sample B did not further shrink under the longer oxidation time. This may be due to the effect of self-limited oxidation.[16] The self-limiting oxidation of GeSi layers is reported by many research groups.[12–17] Tezuka *et al.* showed that oxidation was self-limited because the oxygen radical could not pass through the strained oxide layer.[13] According to the simulation of Shanavas *et al.*,[18] GeO_2 transforms reversibly to a denser and higher-coordinated Ge-O monoclinic phase under high-pressure and high-temperature condition, which may stop the oxygen from passing though the oxide layer surrounding the GeSi core. The strain in the surrounding oxide layer usually becomes higher when the surface has a large curvature.[19]

Due to the effect of self-limiting oxidation, ideally the oxidation of Ge atoms stops once the Si atoms are fully consumed, and the amount of Ge is conserved before and after the oxidation.[20] Then the cross-section areas of GeSi nanowires in sample A (S_A) and sample B (S_B) after a sufficient oxidation can be express as

$$S_\text{A} = 0.1 \times 15\,\text{nm} \times W, \tag{1}$$

$$S_\text{B} = 0.2 \times 30\,\text{nm} \times W. \tag{2}$$

As shown in Fig. 4(b), the cross-section area of small nanowires in sample B is close to the ideal situation, meaning that the Ge content of these nanowires may be close to unity. Small nanowires in sample B have already reached the self-limited oxidation condition. The cross-section area of small nanowires in sample A is still larger than the ideal situation, meaning that the Ge content of these nanowires is not very high. A longer oxidation time is needed to finally reach a self-limited oxidation condition.

Figure 5 shows a series of Raman spectra for different GeSi nanowires in sample B, using a 532-nm laser as the excitation source. From the Raman spectra, the values of Ge fraction x in the GeSi nanowires can be determined. When the intensity of Si-Si peak in the GeSi nanowires is larger than those of Si-Ge and Ge-Ge peaks and it is suggested that Ge fraction x should be less than 0.5 in the GeSi layer, the values of Ge fraction are evaluated from the peak positions of Si-Si and Si-Ge modes in the GeSi nanowires. When the intensity of the Ge-Ge peak in the GeSi nanowires is much stronger than that of the Si-Si peak, indicating that the Ge content is larger than 0.5, the values of Ge fraction can be calculated from the ratio of the integrated intensities between the peaks of Si-Ge and Ge-Ge modes in the GeSi nanowires.[21] The calculated results of Ge fraction in Figs. 5 (a)–5(c) are 50.7%, 71.5% and 97%, respectively.

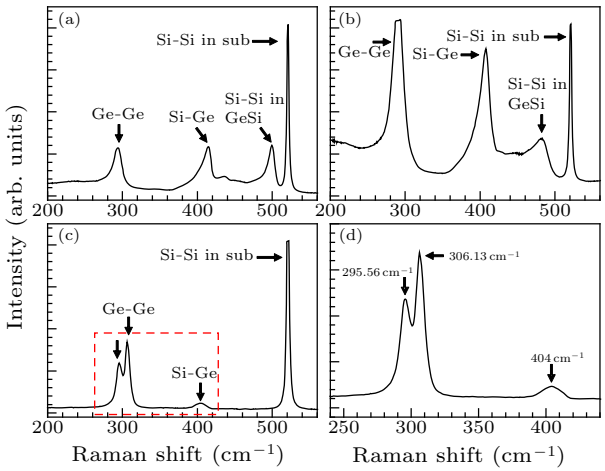

Fig. 5. A series of Raman spectra for different GeSi nanowires in sample B, using a 532-nm laser as the excitation source. The initial wall width of these GeSi nanowires before the Ge-condensation process are (a) 74 nm, (b) 60 nm, and (c) 46 nm. (d) The enlarged Raman spectrum in (c).

Figure 5(d) shows the enlarged Raman spectra in Fig. 5(c). It is worth noting that there are two Ge-Ge peaks for the nanowires with Ge fraction of 97%, locating at $295.56\,\text{cm}^{-1}$ and $306.13\,\text{cm}^{-1}$, respectively. As is known, the strain-free bulk Ge exhibits the first order optical phonon peak at $300.5\,\text{cm}^{-1}$. An application of stress to the bulk Ge can cause a shift of Ge-Ge peak position to be linearly dependent on the strain. The relation of the shift in the Raman spectrum and uniaxial strain is given by

$$\Delta\omega \cong -k \times \varepsilon_{||}, \tag{3}$$

where $\Delta\omega$ represents the shift in peak position, k is a proportionality factor, and $\varepsilon_{||}$ is the strain in the $\langle 111 \rangle$ direction. The value of k is about $434\,\text{cm}^{-1}$ according to the previous report of Ge nanowires.[22]

If we assume that the Ge fraction in Fig. 5(d) is unity, the shifts of two Ge-Ge peaks correspond to a tensile strain of about 1.14% and a compressive strain of about 1.3%, respectively. This result shows that there is a biaxial strain inside the Ge nanowire. The compressive strain is caused by the Ge condense process: the Si atoms are replaced by Ge atoms rejected from the oxide layer, then the GeSi and Si layers are merged into a uniform GeSi layer by inter-diffusion between Si and Ge atoms. If the lattice constant does not change through the oxidation process, which is equal to that of Si, the compressive strain in the Ge lattice after oxidation should be 4.2%. Thus the compressive strain values evaluated in the Ge nanowire of 1.3% mean that the strain of 2.9% was relaxed mainly by plastic deformation of the surrounding oxide layer. The cause of the tensile strain may partially be caused by the difference of thermal expansion between Ge nanowire and the surrounding oxide layer. Further research is needed to reveal the dominant mechanism of the tensile strain.

In summary, we have demonstrated the controllable fabrication of ordered GeSi nanowires using top-

down and Ge condensation techniques. Ordered GeSi nanowires with a ∼10 nm cross section are fabricated. The GeSi nanowires exhibit a single crystal lattice image and smooth GeSi/SiO_2 interfaces. By appropriately choosing the initial GeSi wall width and oxidation time, we can precisely control the cross-section size of GeSi nanowires. The Raman spectra prove that the Ge fraction in ordered nanowires can be up to 97%. However, further research is needed to reveal the mechanism of the complex biaxial strain. This fabrication method of ordered GeSi nanowires is compatible with the sophisticated Si integration technology, and will open up tremendous opportunities for the realization of a wide range of GeSi nano-structures-based optoelectronic devices.

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