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Strain Engineering for Germanium-on-Insulator Mobility Enhancement with Phase Change Liner Stressors *

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We investigate the strain in various Ge-on-insulator (GeOI) micro-structures induced by three phase-change materials (PCMs) ($Ge_2Sb_2Te_5$, Sb_2Te_3, GeTe) deposited. The PCMs could change the phase from amorphous state to polycrystalline state with a low temperature thermal annealing, resulting in an intrinsic contraction in the PCM films. Raman spectroscopy analysis is performed to compare the strain induced in the GeOI micro-structures by various PCMs. By comparison, Sb_2Te_3 could induce the largest amount of tensile strain in the GeOI micro-structures after the low temperature annealing. Based on the strain calculated from the Raman peak shifts, finite element numerical simulation is performed to calculate the strain-induced electron mobility enhancement for Ge n-MOSFETs with PCM liner stressors. With the adoption of Sb_2Te_3 liner stressor, 22% electron mobility enhancement at $N_{inv} = 1 \times 10^{13}\ cm^{-2}$ could be achieved, suggesting that PCM especially Sb_2Te_3 liner stressor is a promising technique for the performance enhancement of Ge MOSFETs.

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Improvements in the performance of Si MOSFETs through conventional device scaling has become incredibly challenging due to the physical limitation of device scaling as well as the increase of fabrication cost. To improve CMOS device performance in terms of on-state current, strain technology has been considered as a feasible method to increase the carrier mobility.[1] As the strain induced in a MOSFET channel could reduce both effective mass and scattering, carrier mobility is therefore enhanced, resulting in high drive current.[2−5] On the other hand, high-mobility channel materials can be taken as technology boosters in device performance improvement. Among the widely recognized high mobility materials, germanium (Ge) is a promising channel material for both high electron and hole mobilities. Furthermore, MOSFETs fabricated on Ge-on-insulator (GeOI) have better electrostatic controllability than those on Ge substrates. Therefore, the combination of strain engineering and GeOI structure could be an excellent method to improve the CMOS performance in future technology nodes.

The working mechanism of the mainstream high-stress liner stressor is the mechanical coupling between the intrinsic stress in the liner film and the channel covered beneath it, such as the silicon nitride (Si_3N_4) liner stressor on Si MOSFETs.[6−9] However, this conventional technique could only induce high channel stress at a very high annealing temperature of around 750℃–850℃, which is not suitable for Ge-based fabrication process. Therefore, a new concept of stress introduction by utilizing phase change materials (PCMs) as a liner stressor was adopted.[10] Different from the usual application of PCMs in memories, we focus on its property of volume contraction when changing phase from amorphous state to polycrystalline state at a low temperature annealing. The contracted PCM film would induce large stress in the structure beneath it, resulting in mobility and drive current enhancement.

In this study, we deposit three different PCMs on GeOI micro-structures and investigated the strain induced in GeOI substrates by Raman spectroscopy. Finite element numerical simulation is performed to study the strain profile in the PCM-stressed Ge structures. Based on the strain profile, the strain-induced mobility enhancement is also calculated, showing that PCM is a promising candidate for device performance enhancement.

Figure 1(a) shows the process flow for fabricating the GeOI micro-structure with PCM stressors. According to several references,[11,12] the strain induced in the GeOI structures increases as the thickness of PCM films increases below ∼70 nm. In our work, 50-nm-thick PCMs, including $Ge_2Sb_2Te_5$ (GST), Sb_2Te_3 and GeTe, were deposited on GeOI substrates by sputtering at room temperature. After deposition, the samples were annealed in ambient $N_2$for 20 min at the optimized temperatures of 270℃, 300℃, and 400℃, respectively. After that, different sizes of patterns were formed by photolithography followed by the wet etch in diluted HNO_3 solution. The length of the pattern is fixed at 90 μm while the width varies from 2 μm to 20 μm. The mechanism of the strain induction

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is illustrated in Fig. 1(b). The PCM changes phase from the amorphous state to the crystalline state after annealing, resulting in a volume contraction in the PCM film. This volume contraction would induce an intrinsic compression in the film. This compressive stress was then transferred to the Ge layer beneath it, as shown on the left of Fig. 1(b). After structure formation, the PCM film on the patterned region was removed and therefore, the patterns without the PCMs tend to relax. However, those regions with an unremoved PCM film were still compressively stressed in the lateral direction, leaving the patterned region laterally tensile stressed, as shown on the right of Fig. 1(b). Figure 1(c) shows the crystal structure of Sb_2Te_3.[13] Crystalline Sb_2Te_3 is a rhombohedral structure and has a large thermoelectric effect.

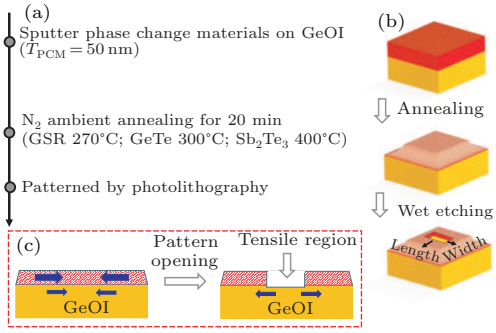

Fig. 1. (a) Process flows of structure formation. (b) Principle of stress introduction. (c) Crystal structure of Sb_2Te_3.

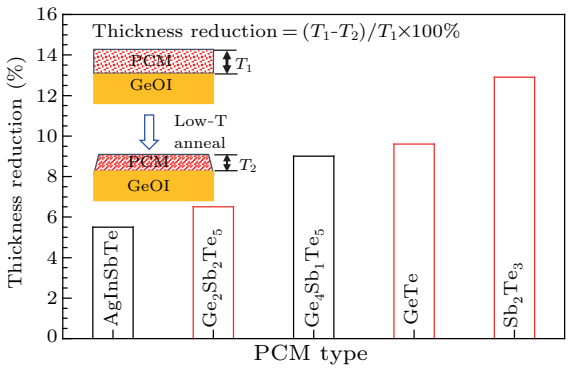

Fig. 2. Thickness reduction in percentage of different PCMs before and after annealing.

According to the previous report,[12] larger volume contraction of PCM stressor could induce larger compressive stress to the GeOI film. To achieve higher channel stress, we investigate the percentage of volume contraction for several PCM materials, as shown in Fig. 2. The volume contraction is calculated by measuring the thickness of the three PCMs before and after annealing using atomic force microscope (AFM), as illustrated in the inset of Fig. 2. As compared with other reported PCMs including AgInSbTe and $Ge_4Sb_1Te_5$, the thickness reduction in percentage for the three PCMs used in this work exhibits similar or even stronger volume contraction ability. The thickness reduction in percentage of Sb_2Te_3 reaches as high as 12.9%, indicating a strong potential for high strain induction in the transistor channel.[12,14,15]

The stresses induced by the PCMs were experimentally characterized by the Raman spectroscope to analyze the strain. Figure 3(a) shows the Ge Raman spectra of the strained patterns with length/width of 90 μm/2 μm. Compared with the Ge Raman peak on GeOI substrates without PCM capping (no strain), negative peak shifts could be observed in all the samples with PCM patterns. These results indicate that all three PCMs could induce tensile strain in the GeOI layer in the open region. Sb_2Te_3 stressor results in the largest peak shift on the GeOI layer, which is consistent with its largest thickness reduction in percentage as shown in Fig. 2. Figure 3(b) shows the average Ge peak shifts for GeOI microstructures covered by PCMs with different pattern sizes. The Raman peak shifts caused by GST and GeTe stressors are around 0.4–0.8 cm^{-1}, while the values reach 1–1.6 cm^{-1} for Sb_2Te_3 stressor. For patterns with three different sizes, Sb_2Te_3 could induce much larger peak shifts in GeOI than those induced by GST and GeTe. For patterns with the length size of 90 μm and the width length of 2 μm, the Raman peak shift reaches the maximum of 1.6 cm^{-1} for the GeOI structure stressed by Sb_2Te_3 film. As channel strain could improve the device performance in terms of mobility and I_{on}, the strain distribution in channel and mobility enhancement due to the PCMs are investigated.

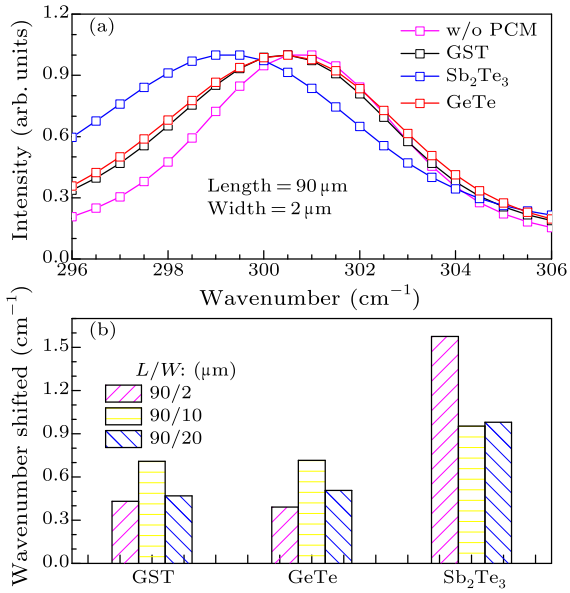

Fig. 3. Raman measurement results on GeOI structures with (a) length of 90 μm, width of 2 μm. (b) Raman peak shifts on GeOI structures with different pattern sizes.

To evaluate the effect of the strain induced by PCMs on the performance of the Ge n-MOSFET, finite element numerical simulation is carried out based on the framework of thermoelasticity. The schematic diagram of the GeOI n-MOSFETs covered by the PCM films is shown in Fig. 4(a). The geometric parameters in the simulations are provided as follows:

gate length $L_G = 150\,\text{nm}$, gate height $H_G = 100\,\text{nm}$, fin width $W_{Fin} = 10\,\text{nm}$, and fin height $H_{Fin} = 40\,\text{nm}$. The fin FET is conformally covered by a layer of PCM with a thickness T_{PCM} of 50 nm. Upon crystallization, the GST, GeTe and Sb_2Te_3 volume contract by ~6.5%, 9.6%, and 12.9%, respectively.

The boundary conditions of the model are set as follows: the upper surfaces normal to (100) plane are set to be free surfaces. The bottom surface of the substrate is fixed with the zero displacement in the vertical or [001] direction u [001]. The PCM film is allowed to relax in both S-to-D ([110]) direction and transverse fin ([$\bar{1}$10]) directions. The lateral dimensions of the buried oxide and Si substrate are set to be large enough so that the stress near the substrate boundaries is negligible compared with the stress in the channel region.

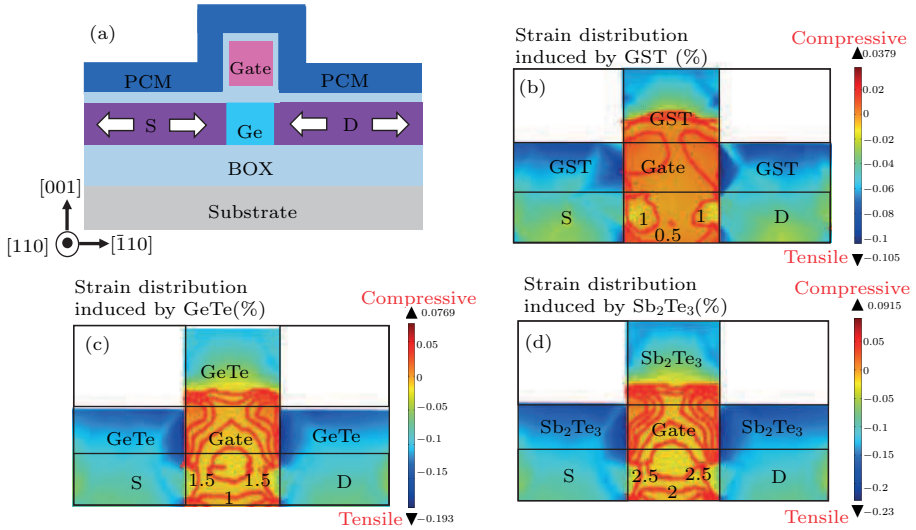

Fig. 4. (a) The 3D structure of the simplified n-MOSFET model. (b)–(d) Strain distribution along channel direction (source-to-drain direction) induced by three PCMs.

Young's modulus for Si, SiO_2, Ge, GST, GeTe and Sb_2Te_3 are taken as 131 GPa, 72.8 GPa, 103 GPa, 29.5 GPa, 58 GPa, and 63.2 Gpa, respectively.[16,17] The stiffness constants used to convert the stress tensors to the strain tensors are $C_{11} = C_{22} = 155\,\text{GPa}$, $C_{12} = 21\,\text{GPa}$, $C_{13} = C_{23} = 48\,\text{GPa}$, $C_{33} = 129\,\text{GPa}$, $C_{44} = C_{55} = 66.5\,\text{GPa}$, and $C_{66} = 41\,\text{GPa}$ at room temperature.[18] The contraction of the PCM layer was simulated using the framework of thermoelasticity.[19,20] The plane shown in Fig. 4(a) is cut through the fin along [110] or the S-to-D direction, and is 2 nm away from the fin sidewall which is close to the peak of the inversion charge density.[21] Figures 4(b)–4(d) compare the strain profiles for structures with the three PCMs in the S-to-D direction ε[110]. Here ε[110] is ~−1%, −1.5%, and −2.5% in the transistor channel region for GST, GeTe, and Sb_2Te_3, respectively.

As the strain induced in the channel could tune the semiconductor band structure, the effective mass and scattering could be reduced. To study the effect of PCM-induced strain on the transistor performance, the electron mobility at different charge densities in the inversion layer (N_{inv}) are calculated by solving the self-consistent Schrödinger and Poisson equations.[22,23] When the strain is introduced, the conduction band is changed into

$$E_c^{\nu} = E_c^{\nu_0} + \delta E_c^{\nu}, \tag{1}$$

where ν refers to different valleys (Δ_2, Δ_4, $L_\perp$, $L_{//}$), $E_c^{\nu_0}$ is the energy of the valley without strain, and δE_c^{ν} is the conduction band change induced by the strain. In the region of $N_{inv} = 1\times10^{12} - 1\times10^{13}\,\text{cm}^{-2}$, the mobility could be written as

$$\frac{1}{\mu} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}}, \tag{2}$$

where μ_{ph} is the phonon limited mobility, and μ_{sr} is the surface roughness-limited mobility. According to Ref. [24], μ_{ph} could be represented as

$$\mu_{ph} = \sum_{\nu} \frac{e}{m_c^{\nu}} \sum_{i} \langle \tau_{i,ph}^{\nu} \rangle N_i^{\nu} N_{inv}^{-1}, \tag{3}$$

$$\frac{1}{\tau_{i,ph}^{\nu}} = \frac{1}{\tau_{i,intra}^{\nu}(E)} + \frac{1}{\tau_{i,inter}^{\nu}(E)}, \tag{4}$$

where m_c^{ν} is the conduction effective mass of valley ν, $\langle \tau_{i,ph}^{\nu} \rangle$ is the momentum relaxation time of phonon scattering for ith sub-band in ν valley, N_i^{ν} is the ith sub-band electron density, $\langle \tau_{i,ph}^{\nu} \rangle$ consists of the intra valley scattering momentum relaxation time $\tau_{i,intra}^{\nu}(E)$ and μ_{sr}, and the inter valley scattering momentum relaxation time $\tau_{i,inter}^{\nu}(E)$ as shown in Eq. (4) has the similar form as μ_{ph}, which is not shown here. Since both $\langle \tau_{i,ph}^{\nu} \rangle$ and N_i^{ν} are related to δE_c^{ν},

the strain effects on mobility could be calculated as

$$\frac{1}{\tau^{\nu}_{i,\mathrm{intra}}(E)} = \sum_{j} \frac{U(E - E_{\mathrm{f}} - E^{\nu}_{\mathrm{c}})}{\tau^{\nu}_{ij,\mathrm{intra}}(E)}, \tag{5}$$

$$\begin{aligned}\frac{1}{\tau^{\nu}_{i,\mathrm{inter}}(E)} = & \sum_{j} \sum_{K}^{\{f\}} \frac{D^{f}_{i\nu\to\nu''} m_{d\nu'} D^{2}_{K}}{\hbar\rho K} \\ & \times \frac{1}{V_{ij}} \left(N_K + \frac{1}{2} \pm \frac{1}{2} \right) \\ & \times \frac{1 - f(E \mp E_K)}{1 - f(E)} \\ & \times U(E \mp E_K - E'_j - E^{\nu'}_{\mathrm{c}}),\end{aligned} \tag{6}$$

$$N^{\nu}_{i} = \frac{D_{i\nu} m_{d\nu} KT}{\pi\hbar^{2}} \ln\left(1 + e^{(\frac{E_{\mathrm{F}} - E_i - \delta E^{\nu}_{\mathrm{c}}}{kT})}\right), \tag{7}$$

where $U(x)$ is the step function, $\tau^{\nu}_{ij,\mathrm{intra}}(E)$ is the momentum relaxation time for electron from ith to jth sub-band, $D_{i\nu}$ and $D^{f}_{i\nu\to\nu'}$ are the degeneracy of valleys ν and ν', $m_{d\nu}$ and $m_{d\nu'}$ are the effective masses of valleys ν and ν', ρ is the mass density, $\frac{1}{V_{ij}}$ is the form factor, $f(E)$ is the Fermi–Dirac distribution function, plus and minus signs correspond to the phonon emission and phonon absorption, respectively.

The calculated mobilities are plotted in Fig. 5. The results show that all the three PCMs are effective in mobility improvements compared with the n-MOSFET without the PCM. Sb_2Te_3 could improve the electron mobility by 22% at $N_{\mathrm{inv}} = 1 \times 10^{13}\,\mathrm{cm}^{-2}$, which is the highest among the three PCMs considered.

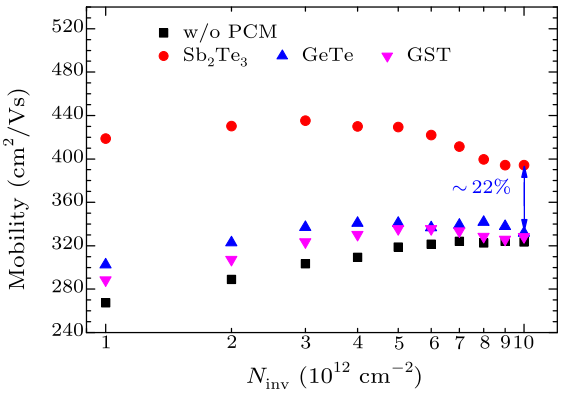

Fig. 5. Comparison of electron mobility enhancement for GeOI samples with and without phase change stressors.

In summary, the strain induced by PCMs in GeOI micro-structures has been comprehensively investigated. AFM and Raman measurements reveal the ability of $Ge_2Sb_2Te_5$, Sb_2Te_3 and GeTe in strain introduction in GeOI structures. The strain distribution in channel is about 1%–2.5% induced by the PCM films. Mobility enhancement calculations further prove the potential of PCM liner stressor in device performance improvement. The 22% mobility enhancement is achieved by Sb_2Te_3, suggesting that Sb_2Te_3 is a promising liner stressor in future CMOS applications.

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