Comparative Study of Monolayer and Bilayer Epitaxial Graphene Field-Effect Transistors on SiC Substrates *

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(Received 16 May 2016)

Monolayer and bilayer graphenes have generated tremendous excitement as the potentially useful electronic materials due to their unique features. We report on monolayer and bilayer epitaxial graphene field-effect transistors (GFETs) fabricated on SiC substrates. Compared with monolayer GFETs, the bilayer GFETs exhibit a significant improvement in dc characteristics, including increasing current density I_{DS}, improved transconductance g_m, reduced sheet resistance R_{on}, and current saturation. The improved electrical properties and tunable bandgap in the bilayer graphene lead to the excellent dc performance of the bilayer GFETs. Furthermore, the improved dc characteristics enhance a better rf performance for bilayer graphene devices, demonstrating that the quasi-free-standing bilayer graphene on SiC substrates has a great application potential for the future graphene-based electronics.

PACS: 68.65.Pq, 85.30.Tv, 72.80.Vp DOI: 10.1088/0256-307X/33/8/086801

Graphene, a two-dimensional honeycomb lattice, attracts tremendous interest due to its excellent electrical properties which make it a promising candidate for future high-speed electronics.[1–3] So far graphene electronics have developed rapidly and a graphene field-effect transistor (GFET) has delivered f_T of 427 GHz with gate length of 67 nm,[4] which begins to approach the best reported values for Si-based transistors. However, many challenges still remain to improve the performance of GFETs. For instance, GFETs always show a weak current saturation due to the existence of band-to-band tunneling current in graphene devices.[5] The origin of this tunneling current is associated with the fact that graphene does not have a bandgap. It has a negative impact on the performance of GFETs, such as transconductance (g_m) and output conductance (g_{ds}), which influence the dc and rf properties of GFETs dramatically. It is crucial to introduce a suitable bandgap in graphene to suppress the inter-band tunneling effect and further to improve the performance of GFETs.

An alternative strategy to induce bandgap is to employ the bilayer graphene. Both theoretical and experimental investigations have demonstrated that a tunable bandgap can be achieved by applying a perpendicular electric field on the surface of the Bernal stacking (AB stacking) bilayer graphene.[6,7] This kind of tunable bandgap is a unique feature of the bilayer graphene and has the advantage of maintaining intrinsic properties of the graphene channel without suffering from the damage of crystal lattice effect. Therefore, the bilayer graphene has attracted significant interest as a promising material system for graphene electrical devices. For graphene materials, epitaxial graphene (EG) grown on SiC is a promising material system for electronic device applications. The main advantage is that it allows the direct growth of large-area and high-quality graphene on an insulating substrate, which does not require transfer to other substrates. For EG on Si-face SiC, a buffer layer is formed between EG and the SiC substrate, and it limits the carrier transport in graphene. Riedl *et al.* demonstrated that the interfacial layer can be removed by intercalation of hydrogen atoms, which results in quasi-free-standing bilayer epitaxial graphene.[8] Sforzini *et al.* found that after hydrogen intercalation the epitaxial graphene shows improved electrical properties.[9] Therefore, it is reasonable to expect that removing the buffer layer will enhance graphene device performance.

In the present work, quasi-free-standing bilayer GFETs were fabricated on Si-face 4H-SiC substrates. Monolayer epitaxial GFETs were also prepared as a counterpart. The performances of the graphene devices were measured and investigated. We show that using the bilayer graphene as GFETs, channel material could provide better performance in terms of dc and rf properties, with respect to monolayer GFETs. The formation mechanism behind the improved performances of bilayer GFETs are investigated, revealing that the bilayer graphene on SiC substrates has a great potential in electronic applications for future

*Supported by the National Natural Science Foundation of China under Grant No 61306006.
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high-speed electronics.

Monolayer and bilayer epitaxial graphenes were synthesized on semi-insulating Si-face 4H-SiC substrates of 15 mm × 15 mm.[10] Before the growth of graphene, the hydrogen etch technology was used to form regular steps on the surface of SiC substrates at 1650℃ for 6 min. Monolayer epitaxial graphene was grown at 1650℃ in ambient Ar. Then, the quasi-free-standing bilayer graphene was synthesized by exposing the monolayer graphene to H_2 atmosphere at 900℃, where the so-called buffer layer between SiC and the epitaxial graphene was converted into a graphene layer. Figures 1(a) and 1(b) show the atomic force microscopy (AFM) images of the monolayer and the bilayer epitaxial graphene, respectively. Both of them reveal a series of smooth and wide terraces around 10 μm. The prepared graphene was characterized and confirmed by Raman spectra, as shown in Fig. 1(c). The full widths at half maximum (FWHM) of the 2D band are 37 cm^{-1} and 62 cm^{-1} for monolayer and bilayer graphenes, respectively. The 2D band of the bilayer graphene can be divided into four Lorentzian sub-bands, indicating that the bilayer graphene is AB stacking.[11] The as-grown monolayer and bilayer graphenes show n-type and p-type doping, respectively. Table 1 lists the electrical properties of graphene materials used in this work, which are derived directly from the Hall measurement. It can be seen that the electrical properties of the bilayer epitaxial graphene have been enhanced significantly.

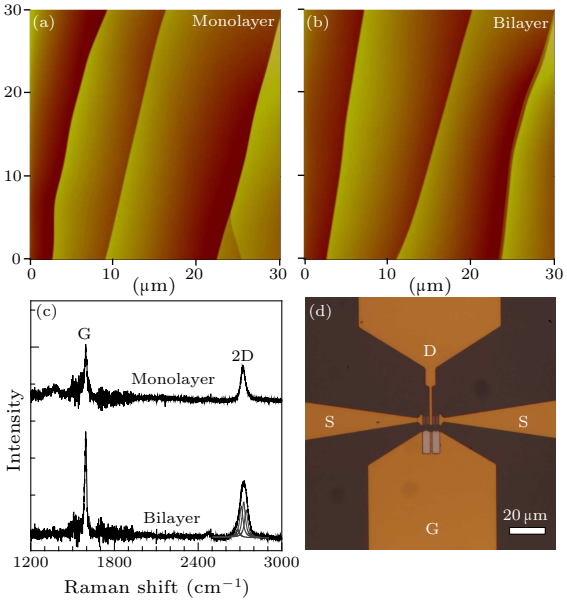

Fig. 1. (a, b) The AFM images of monolayer and bilayer graphenes on Si-face 4H-SiC, respectively. The scanning area is 30× 30 μm^2. (c) Raman spectra of monolayer and bilayer graphenes on 4H-SiC, respectively. (d) Optical micrograph of a top-gated dual-channel GFET. The scale bar is 20 μm.

Table 1. Electrical properties of graphene materials measured by the Hall test. Here n_s is the sheet carrier concentration, $\mu_{n/p}$ is the mobility, and $R_\square$ is the sheet resistance.

Sample	Carrier type	n_s (cm^{-2})	$\mu_{n/p}$ ($cm^2/V{\cdot}s$)	$R_\square$ ($\Omega/\square$)
Monolayer	Electron	7.7×10^{12}	1120	721.2
Bilayer	Hole	1.3×10^{13}	2790	166.8

Subsequent fabrication of the 100-nm gate-length devices involved an improved self-aligned process following the method in our early works[12,13] and is summarized as follows: a 20-nm Au metal film was first pre-deposited on the surface of epitaxial graphene, acting as a protection layer to avoid undesirable damage and contamination to graphene channel during processing. Then, channel regions were patterned by optical lithography. After removal of the Au film outside the channel by a KI+I_2 solution, the electrical isolation was achieved via exposure of the graphene surface to oxygen plasma. Direct-writing gates of 100 nm were obtained by electron beam lithography. Subsequently, the exposed Au film under the gates was wet etched away to form self-aligned source and drain electrodes automatically. Next, a 2 nm Al layer was deposited on the graphene surface by electron beam evaporation, which was then oxidized in air for 30 min at room temperature to form the Al_2O_3 dielectric layer. Finally, a 250 nm Al metal film was evaporated to form the gate electrodes. Figure 1(d) shows the optical micrograph of GFET with a typical top-gated dual-channel, in which the gate length L_g and gate width W_g are 100 nm and 4×2 μm, respectively.

The room-temperature dc electrical transport measurements of GFETs were conducted by a semiconductor parameter analyzer. Figures 2(a) and 2(b) show a typical output characteristic (I_{DS}–V_{DS}) for monolayer and bilayer GFETs, respectively. The value of V_{GS} changes from −1 V to 1 V with steps of 0.5 V. It is necessary to point out that to avoid the electrical breakdown of Al_2O_3 dielectric, the voltage applied in V_{GS} does not exceed ±1 V. The Dirac point of GFETs is not reached in the measurements. The monolayer graphene device shows n-type characteristic and the bilayer one shows p-type, which is consistent with the carrier-type of as-grown epitaxial graphene, indicating slight material contamination and doping during the device fabrication. As shown in Fig. 2(a), a current density I_{DS} of 1.29 A/mm is obtained at $V_{DS} = 0.5$ V and $V_{GS} = 1$ V with a slight current saturation. For the bilayer graphene device in Fig. 2(b), a maximum I_{DS} as high as 2.53 A/mm is achieved at $V_{DS} = -0.5$ V and $V_{GS} = -1$ V with an obvious current saturation.

Here I_{DS} of GFETs can be approximately expressed as

$$I_{DS} = \sigma \cdot E = n_s e\mu \cdot (V_{DS}/W_{DS}), \quad (1)$$

where σ is the conductance of the graphene channel, E is the electric field between drain and source electrodes, n_s is the sheet carrier density, e is the charge of electron, μ is the carrier mobility, and W_{DS} is the space distance between drain and source electrodes. For a fixed V_{DS}, I_{DS} is proportional to the product of n_s and μ, leading to the larger I_{DS} in the bilayer GFET. The above results indicate that the current-carrying capacity of the bilayer GFET is superior to that of the monolayer graphene on SiC.

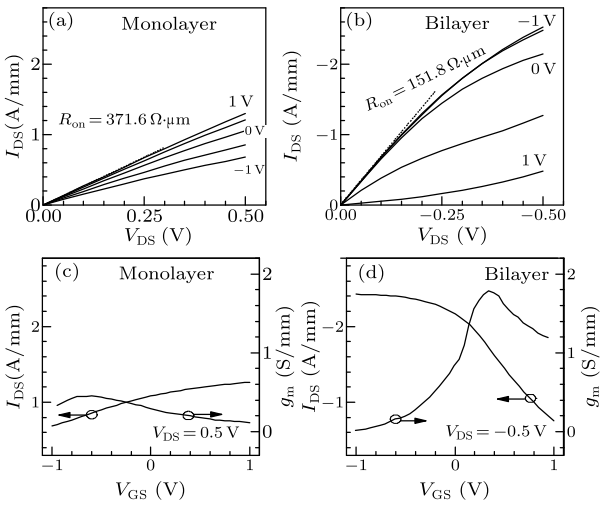

Fig. 2. The room-temperature dc characteristics of GFETs. (a, b) The output characteristics of GFETs. (c), (d) The transfer curves of GFETs, measured at $V_{DS} = 0.5$ V and $V_{DS} = -0.5$ V, respectively. $L_g = 100$ nm, $W_g = 4\,\mu$m.

The on-resistance R_{on} measured at $V_{GS} = -1$ V in the bilayer GFET is only $151.8\,\Omega\cdot\mu$m. The normalized contact resistance R_c between Au metal and the bilayer graphene channel is estimated to be less than $75.9\,\Omega\cdot\mu$m ($2R_c = R_{on} - R_{channel}$), which is reduced by a factor of 2.45 compared with that in the monolayer GFET ($185.8\,\Omega\cdot\mu$m). The low R_c demonstrates that using bilayer graphene can result in significantly lower contact resistance between the contact metal and graphene channel. This is mainly due to the fact that the bilayer graphene used in this work possesses higher carrier concentration as well as higher mobility, which can improve the carrier injection efficiency from metal to graphene and can reduce the ohmic contact resistance.[14] Figures 2(c) and 2(d) show the transfer curves of monolayer and bilayer GFETs with the characteristics of n-type and p-type doping, respectively. The value of g_m of the bilayer GFET reaches 1786 mS/mm at $V_S = -0.5$ V and $V_{GS} = 0.4$ V, greatly increased compared with that of the monolayer GFET (452 mS/mm at $V_{DS} = 0.5$ V and $V_{GS} = -0.6$ V). Here g_m can be expressed as

$$g_m = \mu_{n,p} \cdot C_{ox} \cdot (W_g/L_g), \quad (2)$$

where C_{ox} is the oxide capacitance, W_g is the gate width, and L_g is the gate length. It can be expected that as the carrier mobility increases, g_m will increase. Thus an improved g_m is obtained in the bilayer GFET due to the higher carrier mobility.

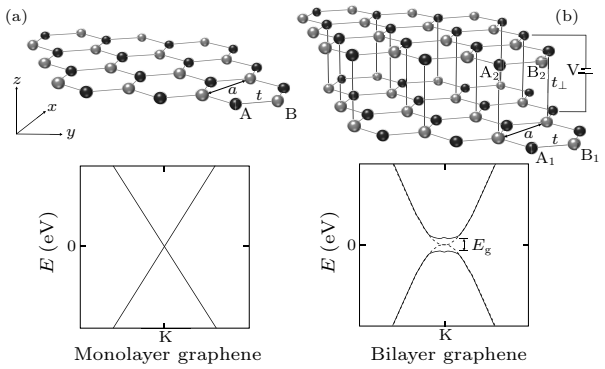

Fig. 3. (a, b) Lattice structure and band structure of monolayer and bilayer graphenes, respectively, where A, B, A_1, B_1, A_2, B_2 are the sublattices, a is the lattice constant, t is the in-plane hopping parameter, $t_\perp$ is the inter-plane hopping parameter, and V is the electrostatic potential between layers. Bilayer graphene energy gap opens at $V \neq 0$ (solid line) or closes at $V = 0$ (dashed).

From the output characteristics, it can also be seen that the current saturation is much more pronounced in the bilayer GFET compared with the monolayer one. The on-off ratio I_{on}/I_{off} is much larger in the bilayer GFET than the monolayer GFET. A tunable bandgap in the bilayer graphene is considered to be the main reason for the experimental results observed. To further investigate the phenomena mentioned above, the lattice structure and band structure for monolayer and bilayer graphenes are given, respectively, as shown in Fig. 3. The bandgap in AB stacking bilayer graphene induced by a vertical electric field can be expressed as[15]

$$E_g = \sqrt{e^2 V t_\perp^2/(t_\perp^2 + e^2 V^2)}, \quad (3)$$

where E_g is the bandgap in the bilayer graphene, V is the electrostatic potential between two graphene layers, and $t_\perp$ is the inter-plane hopping parameter ($t_\perp \approx 0.4$ eV). Due to the existence of a tunable bandgap, the band-to-band tunneling current in the bilayer GFET is better suppressed than the monolayer device, leading to a better current saturation.[5] Here I_{on}/I_{off} has a relationship with E_g,[7] which can be expressed as $I_{on}/I_{off} \propto A \cdot E_g$, where A is the fitting parameter. Thus the bilayer GFET has a higher I_{on}/I_{off} due to the existence of E_g. The above analysis indicates that the tunable bandgap in the bilayer GFET by a vertical electric field (from top-gate voltage V_{GS}) is responsible for the obvious current saturation and high I_{on}/I_{off}. However, the level of current

saturation and I_{on}/I_{off} in the bilayer GFET is not yet high enough, indicating that in our experiments the electric field-induced bandgap in the bilayer device is rather small, which is consistent with the theoretical and experimental studies in Refs. [6,16].

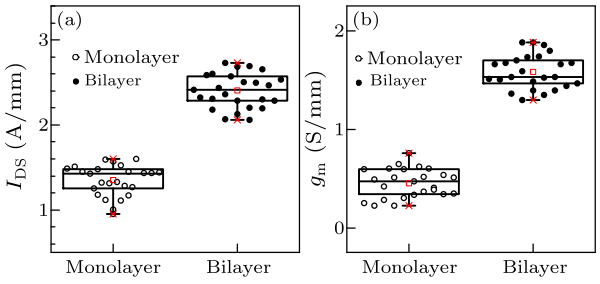

Fig. 4. (a) Statistical data of I_{DS} for monolayer (the hollow circle) and bilayer (the solid circle) GFETs, respectively. (b) Statistical data of g_m for monolayer and bilayer GFETs, respectively.

Figures 4(a) and 4(b) show the statistical distributions of I_{DS} and g_m for monolayer and bilayer graphene devices, respectively. As many as 25 devices are measured. As can be seen, a reasonable amount of variation in I_{DS} and g_m is observed, partly due to the local crystal defects and inhomogeneity of epitaxial graphene on SiC substrates.[10] Despite this variation, the results in Fig. 4 reveal the fact that the device performance is significantly improved for the bilayer GFETs. Compared with the monolayer GFETs, current densities of the bilayer graphene devices increase from an average of 1.3 A/mm to 2.4 A/mm, improved by a factor of 1.8. Transconductance improves from an average of 453 mS/mm to 1584 mS/mm, increased by a factor of 3.5. The results provide compelling evidence that bilayer GFETs on SiC exhibit excellent dc performance.

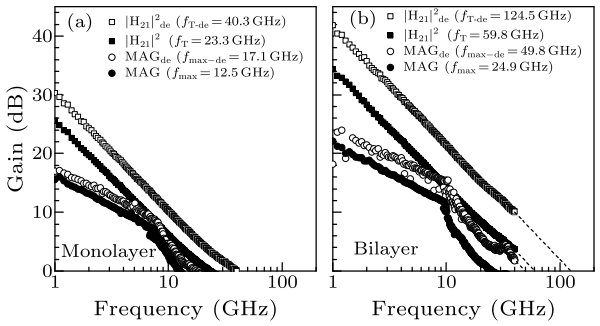

Fig. 5. (a, b) The rf characteristics of GFETs with gate length of 100 nm. For the monolayer GFET, the data are measured at $V_{DS} = 0.5$ V, $V_{GS} = -0.6$ V. For the bilayer GFET, the data are measured at $V_{DS} = -0.5$ V, $V_{GS} = 0.4$ V. The hollow squares, solid squares, hollow circles and solid circles represent the $|H_{21}|^2_{de}$, $|H_{21}|^2$, MAG_{de} and MAG, respectively.

The small-signal scattering parameters were measured from 0.1 to 40 GHz to investigate the rf characteristics of GFETs. Figures 5(a) and 5(b) show the rf properties of monolayer and bilayer GFETs with gate length of 100 nm, respectively. The data shown in Fig. 5 are current gain (H_{21}) and the maximum available gain (MAG), which consists of two portions: the direct measured and pad de-embedded data. Here a commonly used de-embedding process with 'open' and 'short' structures is adopted to exclude parasitic effects such as the pad capacitance, resistance, and inductance.[17] For the monolayer GFET, the direct measured f_T and f_{max} are 23.3 and 12.5 GHz, respectively. After pad de-embedding, f_{Tde} is 40.3 GHz and f_{max-de} is 17.1 GHz. In the case of the bilayer GFET, before de-embedding, an f_T as high as 59.8 GHz is direct measured, and the result is among the highest extrinsic f_T values (40–60 GHz) reported for GFETs.[18–20] The value of f_{max} is 24.9 GHz, which is lower than the value of f_T. After pad de-embedding, f_{Tde} and f_{max-de} are 124.5 and 49.8 GHz, respectively. These results demonstrate that the bilayer GFET possess a higher rf performance than the monolayer GFET, which are consistent with the results of dc measurement. As we know, for a well-behaved FET, the cutoff frequency f_T can be deduced by[21]

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}, \tag{4}$$

where C_{gs} is the gate–source capacitance, and C_{gd} is the gate–drain capacitance. From Eq. (4), it can be seen that f_T would increase with g_m. Hence, an improved f_T is obtained in the bilayer GFET due to the higher g_m than the monolayer GFET. Here f_{max} is another important figure of merit for rf performance, especially in the analog applications, and can be calculated by using a more complex function[21]

$$f_{max} = \frac{g_m}{4\pi C_{gs}} \cdot \frac{1}{\sqrt{g_{ds}(R_i + R_S + R_G) + g_m R_G C_{gd}/C_{gs}}}, \tag{5}$$

where g_{ds} is the differential source–drain conductance, R_i is the channel resistance under the gate, R_S is the source resistance, and R_G is the gate resistance. It can be seen that the f_{max} not only depends on intrinsic elements such as g_m and g_{ds}, but also relies on the extrinsic parasitic parameters. The larger the g_m, the smaller the R_S and g_{ds} (associated with saturation of the drain current) leading to the better f_{max} in the bilayer GFET. However, f_{max} is still lower than the one of f_T, indicating that deteriorating effects of parasitic parameters (such as R_S and R_G) have a strong influence on the f_{max} in GFETs. Therefore, to improve the power gain and f_{max}, extrinsic parasitic passive elements should be further optimized in the future work. The results reveal that the epitaxial bilayer graphene

on SiC has a great potential in rf applications. In addition, the GFETs show almost unchanged characteristics after repeated measurements and demonstrate a good stability over the course of several months. The stable material properties of graphene on SiC, together with the improved device fabrication process used in this work, are considered to be the main reason for the long-term stability of the GFETs.

In summary, the device performance of monolayer and bilayer GFETs have been measured and investigated on Si-face 4H-SiC substrates. Improved dc performances including increasing $I_{\rm DS}$, improved $g_{\rm m}$, reduced $R_{\rm on}$ and current saturation are obtained in bilayer GFETs. The higher $n_{\rm s}$, μ and a tunable bandgap in bilayer graphene are considered to be the main reason for the improved characteristics. Furthermore, the improved dc characteristics enhance a better rf performance for bilayer graphene devices. Our works demonstrate that the quasi-free-standing bilayer graphene material on SiC substrates has a great potential in the future graphene-based electronics.

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