Polymer-Sandwich Ultra-Thin Silicon(100) Platform for Flexible Electronics *

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As a potential flexible substrate for flexible electronics, a polymer-sandwiched ultra-thin silicon platform is studied. SU-8 photoresist coated on the silicon membrane improves its flexibility as shown by an ANSYS simulation. Using the plasma enhanced chemical vapor deposited SiO_2/Si_3N_4 composite film as an etching mask, a 4″ silicon-(100) wafer is thinned to 26 μm without rupture in a 30 wt.% KOH solution. The thinned wafer is coated on both sides with 20 μm of SU-8 photoresist and is cut into strips. Then the strips are bent by a caliper to measure its bending radius. A sector model of bending deformation is adopted to estimate the radius of curvature. The determined minimal bending radius of the polymer-sandwiched ultra-thin silicon layer is no more than 3.3 mm. The fabrication process of this sandwich structure can be used as a post-fabrication process for high performance flexible electronics.

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Mechanically flexible electronics is a promising field in which electronic and optoelectronic devices are fabricated on flexible substrates which can be mechanically deformed without rupture of substrates or losing the functionality of devices. It has gained increasing attention for potential applications such as artificial skin,[1] retina,[2] neural probes,[3] imaging arrays[4] and solar cells.[5] The mechanical flexibility of substrates is the key attribution of this technology. Commonly used flexible substrates are organic polymers and plastics (polyimide, parylene, silicone, etc.), on which most devices are fabricated either using transfer printing or direct monolithic patterning.[6,7] However, there are several challenges in flexible electronics applications of these organic materials such as slow information processing speed. The organic materials have less compatibility with crystalline silicon-based devices. They have low melting points which make it difficult to subject them to traditional high performance electronics fabrication processing. High temperature materials are difficult to directly fabricate.

Therefore, as a standard material in the electronics industry, silicon has attracted a second look from researchers for making pliable electronics. Different technologies have been developed for using single crystalline silicon. These include transferred substrate approaches from silicon on insulators[8] and anisotropic etching of bulk silicon-(111) wafers.[9] The most compelling reason for using silicon is its ability to host complex structures such as integrated circuits (ICs). Approaches that require unusual substrates (i.e., nanoribbons or wires, prethinned wafers, SOI, or diced wafers) make excellent research subjects, but they cannot use high-volume integrated circuit fabrication manufacturing capabilities which run on 300 mm wafers. SOI manufacturing exists, but it is more expensive and much less common than bulk. Post fabrication self-assembly imposes another set of restrictions. Flexible devices from silicon-(100) wafers were also demonstrated by using etch holes,[10] but this requires a special real-estate intensive layout.

In this Letter, we seek to modify a silicon wafer as though the front side contains an integrated circuit. By protecting the top side, relying only on low temperature processing, and not using any real estate on the wafer, the polymer-sandwiched ultra thin silicon-(100) layer is demonstrated by utilizing wet chemical etching of the back side. The silicon-(100)-based flexible sandwich structure is completely compatible with complex integrated circuits. Compared with the reported polyimide-based ultra-thin chip package technology,[11] rigid carriers are not needed, and therefore the process is simplified.

Silicon is traditionally regarded as a rigid and brittle material in its bulk form. However, according to the theory of mechanics of materials,[12] the flexibility arises due to the fact that, for a given force, the maximum beam deflection is proportional to the inverse cube of the thickness while the maximum stress is proportional to the thickness squared. Thus thinner layers can accept larger deflections without fracture. In addition, silicon membrane retaining a single crystalline structure obtained by thinning wafer presents an attractive flexible material platform for many electronic devices, especially active devices. When a thin film is bent in an arc, surface strain induced by bending film is directly proportional to the distance from the neutral bend surface, and strain vanishes at the so-called 'neutral plane'. However, the amount of bend still must be controlled. Even if devices are exactly placed on the neutral bend radius, dislocations and slip planes induced elsewhere can easily propa-

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gate through the silicon lattice to the devices. What is more, a force that could break ultra-thin silicon may easily arise during handling of the device, for example, during deployment. Therefore, a composite structure which not only protects the silicon membrane but also provides some mechanical support is desirable. SU-8 is a high-contrast, negative tone, and epoxy-based photoresist, which can be patterned by near-UV photolithography. Due to the good chemical stability, biocompatibility and mechanical properties of this photoresist, SU-8 has attracted great interest for micromachining, micro-electro-mechanical systems (MEMS) and other microelectronics applications.[13] SU-8 resist is also an excellent encapsulating material for preventing corrosion to structural materials and devices.[14] Therefore, a silicon membrane coated with SU-8 would be an attractive sandwich structure platform for flexible electronics.

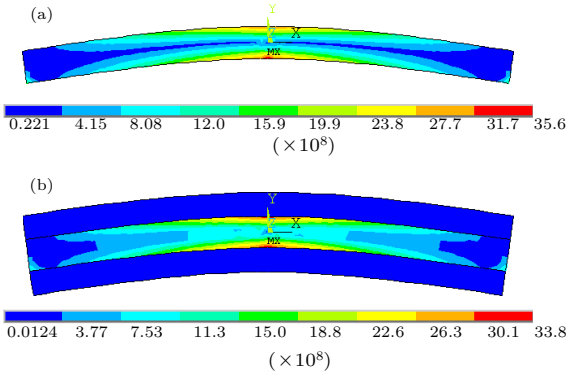

Fig. 1. Contour plot of stress intensity obtained from an FE simulation: (a) bare silicon layer, (b) sandwich structure.

To predict the mechanical effect of SU-8 polymers on a silicon membrane, a finite-element analysis was made for an SU-8 polymer-sandwiched silicon membrane and a bare silicon membrane utilizing the general-purpose FE software ANSYS 10.0. A 2D model was used for analysis. The structural models were built using element PLANE 2. The sandwich structure comprises a 26-μm-thick silicon layer and two 20-μm-thick SU-8 layers on both the sides. A bare silicon membrane with the thickness of 26 μm was also simulated. Both models are 400 μm in length. The center of silicon was fixed, and both ends were displaced by the same amount. The mechanical simulations were performed assuming linear material properties with Young's modulus $E_s = 169$ GPa and Poisson's ratio $v_s = 0.22$ for silicon,[15] and Young's modulus $E_s = 2.0$ GPa as well as Poisson's ratio $v_s = 0.222$ for SU-8 photoresist.[16]

Figure 1 shows the contour plots of the simulated stress intensity. It can be seen that the stress is concentrated in central parts of both sides of the silicon layer in both cases, and the bare silicon layer has a higher stress intensity in the central part than that in the sandwich structure. A similar result is also clearly shown in Fig. 2. It shows that the horizontal stress in the polymer-sandwiched thin silicon layer is less than that in the bare silicon layer. The ratio of the peak horizontal tensile stress (3.206 GPa) in bare silicon to that (1.626 GPa) in sandwiched silicon is about 2.0:1. This indicates that the sandwiched silicon will have a greater nominal limiting strain. These results can be attributed to the modulus mismatch between silicon and SU-8 photoresist.[6] This mismatch results in shear strain in silicon which effectively relieves the strain on the multi-layer stack surface. This means that the SU-8 resist coated on silicon membrane can not only protect the silicon membrane from corrosion but also improve its flexibility.

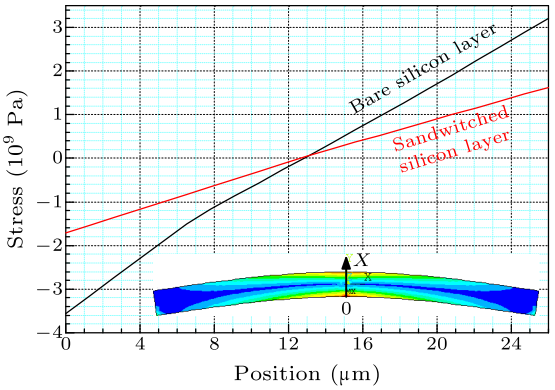

Fig. 2. ANSYS simulated through-silicon thickness horizontal stress distribution.

Silicon membrane was obtained by etching silicon wafers. The wet chemical etching of silicon in KOH solution is a commonly used and key bulk micro-machining technology for fabricating silicon microstructures.[17,18] In most cases, Si_3N_4 is deposited on the polished wafer as an etching mask. However, herein only the plasma enhanced chemical vapor deposition (PECVD) Si_3N_4 film is insufficient for obtaining the very thin silicon wafer. The tensile stress of PECVD Si_3N_4 film will result in the cracking of thin wafer. In view of the compressive stress of PECVD SiO_2 film, the PECVD SiO_2/Si_3N_4 composite film is used as the etching mask. For the purpose of obtaining the low stress and high quality SiO_2/Si_3N_4 composite film, the effect of thickness ratio of SiO_2 to Si_3N_4 on the internal stress of the composite film was studied. SiO_2 and Si_3N_4 films were prepared by PECVD using a Plasma-Therm 790. The thickness of the films was measured with a Rudolph ellipsometer MS14C2C. The stress was measured with the MAKE 900TC film stress measurement system based on Stoney's equation[19]

$$\sigma_m = \{[E_s/(1-v_s)]h_s^2\}/(6tR_{eff}), \quad (1)$$

$$R_{eff} = (RR_0)/(R_0 - R), \quad (2)$$

where σ_m is the mean thin film stress (MPa), E_s is Young's modulus of the substrate (MPa), v_s is Poisson's ratio of the substrate, h_s is the substrate thickness (μm), t is the film thickness (μm), R_{eff} is the

effective substrate radius of curvature (μm), R_0 is the initial substrate radius of curvature (μm), and R is the final substrate radius of curvature (μm).

It is found that the composite film deposited at lower temperature could not withstand a long exposure to the alkaline etch solution. For example, a film stack deposited at 100℃ delaminated after 10 min in KOH solution. However, films deposited at 340℃ could withstand extended exposure. The selected source gas parameters and working conditions for SiO_2/Si_3N_4 composite film are listed in Table 1.

The result of experiments shows that after the PECVD SiO_2 film with a certain thickness is deposited on silicon wafer, the internal stress of the PECVD SiO_2/Si_3N_4 composite film is approximately inversely proportional to the thickness of Si_3N_4 (Fig. 3), and the composite film has a minimal internal stress when the thickness ratio of SiO_2 to Si_3N_4 is close to 3:1.

Table 1. Source gas parameters and working conditions for PECVD silicon oxide and silicon nitride.

	Source gas parameters				Working conditions		
	2% SiH_4/He (sccm)	N_2O (sccm)	NH_3 (sccm)	N_2 (sccm)	Power (W)	Pressure (mtorr)	Temperature(℃)
SiO_2	200	450	–	–	20	900	340
Si_3N_4	140	–	2.5	520			

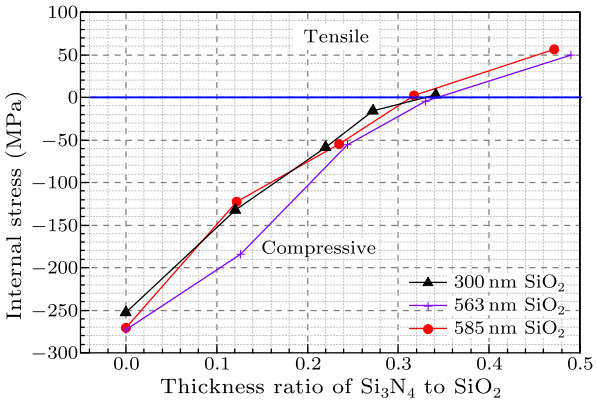

Fig. 3. Variation of the stress of PECVD SiO_2/Si_3N_4 composite film with the thickness ratio of SiO_2 to Si_3N_4.

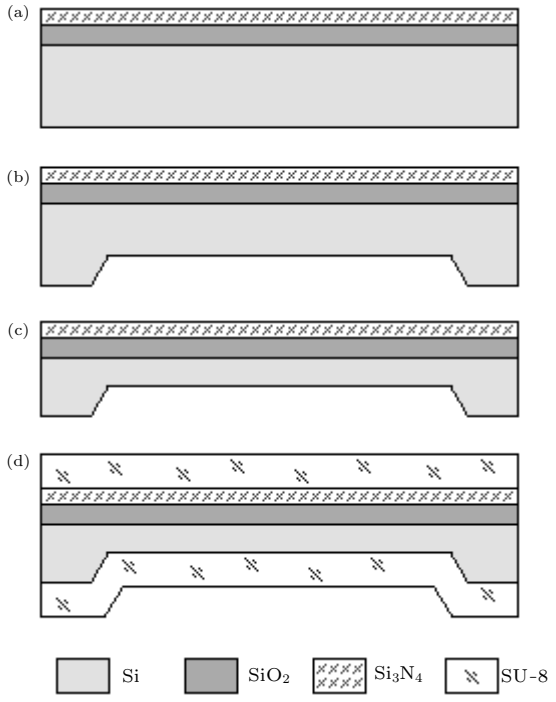

Fig. 4. Fabrication steps of silicon-based sandwich structure.

According to the above-mentioned information, we have developed a fabricating procedure to obtain a sandwich structure for flexible application. Figure 4 shows the fabrication process for silicon-(100)-based flexible sandwich structure.

First, PECVD SiO_2 of 590 nm thickness and PECVD Si_3N_4 of 210 nm thickness are deposited on p-type(100) 4″ silicon wafers on the polished side of the wafer as a composite etch mask (Fig. 4 (a)). Then the back side of the wafer is etched using the advanced micromachining tools (AMMT) wafer holder in a 30 wt.% KOH solution. To avoid wafer cracking induced by the wafer holder, etching is carried out in two steps. The wafer is first thinned to 100 μm in the holder (Fig. 4(b)). It is then removed and thinned without a holder until 26 μmm is obtained (Fig. 4(c)). The thicker wafer edge supports the thin silicon membrane for subsequent process steps. Finally, 20-μm-thick SU-8 photoresist is spin-coated on both sides of the etched wafer (Fig. 4(d)).

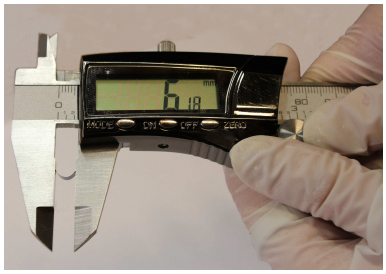

Fig. 5. Bending radius measurement of the sandwiched silicon strip.

If there are devices fabricated on the top side of the silicon film and an electrical connection is needed, vias to the contact of the devices will be easily obtained using near-UV photolithography.

The silicon-based sandwich structure was cut into strips with width of 4 mm and length of 8 mm. By utilizing a caliper, the flexibility of sandwiched silicon strips and the bare ones are compared. As shown in Fig. 5, rupture does not happen when the distance between two ends of the curved strip is 6.18 mm, while the silicon strip without polymer will rupture when the distance is 7.59 mm. These show that the sandwiched silicon strip has a better flexibility than the

bare silicon strip.

By assuming that the radius of curvature of the suspended bending silicon strip is equal everywhere, the minimal bending radius of the sandwiched silicon strip can be estimated according to the sector model shown in Fig. 6.

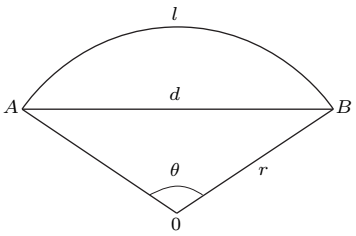

Fig. 6. The sector model of bending deformation.

Based on the geometry, the arc length of sector (l) is described by

$$l = 2\pi r \times \frac{\theta}{2\pi}, \tag{3}$$

where r and θ are the radius and the central angle of sector, respectively.

The length of chord (d) can be computed from

$$d = 2r \sin \frac{\theta}{2}. \tag{4}$$

According to Eqs. (3) and (4), we can confirm that the minimal bending radius of the sandwiched silicon strip is no more than 3.3 mm with known l and d. Based on $\varepsilon = t/2r$ (where ε is the strain, t is the thickness of thin film, and r is the bending radius)[20] and measurements, the calculated ratio of nominal limiting strain in sandwiched silicon to that in bare silicon is about 2.1:1, which is very close to the simulation result.

In summary, a silicon-(100)-based sandwich structure has been fabricated by utilizing wet etching the back side of the silicon wafer in KOH solution with a PECVD SiO_2/Si_3N_4 composite film as the hard mask. SU-8 photoresist is used to form a sandwiched structure. We find that the minimal bending radius of the sandwiched thin strip is no more than 3.3 mm. The polymer-sandwiched ultra-thin silicon strip has a better flexibility compared with the bare one. Since the SU-8 film is spin-coated on single crystalline silicon membrane in the last step of the fabrication process, this enables the integration of many high performance devices and circuits already well developed based on silicon and other high temperature materials on this flexible sandwich structure. Although the silicon film based on the sandwich structure can be easily bent without rupture, one still needs to study the effect of thickness and bending radius of the silicon film and to repeat cycling at lower stress on the performance of the devices in the film for flexible electronic technology applications in the future.

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