Influence of Post-Annealing on Electrical Characteristics of Thin-Film Transistors with Atomic-Layer-Deposited ZnO-Channel/Al_2O_3-Dielectric *

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High-performance thin-film transistors (TFTs) with a low thermal budget are highly desired for flexible electronic applications. In this work, the TFTs with atomic layer deposited ZnO-channel/Al_2O_3-dielectric are fabricated under the maximum process temperature of 200°C. First, we investigate the effect of post-annealing environment such as N_2, H_2-N_2 (4%) and O_2 on the device performance, revealing that O_2 annealing can greatly enhance the device performance. Further, we compare the influences of annealing temperature and time on the device performance. It is found that long annealing at 200°C is equivalent to and even outperforms short annealing at 300°C. Excellent electrical characteristics of the TFTs are demonstrated after O_2 annealing at 200°C for 35 min, including a low off-current of 2.3×10^{-13} A, a small sub-threshold swing of 245 mV/dec, a large on/off current ratio of 7.6×10^8, and a high electron effective mobility of 22.1 $cm^2/V{\cdot}s$. Under negative gate bias stress at −10 V, the above devices show better electrical stabilities than those post-annealed at 300°C. Thus the fabricated high-performance ZnO TFT with a low thermal budget is very promising for flexible electronic applications.

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Recently, flexible electronics have received increasing attention due to the fact that they are lightweight, thin, and bendable. As a key component for flexible electronic applications, thin-film transistors (TFTs) must be fabricated under a thermal budget as low as possible while maintaining high device performance. Although organic TFTs are very suitable for the flexible manufacture due to their low processing temperature, the low carrier mobility (<1 $cm^2/V{\cdot}s$) and ordinary reliability overshadow their device performance attributes.[1,2] Compared with organic semiconductors, ZnO is also regarded as an excellent candidate for flexible electronic application due to its high electron mobility, low processing temperature, high transparency for visual light and excellent environmental stability.[3,4] Among various preparation methods of ZnO films, the atomic-layer-deposition (ALD) technique can ensure excellent thickness uniformity, nearly stoichiometric composition and relatively low deposition temperature. These make it very attractive for the TFT fabrication on a flexible substrate. However, the ALD ZnO films generally have a very high carrier concentration, thus the ZnO-channel of TFT is conductive even in the absence of an applied gate voltage.[5] This makes the ZnO TFT unable to work in a normal mode. To solve this issue, some strategies have been attempted to reduce the carrier concentration in the ZnO channel to improve the device performance.[6–10] Unfortunately, they either require a high annealing temperature (400℃),[3,10] or improve the device performance slightly.[6–9] Therefore, it is imperative to explore low temperature fabrication of high-performance ZnO TFTs for flexible electronic applications.

In this Letter, the TFTs with ALD ZnO-channel/Al_2O_3 -dielectric were fabricated under the maximum processing temperature of 200℃. In particular, O_2 post-annealing at 200℃ was investigated intensively. As a result, excellent device performance has been achieved, such as a large on/off current ratio, a high electron effective mobility, a small sub-threshold swing and good electrical stabilities under negative gate bias stressing (NGBS).

A low resistivity p-type (100) silicon substrate was used as the back gate electrode of TFTs. After standard RCA cleaning, a 50-nm Al_2O_3-dielectric layer and a 37-nm ZnO active layer were deposited in turn by ALD at 200℃ without breaking the vacuum. Herein, the precursors for ALD Al_2O_3 and ZnO films were $Al(CH_3)_3/H_2O$ and $Zn(C_2H_5)_2/H_2O$, respectively. Subsequently, the active layer of ZnO was defined by photolithography, and was formed by wet etching with diluted HCl solution. Then, the source and drain contacts of the 100-nm Mo layer were formed by sputtering and a lift-off process. After that, the device was first annealed in N_2, N_2-H_2 (4%) and O_2, respectively, to improve and optimize its performance. Then, the environment of O_2 was selected as a perfect annealing environment, and the influences of annealing temperature and time on the electrical characteristics of the device were studied comprehensively, especially at the temperature as low as 200℃.

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The thicknesses of the deposited ZnO and Al_2O_3 films were determined by an ellipsometer (Sopra GESSE, France). The texture of the ZnO film was characterized with x-ray diffraction (XRD). The electrical characteristics of the TFTs were measured with a semiconductor device analyzer (B1500A, Agilent Technologies, Japan) at room temperature in a dark box.

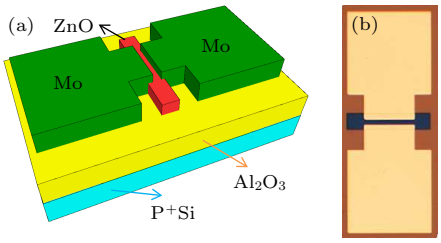

Fig. 1. Schematic diagram (a) and optical top view (b) of the fabricated TFT device.

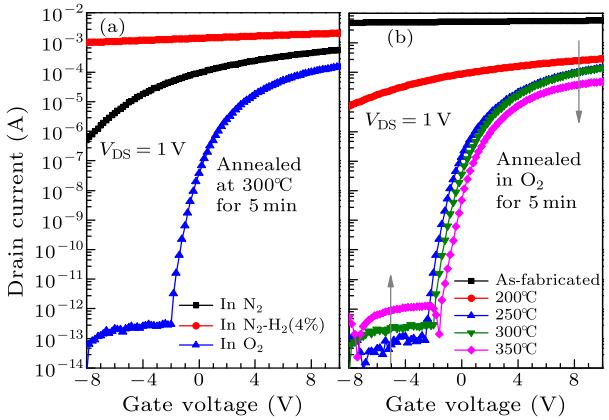

Fig. 2. Transfer characteristics of the ZnO TFTs: (a) annealed at 300℃ for 5 min in N_2, N_2-H_2(4%), and O_2, respectively, (b) annealed at different temperatures for 5 min in O_2.

Figure 1 shows the schematic structure and top view of the fabricated TFT device. It is indicated that the Mo electrodes and the ZnO channel overlap, thus ensuring sufficient contact between the source/drain electrode and the channel. To find out the effect of annealing environment on the electrical characteristics of the TFTs, the fabricated devices were first annealed in N_2, N_2-H_2(4%) and O_2, respectively, at 300℃ for 5 min. As shown in Fig. 2(a), the annealing in O_2 can result in the best transfer characteristics of the device compared with the annealing in N_2 or N_2-H_2(4%). Therefore, the influence of annealing temperature on the transfer characteristics of the ZnO TFTs was further studied in the environment of O_2 under a constant annealing time of 5 min, as shown in Fig. 2(b). It is found that the device does not exhibit a normal I_d–V_g characteristic of the TFT until the annealing temperature increases to 250℃. This can be understood as follows: O_2 annealing at higher temperatures can effectively passivate oxygen vacancies supplying free electrons in the ZnO channel,[11] hence reducing the carrier concentration in the ZnO film.[3] Further, as the annealing temperature rises from 250 to 350℃, the off-current of the device increases by around one order of magnitude, and the on-current also decreases evidently. As Janotti *et al.* reported, Zn atoms in ZnO could diffuse into Al_2O_3 at higher annealing temperatures of ≥300℃,[12] thus resulting in the formation of a Zn-doped alumina (ZAO) layer at the Al_2O_3/ZnO interface. However, the ZAO layer contains numerous charge trapping centers,[13] which likely provide extra leakage paths between source and drain, and enhance carriers trapping as well. This is also confirmed by the drop of effective mobility from 14.2 to 6.8 $cm^2/V{\cdot}s$ with increasing the annealing temperature from 250 to 350℃.

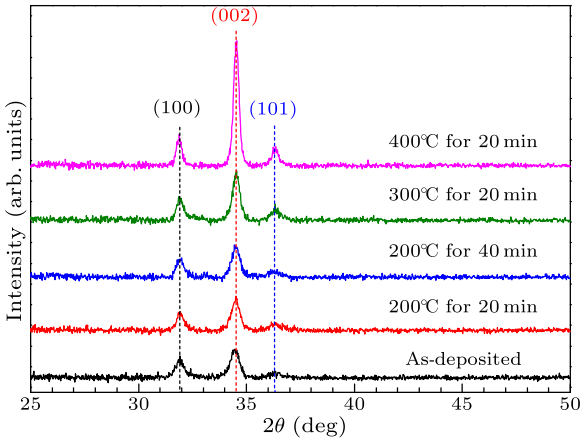

Fig. 3. XRD patterns of the as-deposited ZnO film (40 nm) and those annealed at different temperatures for different times.

Figure 3 shows the XRD patterns of the as-deposited ZnO film and those annealed under different conditions. All the ZnO films show a hexagonal wurtzite structure associated with the (100), (002), and (101) diffraction peaks. Based on the full width at half maximum (FWHM) of the preferential (002) peak, the average grain size was estimated by the Sherrer equation

$$D = \frac{0.9\lambda}{B\cos\theta},$$

where λ, B and θ denote the x-ray wavelength, the FWHM of the (002) peak, and the corresponding Bragg diffraction angle, respectively. Therefore, the mean grain size of the as-deposited ZnO film is 18.54 nm, and those for the films annealed at 200℃, 300℃ and 400℃ for 20 min are 20.51, 22.95 and 28.36 nm, respectively. This indicates that the annealing temperature has a significant influence on the crystallization of the ZnO film, which should be related to the annealing temperature-dependent performance of the device. However, for the annealing at 200℃, the crystallization of the ZnO film is slightly dependent on annealing time. For example, when the annealing

time increases from 20 to 40 min, the average grain size only increases by 0.45 nm.

Considering that the passivation of oxygen vacancies in ZnO could be related to annealing time in addition to the annealing temperature, we thus attempted to extend annealing time at 200℃. As shown in Fig. 4(a), when the cumulative annealing time increases to 10 min, the electrical performance of the ZnO TFT is improved significantly in comparison with 5 min annealing time. Further, as the cumulative annealing time increases gradually from 15 min to 40 min, the $I_{\rm d}$–$V_{\rm g}$ curves exhibit a small change, and the corresponding electrical parameters are listed in Table 1. In terms of sub-threshold swing S, annealing for 35 min causes a minimum S of 245 mV/dec while maintaining other superior characteristics, i.e., $\mu_{\rm ef} = 22.1\,{\rm cm}^2/{\rm Vs}$, $I_{\rm on}/I_{\rm off} = 7.6 \times 10^8$, and maximum $I_{\rm off} = 2.3 \times 10^{-13}$ A. From S, the maximum density of interface states at the ZnO/Al_2O_3 interface can be deduced as $D_{\rm it} = [\frac{S \log e}{kT/q} - 1]$, where q, k, and T are the unit electron charge, Boltzmann's constant, and absolute temperature, respectively. Based on the extracted S value and the unit area capacitance of the Al_2O_3 layer, $D_{\rm it}$ of the device annealed at 200℃ for 35 min is calculated to be $2.98\times10^{12}\,{\rm eV}^{-1}{\rm cm}^{-2}$, and $D_{\rm it}$ for the device annealed at 200℃ for 10 min is $7.25\times10^{12}\,{\rm eV}^{-1}{\rm cm}^{-2}$. This indicates that increasing annealing time at 200℃ can reduce the interface states, which is mainly ascribed to effective passivation of oxygen vacancies at the interface of ZnO/Al_2O_3,[14] rather than the change of crystallization in the ZnO channel. For comparison, Fig. 4(b) shows the transfer characteristics of the ZnO TFT as a function of the annealing time at a higher temperature of 300℃. Different from the annealing at 200℃, 5 min annealing at 300℃ can result in good performance of the device. As the annealing time increases up to 20 min or above, the $I_{\rm d}$–$V_{\rm g}$ curve does not exhibit evident variation. This indicates that the annealing at a higher temperature can rapidly passivate oxygen vacancies in the ZnO channel. Table 2 compares the electrical parameters of our device annealed at 200℃ and others. It is found that our device demonstrates much better electrical characteristics than others, even compared with those annealed at higher temperatures.

Table 1. Major electrical parameters of the ZnO TFTs annealed at 200℃ for different times in O_2.

Annealing time (min)	Max $I_{\rm off}$ (A)	$\mu_{\rm ef}$ ($\rm cm^2/V{\cdot}s$)	$I_{\rm on}/I_{\rm off}$	$V_{\rm th}$ (V)	S (mV/dec)
10	9.3×10^{-14}	23.9	1.6×10^9	2.48	510
15	1.3×10^{-13}	19.5	1.8×10^9	3.73	410
20	1.4×10^{-13}	19.6	1.01×10^9	4.51	360
25	1.7×10^{-13}	20.7	1.03×10^9	4.64	354
30	1.9×10^{-13}	20.5	7.8×10^8	4.25	347
35	2.3×10^{-13}	22.1	7.6×10^8	4.89	245
40	3.0×10^{-13}	21.6	6.1×10^8	4.90	264

Table 2. Comparison of major electrical parameters between our device and other ZnO TFT devices.

$T_{\rm max}$(℃)	$I_{\rm on}/I_{\rm off}$	$\mu_{\rm ef}$ ($\rm cm^2/V{\cdot}s$)	$V_{\rm th}$ (V)	S (mV/dec)	
200	7.6×10^8	22.1	4.89	245	This work
90	2.43×10^6	0.13	13.1	1210	Ref. [7]
140	2.2×10^6	1.786	11.43	710	Ref. [8]
150	9.5×10^7	6.7	4.1	670	Ref. [6]
200	$\sim10^7$	6.3	−7.5	420	Ref. [5]
300	5×10^7	3.9		1350	Ref. [9]
400	$>10^7$	21.3	4.9	390	Ref. [2]

It is known that the amount of time that a typical TFT spends under NGBS is approximately 500 times that spent under a positive gate bias in the active matrix liquid crystal display applications.[15] Therefore, NGBS is more important than positive gate bias stress. To compare the electrical instabilities of the ZnO TFTs annealed under different conditions, the devices were subjected to a negative gate bias stress (i.e., $V_{\rm G} = -10$ V and $V_{\rm DS}$ grounded) for different times at room temperature. Figure 5 shows the dependences of threshold voltage shift ($\Delta V_{\rm th}$) and sub-threshold swing variation (ΔS) of the TFTs on stress time under different annealing conditions. Regarding the devices annealed at 200℃ for 35 min, as the stress time increases from 500 to 2000 s, $\Delta V_{\rm th}$ shifts approximately from −0.01 to −0.11 V and ΔS increases from 0.04 to 0.07 V/dec. However, for the devices annealed at 300℃ for 5 min, $\Delta V_{\rm th}$ moves from −0.05 V to −0.17 V and ΔS rises from 0.04 to 0.12 V/dec. These results reveal that the annealing at 200℃ for 35 min can produce better stability under NGBS than that at 300℃ for 5 min. The shift of $V_{\rm th}$ toward negative bias under NGBS should result from accumulation of positive ionized oxygen vacancies at the ZnO/Al_2O_3 interface,[16,17] which is also accompanied by degradation of S. To sum up, long annealing at 200℃ is

equivalent to and even better than short annealing at 300℃.

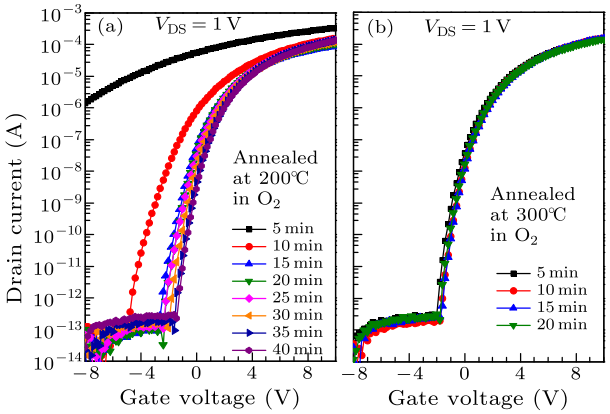

Fig. 4. Transfer characteristics of the ZnO TFTs as a function of cumulative annealing time: (a) at 200℃ in O_2, (b) at 300℃ in O_2.

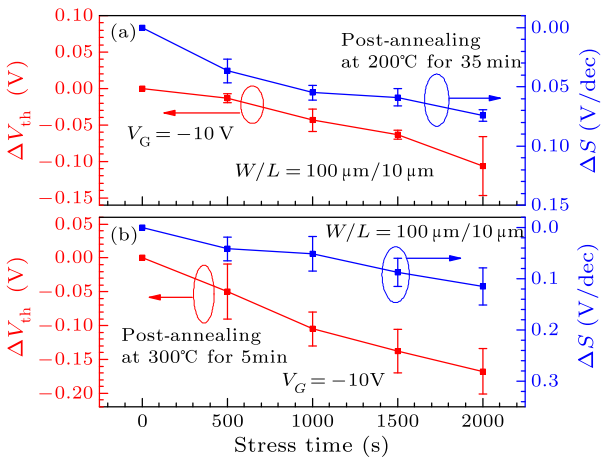

Fig. 5. Dependences of ΔV_{th} and ΔS on stress time under negative gate bias stressing ($V_G = -10$ V) for the devices: (a) annealed at 200℃ for 35 min, (b) annealed at 300℃ for 5 min.

In conclusion, the TFTs with ALD ZnO-channel/Al_2O_3-dielectric have been fabricated under the maximum thermal budget of 200℃. By post-annealing in O_2 at 200℃ for 35 min, excellent electrical characteristics are achieved, including a small sub-threshold swing of 245 mV/dec, a high on/off current ratio of 7.6×10^8, and a high electron effective mobility of 22.1 cm^2/V·s. In particular, superior electrical stabilities under NGBS are demonstrated in comparison with the device annealed at 300℃. The current ZnO TFT with high-performance and a low thermal budget is very promising for flexible electronic applications.

References

[1] Dimitrakopoulos C D and Malenfant P R L 2002 *Adv. Mater.* **14** 99
[2] Chen Y N, Xu Z, Zhao S L et al 2013 *Chin. Phys. Lett.* **30** 037302
[3] Geng Y, Yang W, Lu H L et al 2014 *IEEE Electron Device Lett.* **35** 1266
[4] Levy D H, Freeman D, Nelson S F et al 2008 *Appl. Phys. Lett.* **92** 192101
[5] Oh B Y, Kim Y H, Lee H J et al 2011 *Semicond. Sci. Technol.* **26** 85007
[6] Ahn C H, Yun M G, Lee S Y et al 2014 *IEEE Trans. Electron Devices* **61** 73
[7] Lim S J, Kwon S J, Kim Het al 2007 *Appl. Phys. Lett.* **91** 183517
[8] Kwon S, Bang S, Lee S et al 2009 *Semicond. Sci. Technol.* **24** 035015
[9] Bang S, Lee S, Park J et al 2009 *J. Phys. D: Appl. Phys.* **42** 235102
[10] Yang J, Park J K, Kim S et al 2012 *Phys. Status Solidi* A **209** 2087
[11] Zhang J, Liu Y, Wei Z Y et al 2013 *Appl. Surf. Sci.* **265** 363
[12] Janotti A, Van de Walle C G 2009 *Rep. Prog. Phys.* **72** 126501
[13] Chen S, Cui X M, Ding S J et al 2013 *IEEE Electron Device Lett.* **34** 1008
[14] Huang X M, Wu C F, Lu h et al 2015 *Chin. Phys. Lett.* **32** 077303
[15] Lee K H, Jung J S, Son K S et al 2009 *Appl. Phys. Lett.* **95** 232106
[16] Kim Y, Kim S, Kim W et al 2012 *IEEE Trans. Electron Devices* **59** 2699
[17] Pan T M, Chen C H, Her J L et al 2014 *J. Appl. Phys.* **116** 194510