Oxygen Scavenging Effect of $LaLuO_3$/TiN Gate Stack in High-Mobility Si/SiGe/SOI Quantum-Well Transistors *

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Higher-κ dielectric $LaLuO_3$, deposited by molecular beam deposition, with TiN as gate stack is integrated into high-mobility Si/SiGe/SOI quantum-well p-type metal-oxide-semiconductor field effect transistors. Threshold voltage shift and capacitance equivalent thickness shrink are observed, resulting from oxygen scavenging effect in $LaLuO_3$ with Ti-rich TiN after high temperature annealing. The mechanism of oxygen scavenging and its potential for resistive memory applications are analyzed and discussed.

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As the complementary metal-oxide-semiconductor technology node continues to scale down, a new gate dielectric with high dielectric constant is required to replace SiO_2.[1,2] Regarding the gate dielectric nowadays, hafnium oxide (HfO_2, $\kappa \sim 20$) is the most well-known high-κ gate dielectric and has already been adopted in advanced device processing. However, higher-κ (>20) dielectrics are still required for further scaling down to sub-20 nm technology nodes. Lanthanum lutetium oxide ($LaLuO_3$) with a dielectric constant of $\kappa = 32$ is a viable gate dielectric solution presenting large band gap, band off-sets to Si and SiGe, and high thermal stability. $LaLuO_3$ has a large optical band gap of 5.2 eV and band off-sets to Si of 2.1 eV, and maintains its amorphous phase up to a temperature of 1000℃.[3] On account of these advantages of $LaLuO_3$, it has been integrated into transistors.[4–7] However, the unique effects of $LaLuO_3$ as gate dielectric have not been thoroughly investigated.

In this Letter, we integrate $LaLuO_3$/TiN gate stack into high-mobility Si/SiGe/strained-SOI quantum-well p-type metal-oxide-semiconductor field effect transistors (MOSFETs). With Ti-rich TiN, oxygen scavenging is induced in $LaLuO_3$ after high temperature annealing. Its effects on capacitance equivalent thickness (CET), flat-band voltage (V_{fb}) shift, mobility and its potential for resistive memory application are analyzed and discussed.

In experiment, p-MOSFETs were fabricated on $Si/Si_{0.5}Ge_{0.5}$/strained-SOI heterostructure substrates. The SiGe channel is supposed to enhance hole mobility[4–14] and a Si layer is capped on SiGe to maintain the process compatible with Si.[7,15] A gate first process was adopted. RCA cleaning was carried out before high-κ deposition, with SC2 solution cleaning as the last step which leads to a SiO_2 layer remaining on the surface. The 10 nm $LaLuO_3$ was deposited by molecular beam deposition (MBD) followed by 40 nm TiN as gate metal by sputter deposition. The gate stack was exposed to 650℃ for 1 min during the source and drain activation. Transistors with HfO_2/TiN gate stack were also fabricated by the same processes, except that HfO_2 was deposited by atomic layer deposition (ALD) and TiN by atomic vapor deposition (AVD).

The transfer and output characteristics of a p-MOSFET with the gate length of $L = 5\,\mu$m are shown in Fig. 1. The device features a sub-threshold slope of 92 mV/dec. The device presents a good I_{on}/I_{off} ratio of about 10^6 and the output characteristics show a good current saturation. A large threshold voltage V_{th} of −1.5 V was measured.

The split C–V characteristics, measured at a frequency of 1 MHz, are shown in Fig. 2, indicating a CET value of 1.73 nm. The split C–V is also measured at a frequency of 100 kHz, which shows no significant difference and is not plotted. This CET value is lower than the theoretical expectation. Figure 2 also shows the C–V curve of the transistor with 5 nm HfO_2 gate dielectric. Theoretically, the CET of the $LaLuO_3$ transistor should be higher than the HfO_2 one, as the $LaLuO_3$ layer has a higher ratio of thickness to the κ value. However, Fig. 2 shows that the CET of the HfO_2 transistor is ∼1 nm higher than the $LaLuO_3$ transistor. Moreover, a V_{fb} shift is observed for the $LaLuO_3$ transistor, corresponding to the V_{th} shift.

To explain the lower-than-normal CET, we made a cross-sectional TEM image of the gate stack, shown in Fig. 3. It can be seen that there are many vague holes in the upper half of the $LaLuO_3$ layer, forming

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an interfacial layer between $LaLuO_3$ and TiN. In comparison, there is no interfacial layer in HfO_2/TiN stack after the same annealing process, as shown in Fig. 4. It is worth noting that the TiN deposition processes in $LaLuO_3$/TiN and HfO_2/TiN are different. Since our sputtering recipe was reported to deposit Ti-rich TiN,[16] the formation of this interfacial layer is probably due to significant oxygen scavenging induced by rich Ti near the $LaLuO_3$/TiN interface during high temperature annealing,[17] which generates oxygen vacancies in the $LaLuO_3$ layer. It is speculated that the interfacial layer is metal-like and its electrical properties are quite different from $LaLuO_3$. As a result, the formation of the interfacial layer leads to reduction of the effective thickness of $LaLuO_3$. The lower-than-expected CET is clear evidence of the thickness reduction of $LaLuO_3$. In addition, the existence of the interfacial layer affects the metal work function in the $LaLuO_3$/TiN stack. The work function is close to the one of the metal-like interfacial layer rather than TiN. The V_{th} shift and V_{fb} shift of the transistor are clear evidence of the work function shift.

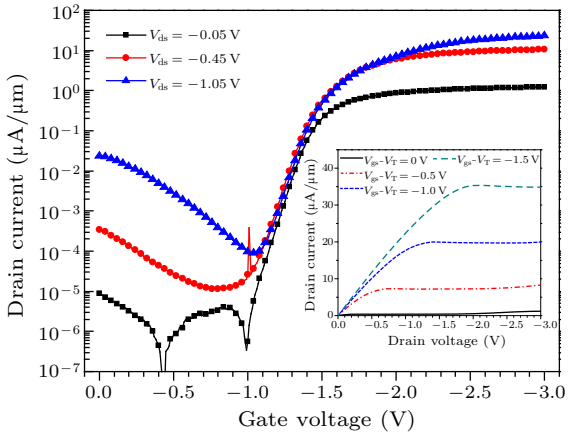

Fig. 1. The I–V characteristics of a p-MOSFET with $LaLuO_3$/TiN gate stack. The gate length is 5 μm.

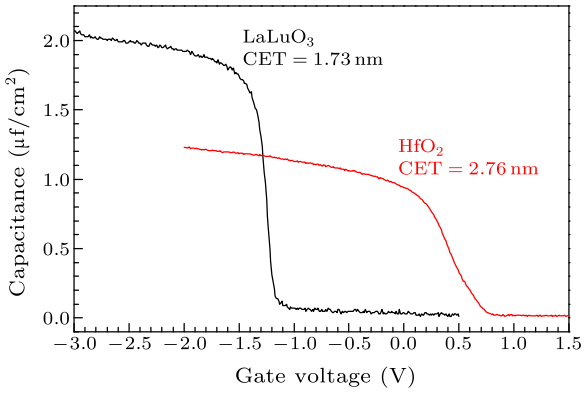

Fig. 2. Split C–V characteristics of p-MOSFETs with $LaLuO_3$/TiN and HfO_2/TiN gate stacks.

The effective hole mobility of $Si/Si_{0.5}Ge_{0.5}$/SOI QW p-MOSFETs is extracted by a split C–V method, as shown in Fig. 5. A long-channel ($L_g = 1$ μm) device was used for a more precise result. The hole mobility is about 200 $cm^2/V{\cdot}s$ under the strong inversion condition, twice as high as the Si universal hole mobility. High hole mobility is attributed to the intrinsic high mobility of compressively strained SiGe, effective hole confinement in the QW channel and low high-κ related scattering due to the Si cap screening.[7] Compared with the mobility of the HfO_2/TiN gate stack transistor, the $LaLuO_3$/TiN gate stack transistor does not suffer from any mobility degradation due to the oxygen scavenging effect. It is indicated that the oxygen vacancies and interfacial layer do not induce severe carrier scattering in spite of CET reduction and flat-band voltage shift.

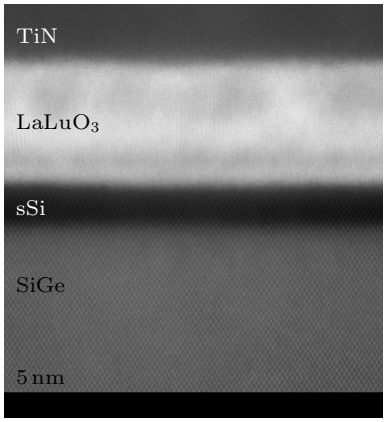

Fig. 3. TEM image of $LaLuO_3$/TiN (by sputtering deposition) gate stack after annealing at 650℃.

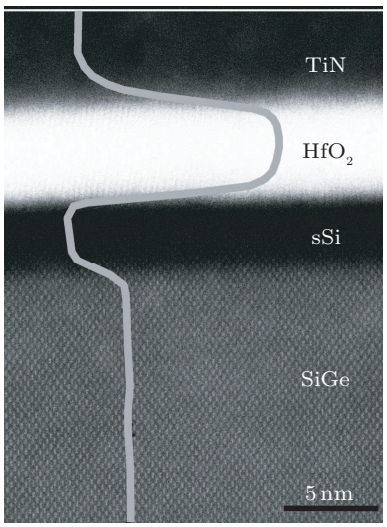

Fig. 4. TEM image of HfO_2/TiN (by AVD) gate stack after annealing at 650℃.

Generally the oxygen vacancies could act as charge traps, thus we presume that the $LaLuO_3$ layer after oxygen scavenging could have resistive memory effect. A test structure, shown in the inset of Fig. 6, was made to testify the resistive properties of $LaLuO_3$. TiN is also Ti-rich and the device was annealed by

the same process as activation annealing for quantum-well transistors. The resistive properties under forward and reverse sweeping are illustrated in Fig. 6. The resistance is relatively high when voltage sweeps from 0 when the oxygen vacancies are unoccupied. After the voltage reaches −3 V, the current goes up abruptly as more and more vacancies were electrically charged. The reverse sweeping curve shows lower resistance compared with forward sweeping due to the fact that most vacancies are charged. The result verifies that the $LaLuO_3$ layer with oxygen vacancies has resistive memory effect and its resistance depends on whether the oxygen vacancies are charged or not. This property could be potentially used for novel resistive memories.

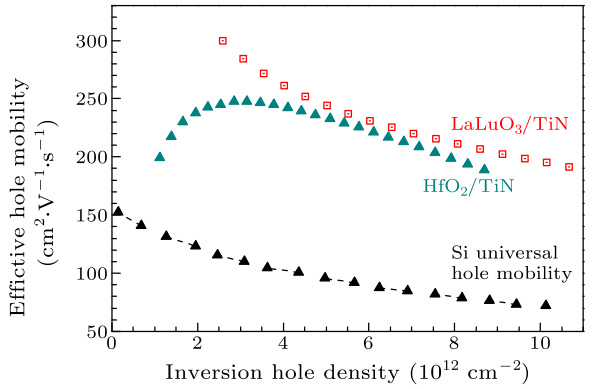

Fig. 5. The effective hole mobility of $Si/Si_{0.5}Ge_{0.5}/SOI$ QW p-MOSFETs with $LaLuO_3$/TiN and HfO_2/TiN gate stacks.

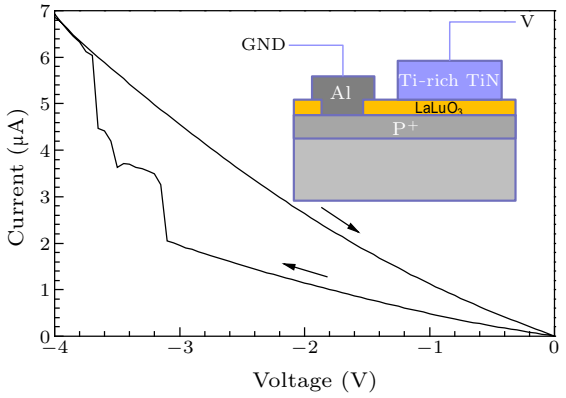

Fig. 6. Resistive properties of the test device under forward and reverse sweeping. The inset shows the structure of the test device.

In summary, $LaLuO_3$/TiN gate stack, with $LaLuO_3$ by MBD and TiN by sputtering deposition, has been integrated into high mobility Si/SiGe/SOI quantum-well p-MOSFETs, exhibiting good I–V characteristics. A flat-band voltage shift and a lower than normal CET are measured, due to an interfacial layer between $LaLuO_3$ and TiN induced by oxygen scavenging of Ti-rich TiN during high temperature annealing. The mobility is not affected by this interfacial layer as the carrier scattering is not intensified. The $LaLuO_3$ layer with oxygen vacancies shows different resistive properties before and after electrically charging, which brings a potential for resistive memory applications.

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