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Programmable Logic Based on Large Magnetoresistance of Germanium *

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We find extremely large low-magnetic-field magnetoresistance (∼350% at 0.2 T and ∼180% at 0.1 T) in germanium at room temperature and the magnetoresistance is highly sensitive to the surface roughness. This unique magnetoelectric property is applied to fabricate logic architecture which could perform basic Boolean logic including AND, OR, NOR and NAND. Our logic device may pave the way for a high performance microprocessor and may make the germanium family more advanced.

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The development of complementary metal oxide semiconductor (CMOS) transistor-based integrated circuits has achieved great success for the modern microprocessor.[1−3] However, the CMOS logic gate shows weak output driving capability and, moreover, their architecture is rigid for the present hardware systems.[1] Additionally, to meet the growing needs of the computational power, the CMOS circuit miniaturization is approaching its fundamental scaling limitations.[4] Therefore, new material systems are required to overcome size barriers for future logic applications.

Nowadays, a number of magnetoresistive devices, mainly including spin-based devices and magnetic-field-based devices, have been proposed to develop magnetic logic circuits.[4,5] They show distinct advantages in computational efficiency and offer interesting possibilities for programmable logic.[5−7] Spin-based logic devices at present are based on the giant magnetoresistance (GMR) effect in metals, while the effect is too weak for logic operations.[7] Recently, extremely large magnetoresistance (MR) has been found in some non-magnetic semiconductors, such as InSb,[5,8] Ag_2Se,[9] and Si.[10−12] These discoveries indicate that semiconductors are potentially superior alternatives to realize logic operations. Among the non-magnetic materials, germanium (Ge) is the first semiconductor for demonstrating the key properties of transistors.[13] Unfortunately, its oxide is chemically unstable in contrast to SiO_2, which hinders its applications.[13] One important way to improve transistor performance is to increase its channel mobility.[14] Motivated by this, Ge enjoys a certain 'comeback' as a promising candidate for the silicon-based microelectronics.[13−17] In recent years, many research works have focused on optical applications of Ge,[18] while the use for logic gate operations has not been reported before. Here we show that large MR has been observed in Ge and the MR is highly sensitive to the surface roughness. Based on these unique magnetoelectric properties, we design simple circuits to realize Boolean logic functions including AND, OR, NOR and NAND.

In this work, three different kinds of Ge wafers (purchased from Shanghai Daheng Optics and Fine Mechanics Co., Ltd.), i.e., one-side polished, double-side polished and double-side unpolished wafers, were used. All the Ge wafers were lightly Sb-doped, which has the thickness d of 500 μm and room-temperature mobility of 2700 $cm^2v^{-1}s^{-1}$. The two-terminal In/Ge/In (In, indium) devices were fabricated by pressing pure In as the electrode on the Ge surface. Figure 1(a) shows the structure diagram of one In/Ge/In device, which has the width (w) of ∼4.5 mm and length (l) of 4 mm. Note that the Ge used in Fig. 1 was cut from one-side polished wafer. The current–voltage (I–V) characteristics of the devices were measured with a Keithley 2400 current source/voltmeter. Additionally, a digital magnetic field generation system was used to provide external magnetic fields (B), and the field was oriented parallel to the sample plane and perpendicular to the current flow (Fig. 1(a)). In addition, all the experiments were conducted at room temperature.

The insets of Figs. 1(c) and 1(d) schematically show the cross sections of two different In/Ge/In devices D_1 and D_2. The difference between them is the electrode placement, i.e., the electrode was made on the polished surface (S_2) of D_1 and on the unpolished surface (S_1) of D_2, respectively. As shown in Fig. 1(b), the I–V characteristics of D_1 obey Ohms' law at low voltage ($V < 6$ V) and satisfy the Mott–Gurney law at high voltage ($7 < V < 13$ V) owing to the space-charge effect. In the latter regime, insufficient charge is present to compensate for the injected electrons, and the quasi-neutrality is broken. This causes a strong in-

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homogeneity in both the carrier concentration and the electric field, similar to the situation existing in other semiconductors in which a strong positive MR was observed.[9,11] When the electric field generated by the accumulated space charge and the applied voltage exceed the threshold that Ge can sustain, it will certainly lead to breakdown in some sufficient field region.[17] Here the threshold voltage $V_{\rm th}$ is defined as the bias at which the measured current reaches ∼50 mA. For the positive magnetic field (0–0.5 T), $V_{\rm th}$ increases with the increasing magnetic field, which indicates a significant MR effect (Fig. 1(c)). We define the MR ratio as $MR = [R(B)/R(B = 0) - 1] \times 100\%$, where $R(B)$ is the two-terminal resistance under the applied magnetic field. Hence the corresponding MR at $V_{\rm bias} = 15.5$ V can reach ∼350% at 0.2 T and ∼180% at 0.1 T, which is larger than that of previously reported semiconductors.[10–12] For the negative magnetic field (−0.1, −0.2 and −0.3 T), though I–V also shows a sharp increase of current above $V_{\rm th}$, the magnetic field dependence of I–V is almost not observed (Fig. 1(c)). Remarkably, the current at $V_{\rm bias} = 15.8$ V varies from ∼80 mA to ∼12 mA, i.e., by a factor of 7, as B changes from −0.2 T to 0.2 T. This voltage-controlled extremely large low-magnetic-field magnetoconductance could offer reliable logic outputs of high signal-to-noise ratio in Ge-based logic circuitry. Figure 1(d) displays the I–V characteristics of D_2 under various magnetic fields. Interestingly, D_2 shows a rather similar I–V behavior as D_1 under reversed magnetic field.

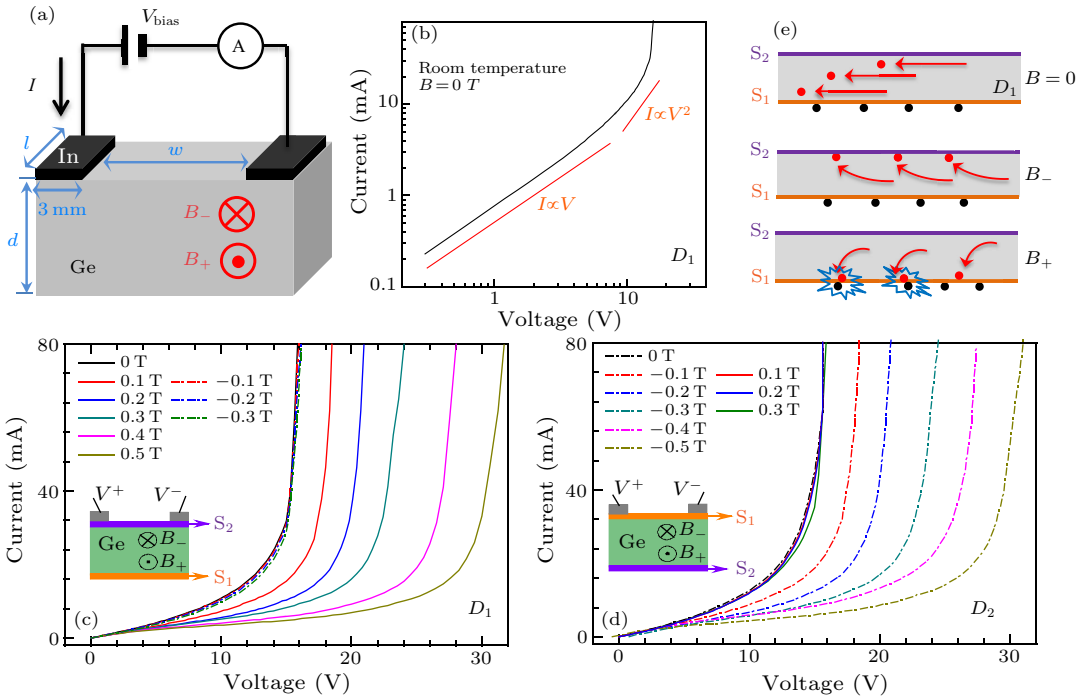


Fig. 1. (a) Schematic illustration of the In/Ge/In device structure and measurement setup. (b) The $\log I$–$\log V$ characteristic of D_1 at 0 T. The I–V characteristics of D_1 (c) and D_2 (d) for various magnetic fields. The inset shows the schematic cross section of D_1 and D_2, respectively. (e) Schematic illustration of carrier recombination process at S_1 and S_2.

Since the magnetic field B is applied parallel to the sample plane and perpendicular to the current, the different surface roughness might account for the asymmetric MR. When positive field B_+ (negative field B_-) is applied to D_1, the carriers are deflected to S_1 (S_2) due to the Lorentz force (Fig. 1(e)). It has been reported that the surface roughness can act like carrier traps, which dominates the carrier recombination process.[19–21] As the unpolished surface S_1 is much rougher than the polished surface S_2, the charge carriers near S_1 have a greater tendency to recombine than those near S_2. Accordingly, the carrier concentration of D_1 is reduced (increased) under B_+ (B_-), leading to a diminished (enhanced) current. Similarly, the current of D_2 is enhanced (diminished) under B_+ (B_-). Recently, asymmetric MR has also been observed by Yang *et al.*[22] in silicon p–n junctions. They ascribe it to the current deflection, which induces an additional Hall voltage at the boundary. In our case, however, the symmetric MR is observed in the sample with identical surfaces under positive and negative magnetic fields. This indicates that the asymmetric MR in our device is mainly dominated by the different surface recombination rates.

To further study the effect of surface roughness on the MR, we fabricated another four samples D_3, D_4, D_5, and D_6. It is worth mentioning that D_3 (D_4) was fabricated from double-side polished (unpolished) germanium wafer, thus its surfaces correspond to S_2 (S_1). Also note that D_5 (D_6) was fabricated from D_1 (D_4)

by polishing its rough side (S_1), and this process creates a new surface, S_3. Moreover, samples D_1–D_6 are of the same size.

The remarkable I–V characteristics of the four devices D_3–D_6, with threshold voltages of V_{th}^{S1}, V_{th}^{S2} and V_{th}^{S3} are given in Fig. 2(a). For $B = -0.2$ T, the electrons of D_3 and D_5 (D_4 and D_6) are deflected to S_2 (S_1), leading to a relatively slow (fast) recombination rate. Accordingly, a low (high) threshold voltage, i.e., V_{th}^{S2} (V_{th}^{S1}), is observed (Fig. 2(a)). On the other hand, when a field of $+0.2$ T is applied, the electrons of D_5 and D_6 are deflected to S_3, leading to a different threshold voltage, V_{th}^{S3} (Fig. 2(a)). Thus from the above discussion it follows that V_{th} changes with the surface conditions. The surface morphologies of S_1, S_2, and S_3 were examined by scanning electron microscopy (SEM), as displayed in Fig. 2(b). It shows that S_2 is the smoothest one, while S_3 is less smooth with some unevenness. However, compared with S_2 and S_3, S_1 is rather rough and covered with cracks. The three-dimensional profiles of S_1, S_2 and S_3 are observed by a Talysurf 5P-120 surface profile measurement instrument and the average roughnesses of them (r^{S1}, r^{S2}, r^{S3}) are measured to be 603 nm, 7.8 nm and 273 nm, respectively. Based on the relationship $V_{th}^{S2} < V_{th}^{S3} < V_{th}^{S1}$ and $r^{S2} < r^{S3} < r^{S1}$, one can draw a conclusion that V_{th} increases with the increasing surface roughness. Thus the MR enhancement in our device results in part from the presence of surface roughness.

Further, programmable Boolean logic is realized based on the unique magnetoelectric property of our device. We designed a simple circuit containing four devices (D_1, D_2, D_1' and D_2') shown in Fig. 3(a). D_1 and D_1' (D_2 and D_2') are two identical samples, thus their magneto-electric properties are quite similar. Recalling the abrupt change of current in D_1 and D_2 (see Figs. 1(c) and 1(d)), we define the currents below 35 mA (above 65 mA) as logic output '0' ('1'). Also, the positive and negative fields ($B_+ = 0.2$ T and $B_- = -0.2$ T) serves as the logic inputs 0 and 1, respectively. In addition, each device was fixed on a separated sample holder and the sample holder can be rotated manually. This ensures that the field direction at each device can be independently controlled.

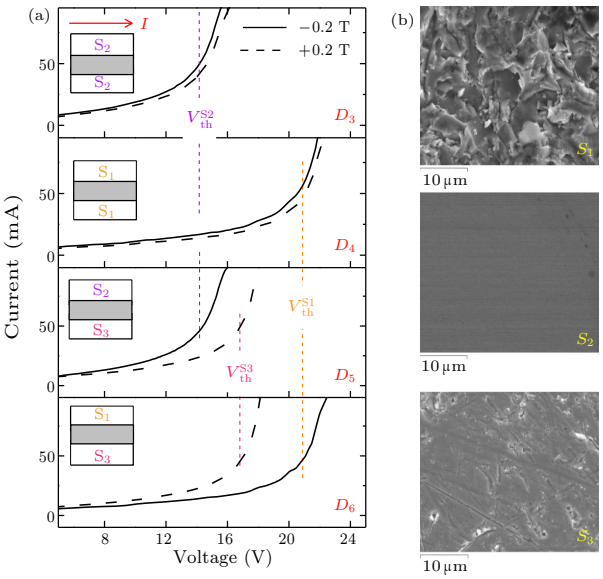
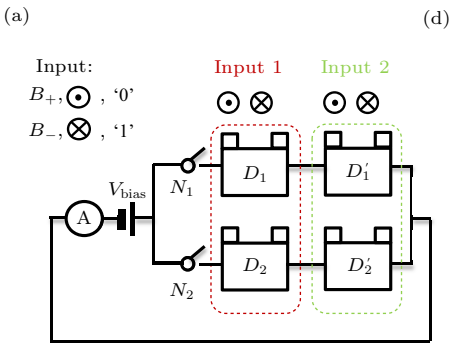


Fig. 2. (a) The I–V characteristics of D_3, D_4, D_5, and D_6 for $B = \pm 0.2$ T. The inset shows the diagram of cross-sections of D_3, D_4, D_5 and D_6 (top to bottom). (b) The SEM images of S_1, S_2 and S_3.



(d)

Logic input		Logic output (current)			
		N_1 : ON & N_2 : OFF		N_1 : OFF & N_2 : ON	
input 1	input 2	$V_{bias} = 33.4$ V	$V_{bias} = 38.3$ V	$V_{bias} = 32.7$ V	$V_{bias} = 37.8$ V
0	0	0 (21 mA)	0 (33 mA)	1 (69 mA)	1(84 mA)
0	1	0 (24 mA)	1 (73 mA)	0 (28 mA)	1(72 mA)
1	0	0 (26 mA)	1 (72 mA)	0 (27 mA)	1(74 mA)
1	1	1 (76 mA)	1 (87 mA)	0 (23 mA)	0(35 mA)
		AND	OR	NOR	NAND

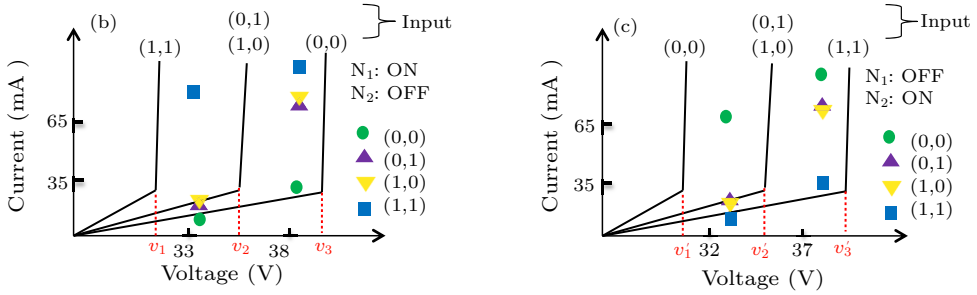


Fig. 3. (a) Schematics of the designed logic device. Schematic diagram of I–V characteristics for (b) N_1: ON & N_2: OFF and (c) N_1: OFF & N_2: ON; the scattered data are obtained experimentally for the logic input $(0,0)$ (●), $(0,1)$ (▲), $(1,0)$ (▼), and $(1,1)$ (■). (d)Truth table of the AND, OR, NOR and NAND logic operations.

For the AND, OR, NOR and NAND logic operations, each of them needs two logic inputs; thus the magnetic fields applied on D_1 and D_2 are regarded as input 1, while the fields applied on D_1' and D_2' are regarded as input 2 (Fig. 3(a)). When the switch N_1 is ON (N_1: ON) and switch N_2 is OFF (N_2: OFF), the output of the logic device will be determined by D_1 and D_1'. There are three cases which will be considered separately, (i) the input is $(1,1)$, i.e., the two devices are under B_-, thus their electrons are deflected to S_2. This leads to an enhanced current flow and a small threshold voltage, v_1 (Fig. 3(b)). (ii) The input is $(0,0)$, i.e., the two devices are under B_+, thus their electrons are deflected to S_1. This leads to a decreased current flow and a high threshold voltage, v_3 (Fig. 3(b)). (iii) The inputs are $(0,1)$ and $(1,0)$, i.e., one of the devices is under B_+ and the other is under B_-, thus the electrons of one device are deflected to S_1 and the electrons of the other device are deflected to S_2. In this case the average recombination rate is slower than that in (ii), and faster than that in (i). Thus the threshold voltage (v_2) for case (iii) is between v_1 and v_3. Figure 3(b) shows the schematic I–V characteristics for different logic inputs, indicating that the Boolean logic can be programmed by the external bias. For example, at $V_{\rm bias} = 33.4$ V, the output current is 21 mA (0), 24 mA (0), 26 mA (0) and 76 mA (1) for input states $(0,0)$, $(0,1)$, $(1,0)$ and $(1,1)$, respectively. Thus the AND logic operation could be realized. Alternatively, at $V_{\rm bias} = 38.3$ V, the output current is 33 mA (0), 73 mA (1), 72 mA (1) and 87 mA (1) for input states $(0,0)$, $(0,1)$, $(1,0)$ and $(1,1)$, respectively. Thus the OR logic operation could be realized.

Compared with AND (OR) operation, NOR (NAND) logic operation has the same logic output and reversed logic input.[4] When the switch N_1 is OFF (N_1: OFF) and the switch N_2 is ON (N_2: ON), the output of the logic device will be determined by D_2 and D_2'. We have demonstrated in Fig. 1 that D_2 can be replaced by D_1 if the logic inputs, B_+ and B_-, are reversed. That is, reversal of field directions turns AND to NOR and OR to NAND. It can be seen in Fig. 3(c), as expected, that the output current at $V_{\rm bias} = 32.7$ V is 23 mA (0), 27 mA (0), 28 mA (0) and 69 mA (1) for the input states $(1,1)$, $(1,0)$, $(0,1)$ and $(0,0)$, respectively. This represents a NOR logic function. Alternatively, the output current at $V_{\rm bias} = 37.8$ V is 35 mA (0), 74 mA (1), 72 mA (1) and 84 mA (1) for the input states $(1,1)$, $(1,0)$, $(0,1)$ and $(0,0)$, respectively. This represents a NAND logic function. The truth table in Fig. 3(d) summarizes the operation of AND, OR, NOR and NAND Boolean logic functions, with each logic function controlled by the pre-setting bias voltages. Our results therefore demonstrate that Ge is a promising material for programmable logic applications at room temperature.

It has been reported by Karakushan *et al.*[23] that a magnetodiode shows the similar I–V behavior under positive and negative magnetic fields, which relies on the magneto-concentration effect and the bipolar injection. A traditional magnetodiode contains a long PIN structure in which the double injection current flows.[24] However, this kind of bipolar injection is totally different from our case where we have demonstrated that local impact ionization results in the bipolar injection (hole-electron). Thus our work may provide another approach for the study of the magnetodiode.

Recently, Joo *et al.*[5] found large MR in an InSb p–n bilayer channel and it offers reliable outputs for the magnetic-field-based logic. However, the electric field of the InSb device is homogeneous even at high voltage, thus it is required to generate sufficient energy for ionization, leading to the relatively high threshold electric field ($\sim 10^5$ V/cm).[5] We have reported in Ref. [17] that a strong inhomogeneous electric field is formed in our device owing to the space-charge effect and thus the electric fields of some local regions are very high, which contribute to the impact ionization at low average electric field ($\sim$50 V/cm). On the other hand, to induce a magnetic-field-direction-dependent MR, an asymmetry structure, a p–n bilayer channel should be formed in the InSb device. However, this is not an easy task to achieve such control. Most pn junction InSb devices were fabricated under high temperature and particular pressure, which would increase the production cost.[25] In our device, simple surface treatment (i.e., polishing the surface by using the abrasive paper) can make the structure asymmetric and thus induce an asymmetric MR. Consequently, our devices have the potential to provide basic logic operations at low power consumption and low cost.

We have realized logical operations using In/Ge/In devices with dimensions of the order of 4 mm. However, for practical applications, integrated devices at sub-micrometer scales are required.[5] Integration problems of our device can be tackled from two aspects: producing high-quality Ge and reducing its size. The recent advances in growth techniques, such as chemical vapor deposition, molecular beam epitaxy and ultra-high-vacuum chemical vapor deposition, have demonstrated the possibility of producing high-quality Ge on Si.[14,26] Also, the surface passivation of Ge has been achieved successfully in the latest years.[14] Therefore, our device may be easily integrated into silicon devices in the near future. On the other hand, since the Lorentz force depends on carrier mobility in semiconductors and high mobility can be kept at small scale,[5] the large magnetoresistive sensitivity of our devices should be scalable. If the length, width and thickness of our device are reduced to $\sim$100 nm, then the output current is expected to be as low as 1 nA (in the low-current state). Assuming that the maximum current is limited to five times larger than the low-current value, we can obtain a high-current output of 5 nA.

In conclusion, we have achieved extremely large

MR of ∼350% at 0.2 T and ∼180% at 0.1 T in Ge at room temperature. This MR is significantly asymmetric in the presence of magnetic fields with opposite signs, which is attributed to the different surface roughness. Based on these findings, programmable logic architecture is presented and the Boolean logic including AND, OR, NOR and NAND is realized. Our logic architecture has superior characteristics, such as ultra-low-threshold field and instant-on performance. This approach not only makes the Ge family more advanced but also has the potential to provide a paradigm shift from the transistor-based logic to the magnetic-field-based logic.

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