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A Single Mode Hybrid Ⅲ–Ⅴ/Silicon On-Chip Laser Based on Flip-Chip Bonding Technology for Optical Interconnection *

Hai-Ling Wang(王海玲)[1], Wan-Hua Zheng(郑婉华)[1,2]**

[1]*Laboratory of Solid State Optoelectronic Information Technology, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083*

[2]*State Key Laboratory on Integrated Optoelectronics, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083*

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A single mode hybrid Ⅲ–Ⅴ/silicon on-chip laser based on the flip-chip bonding technology for on-chip optical interconnection is demonstrated. A single mode Fabry–Pérot laser structure with micro-structures on an InP ridge waveguide is designed and fabricated on an InP/AlGaInAs multiple quantum well epitaxial layer structure wafer by using i-line lithography. Then, a silicon waveguide platform including a laser mounting stage is designed and fabricated on a silicon-on-insulator substrate. The single mode laser is flip-chip bonded on the laser mounting stage. The lasing light is butt-coupling to the silicon waveguide. The laser power output from a silicon waveguide is 1.3 mW, and the threshold is 37 mA at room temperature and continuous wave operation.

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Silicon photonics is now widely accepted as a key technology in next-generation communication systems and data interconnects.[1–3] For silicon photonics, one of the major obstacles is the absence of a compact and power-efficient silicon-based light source, due to the indirect band gap of silicon, especially single mode hybrid silicon lasers with very simple fabrication. As the key component, the light source has been attracting a great deal of attention, because it is difficult to generate light for silicon itself.

Recently, various strategies for the light source in silicon photonic circuits have been demonstrated.[4–13] For example, integrating direct-band Ⅲ–Ⅴ semiconductor materials on the silicon-on-insulator (SOI) substrate through a direct bonding technology,[8–13] and integrating the Ⅲ–Ⅴ laser diode (LD) on the SOI substrate by using the flip-chip bonding technology.[14–19] The flip-chip bonding and butt-coupling are amongst the best technologies to achieve the record device performance when the footprint is not a concern. The efficient flip-chip bonded hybrid lasers are the devices demonstrated by researchers from Fujitsu[14] and Arakawa.[15] The high precision flip-chip bonding technology with exceptionally low alignment error (∼0.1 μm) was a crucial factor in misalignment loss reduction. The highest reported wall plug efficiency (WPE) to date (9.5%) has been achieved in a hybrid laser by Kotura *et al.*[18] Kotura's design utilizes an external cavity reflective semiconductor optical amplifier (SOA), butt-coupled to a silicon waveguide Bragg mirror on an SOI chip. However, most of these devices have the complicated spot-size converter (SSC) to minimize coupling losses and to improve the coupling power and need expensive high resolution processing.

Generally, the stable single mode lasers are obtained by using distributed feedback (DFB),[20,21] or external cavity structures (ECLs),[22,23] while manufacturing of these structures require additional processing steps of epitaxial regrowth and electron beam lithography. To avoid the complex regrowth steps and expensive electron-beam lithography, a single-mode laser has been presented in theory and experiment, which depends on reflective defects (micro-structures or slot structures).[24,25] Using slots in a standard multimode Fabry–Pérot (FP) laser to sufficiently select a single mode. Fabricating the slot structures does not need high resolution processing, and only needs i-line lithography, dry etching into the ridge waveguide.

Here we propose a single mode hybrid Ⅲ–Ⅴ/silicon on-chip laser based on the flip-chip bonding technology. Firstly, a single mode laser with slots on the InP ridge waveguide is designed and fabricated on an InP/AlGaInAs multiple quantum well epitaxial layer structure. The slot structures are designed as the high order grating and the whole fabrication process is achieved by the standard 1:1 photolithography to reduce the cost. Then, a waveguide platform including a simple tapered silicon waveguide and a laser mounting stage is designed and fabricated on an SOI substrate. The single mode laser is flip-chip bonded on the laser mounting stage. Lastly, the lasing light is butt-coupled to the tapered silicon waveguide. The laser power output from the silicon waveguide is 1.3 mW, the threshold is 37 mA at room temperature and continuous wave operation, and the side-mode suppression ratio (SMSR) is 35.7 dB.

The schematic diagram of the proposed hybrid integrated light source is shown in Fig. 1(a), which is a hybrid integration structure consisting a single mode

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**Corresponding author. Email: whzheng@semi.ac.cn

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LD on a silicon waveguide platform. The silicon waveguide platform includes a silicon waveguide and a laser mounting stage. An edge emitting LD lasing wavelength of about 1.55 μm is flip-chip bonded on the mounting stage. The laser has the same epitaxial layer structure as the 1550 nm commercial epitaxial wafer, which consists of an AlGaInAs/InP MQWs active layer, a p-InP cladding layer, an n-cladding layer, and the emission peak around 1550 nm. The lasing light is butt-coupled into the silicon waveguide. We design a simple tapered silicon waveguide on SOI to couple the lasing light of the LD. All of the silicon waveguides designed in this study are based on a silicon-on-insulator (SOI) wafer with a 0.34 μm top silicon layer and a 2 μm buried silicon oxide layer. Figure 1(b) show the schematic diagram of the proposed single mode LD. The single longitudinal mode is obtained by the slot structures on the 4.5 μm-wide InP ridge waveguide. The slot structures are located in the middle of the InP waveguide surface. The two cleaved facets act as the feedback facets to form the laser cavity.

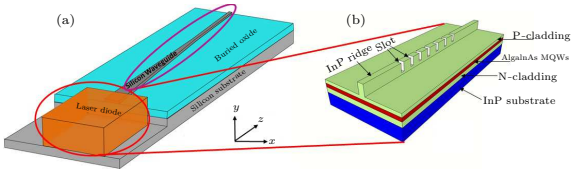

Fig. 1. (a) The schematic diagram of the hybrid integrated light source with a spot-size converter, in which the silicon waveguide is labeled by the purple circle, and the single mode laser diode is labeled by the red circle. (b) The schematic diagram of the single mode laser with the slot structures on the InP ridge waveguide.

To obtain the single longitudinal mode laser diode, we should design the optimum geometrical parameters of slots such as the slot period, slot width and slot etch depth. In fact, the proposed slot structure is based on Bragg's condition with high-order grating.[26] The slot period is defined as $2n_{\rm eff}\Lambda = q\lambda_{\rm B}$, where q is an integer representing the order of the grating, Λ is the period of the slot structure, $n_{\rm eff}$ is the effective index of the slot structure waveguide region, and $\lambda_{\rm B}$ is the Bragg wavelength. To determine the slot parameters, we use the FDTD method to simulate the effect of the slot period and the slot etch depth on the reflection of a group of slots. In the simulation, under the effective index approximation, the p-InP cladding layer of 1.85 μm and the AlGaInAs quantum well has an effective index of 3.18 and 3.52 in the 2D situation, respectively. Figures 2(a) and 2(b) show the contours of the simulated amplitude reflection of the slot structure versus the slot etch depth and the slot period fixed at 500 μm cavity length, 24 slot number, and 1.6 μm InP ridge waveguide height. We can see that a number of local maximum values of amplitude reflection at different wavelengths vary with the depth and period of slots. As the reflection amplitudes vary with wavelength, a single mode can be realized under special injection currents. From Fig. 2(a), we can see that amplitude reflection (labeled with the green circle) is about 35% at the wavelength 1.55 μm and 8.9 μm slot period, which is about the 37th order grating. This period has about a 37 nm free spectral range. From Fig. 2(b), we can see that the 1.1 μm slots etch depth (labeled with the black circle) leads to about 30% reflectivity amplitude in the 1545–1560 nm region. According to the simulating result, we determine the slot structure period and etch depth as 8.9 μm and 1.1 μm, respectively. Moreover, the duty cycle (slot width) of the slot structure period is another parameter we should consider. In this study, we are interested in the slot width around 1.1 μm that can be easily fabricated by standard photolithography.

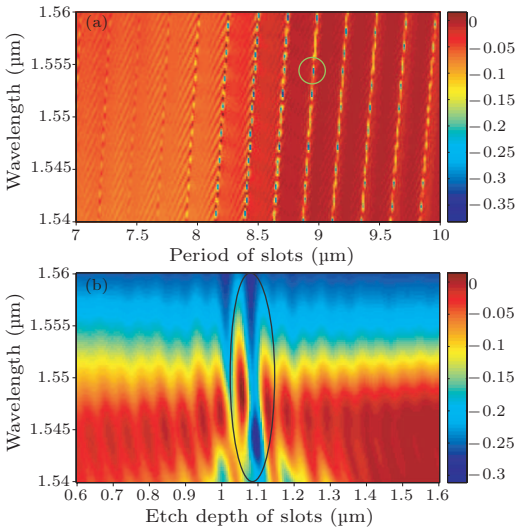

Fig. 2. Contours of the simulated amplitude reflection. (a) Wavelength versus slot period with a slot etch depth of 1.1 μm and a slot width of 1.1 μm. (b) Wavelength versus depth of slot structure with a period of 8.9 μm, a slot width of 1.1 μm and period number of 24.

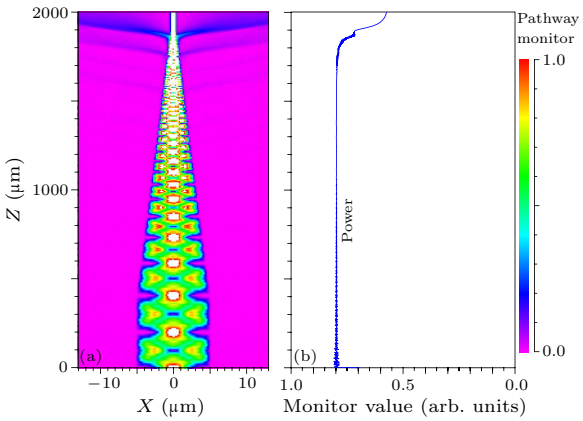

Fig. 3. The transmission map and the lasing light coupling efficiency of the proposed tapered silicon waveguide.

To keep the single mode transmission in the silicon waveguide (shown in Fig. 1(a)), we need to design the silicon waveguide parameters, including the silicon waveguide width, length and etch depth. The tapered silicon waveguide length was designed as 2000 μm, then

the silicon waveguide width was tapered from 10 μm to 450 nm. The BPM method was used to simulate the coupling efficiency of the silicon waveguide, as shown in Fig. 3. The butt coupling efficiency is more than 50%.

Figures 4(a) and 4(b) show the schematic diagram of the proposed tapered silicon waveguide output terminal and the TE mode pattern at the end of the silicon waveguide with the 0.45 μm tip width. Simulation was performed at 1550 nm by using the rigorous coupled-wave analysis method. From Fig. 4(b), a single guiding transverse electric (TE) mode in the silicon waveguide was obtained. The waveguide width at the output facet was therefore set to 450 nm in the fabrication process.

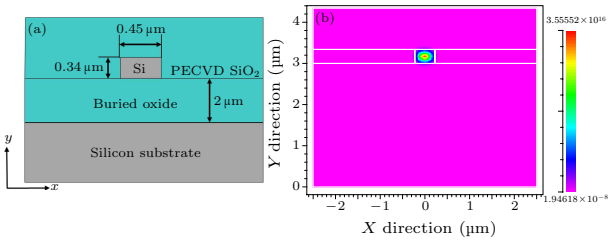

Fig. 4. (a) The schematic diagram of the proposed tapered silicon waveguide output terminal, and (b) the transverse electric mode pattern for the 0.45 μm tip width of the silicon waveguide.

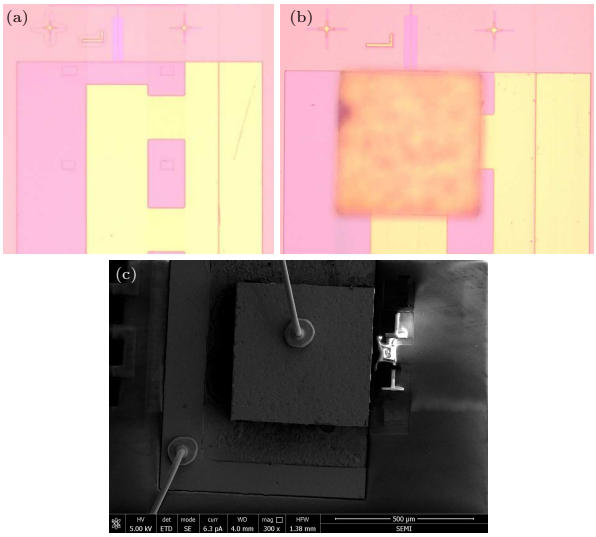

Fig. 5. The microscopy photographs and the scanning electron microscope (SEM) image of the silicon platform and the hybrid laser. (a) The microscopy of the silicon platform with a metal electrode, (b) the microscopy of the hybrid silicon laser, and (c) the SEM image of the hybrid silicon laser.

Firstly, the single mode laser is fabricated by using standard i-line lithography and inductively coupled plasma (ICP) reactive ion etching. Then, a silicon waveguide and a laser diode mounting stage is fabricated on the SOI substrate by using the electron beam lithography and ICP etching. On the LD mounting stage, there are four silicon pedestals. A layer of SiO_2 insulator is deposited on the silicon waveguide to passivation. Finally, the LD is flip-chip bonded on the LD mounting by using the flip-chip bonder. The vertical alignment accuracy of LD was precisely adjusted by the surface position of the etched silicon pedestals and the thickness of evaporation AuSn solder. The vertical alignment accuracy was made better than ±0.1 μm by dry etching and evaporation controllability. Figures 5(a) and 5(b) are the microscopy photography of the silicon waveguide platform and the hybrid silicon laser with an LD mounted on it. Figure 5(c) is the SEM image of the hybrid integrated light source. From Fig. 5(c), we can see that the gap between the LD and silicon waveguide input facet was about 1 μm and was not filled with AuSn.

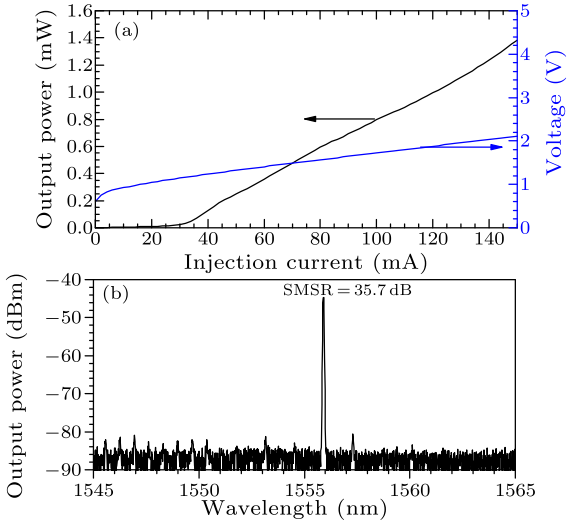

Fig. 6. (a) Measured P–I–V curve under the continuous current. (b) The spectrum at the current of 90 mA of the hybrid silicon laser.

The measured P–I–V curve and the optical spectrum of the fabricated hybrid laser are shown in Figs. 6(a) and 6(b). At room temperature, the laser has a threshold of 30 mA and a peak output power of 1.3 mW under 150 mA continuous wave operation, as shown in Fig. 6(a). At the current of 90 mA, the lasing wavelength is 1556 nm. Over 35 dB SMSR is realized at room temperature, as shown in Fig. 6(b). The measured power coupling efficiency is lower than the simulating results as shown in Fig. 3. Theoretically, there may be several factors that affect the coupling efficiency. Firstly, there is a different mode size in laser diode and the silicon waveguide leading to mode scattering and reflecting, and thus reducing the coupling efficiency. The other reasons may be that the reflectivity and scattering of the silicon waveguide input facet due to Fresnel reflection and the imperfect waveguide facet. It is possible to reduce the reflectivity by filling the gap between the LD facet and the silicon waveguide input facet with a material matched to the refractivity of the silicon waveguide input facet. The other method is making SSC on the silicon platform and using CMOS processing in the future.

In summary, we have proposed the design, fabri-

cation and measurement of a heterogeneously integrated Ⅲ–V-on-Silicon laser based on a single mode laser with the slot structure on InP ridge waveguide and the flip-chip bonding technology. A single mode hybrid Ⅲ–V/silicon laser, lasing at 1556 nm and with 1.3 mW on-chip output power, 35.7 dB SMSR, 30 mA threshold, is obtained.

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