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High-Mobility P-Type MOSFETs with Integrated Strained-$Si_{0.73}Ge_{0.27}$ Channels and High-κ/Metal Gates *

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Strained-$Si_{0.73}Ge_{0.27}$ channels are successfully integrated with high-κ/metal gates in p-type metal-oxide- semiconductor field effect transistors (pMOSFETs) using the replacement post-gate process. A silicon cap and oxide inter layers are inserted between $Si_{0.73}Ge_{0.27}$ and high-κ dielectric to improve the interface. The fabricated $Si_{0.73}Ge_{0.27}$ pMOSFETs with gate length of 30 nm exhibit good performance with high drive current (~428 μA/μm at $V_{DD} = 1$ V) and suppressed short-channel effects (DIBL~77 mV/V and SS~90 mV/decade). It is found that the enhancement of effective hole mobility is up to 200% in long-gate-length $Si_{0.73}Ge_{0.27}$-channel pMOSFETs compared with the corresponding silicon transistors. The improvement of device performance is reduced due to strain relaxation as the gate length decreases, while 26% increase of the drive current is still obtained for 30-nm-gate-length $Si_{0.73}Ge_{0.27}$ devices.

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$Si_{1-x}Ge_x$ is very promising as a channel material in future CMOS devices due to its good compatibility with silicon technology and high carrier mobility.[1–4] It is known that band structure of $Si_{1-x}Ge_x$ on silicon substrates is warped under compressive strain, and the hole effective mass can be reduced as a result.[5–7] Since high-k/metal gate (HKMG) has become essential technology for advanced CMOS process, the integration with HKMG is a prerequisite of $Si_{1-x}Ge_x$ application in large-scale integrated circuits.[8,9] Unfortunately, the poor interface between $Si_{1-x}Ge_x$ and dielectrics will partially cancel out the mobility enhancement due to effective mass reduction, or even degrade final mobility. The degradation of channel mobility associated with the interface quality of high-k dielectric and channel has always been one of the central issues in microelectronics.[10–14] Up to now, the most widely used high dielectric in mass production is HfO_2, and a thin oxide is usually introduced beneath HfO_2 to keep the high carrier mobility of the silicon channel.[15,16] Since $Si_{1-x}Ge_x$ cannot form good interface with those widely used dielectrics in industry, a thin silicon cap layer has to be deposited on top of $Si_{1-x}Ge_x$ to avoid its direct contact with gate stacks.[17–19] In addition, the process should be further addressed to obtain appropriate threshold voltage in the integration of $Si_{1-x}Ge_x$ with HKMG. Although much work was reported on high-mobility $Si_{1-x}Ge_x$ field-effect transistors, the investigation in this field has always been active.[20–22] The integration of $Si_{1-x}Ge_x$ with current advanced CMOS process and the examination of the device performance is still worthy of exploring.

In this work, $Si_{0.73}Ge_{0.27}$-channel p-type metal-oxide-semiconductor field effect transistors (pMOSFETs) were fabricated by a post-HKMG process. To achieve high hole mobility, $Si_{0.73}Ge_{0.27}$ was capped with a thin silicon layer. The highest effective mobility in the fabricated long-gate-length $Si_{0.73}Ge_{0.27}$ pMOSFET is up to 160 $cm^2V^{-1}s^{-1}$, and mobility enhancement is between 100% and 200% compared with silicon devices. Although the enhancement of device performance is reduced due to strain relaxation as gate length decreases, 26% increase of drive current is still gained for 30-nm-gate-length $Si_{0.73}Ge_{0.27}$ devices. In addition, the 30-nm-gate-length transistors show well suppressed short-channel effects and good electrical performance. The threshold voltage in the short-channel transistor is around −0.2 V, which is in the acceptable range for advanced pMOSFET applications.

All process modules of the investigated $Si_{0.73}Ge_{0.27}$ pMOSFETs with HKMG stacks were completed in our 8-inch CMOS platform. After n-well implantation and drive annealing, shallow trench isolation (STI) was realized by oxide fill and chemical mechanical polishing (CMP). The 16-nm-thick $Si_{0.73}Ge_{0.27}$ channel was then selectively grown at 650℃ by ultra-high vacuum chemical vapor deposition (UHVCVD). The germa-

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nium mole fraction was evaluated to be 0.27 by x-ray diffraction analysis, which was made on a separate test wafer. It should be noted that the $Si_{0.73}Ge_{0.27}$ channel is fully strained for 10-nm thickness. To improve the interface quality, an additional ultra-thin silicon cap (its initial thickness is about 4 nm) was grown on top of the selective $Si_{0.73}Ge_{0.27}$ layer at the same temperature. This silicon cap was partially consumed by later oxidation and cleaning process, and finally its thickness was about 2 nm or less. Next, the amorphous silicon gates of different lengths from tens of microns to 30 nm were patterned by mixing using conventional optical lithography and e-beam writing on the same wafers. Self-aligned source and drain regions were then formed by implantation, and the activation was implemented by spike anneals at 1050℃ for 5 s. After that, the dummy gates were exposed to air by CMP, and then removed by TMAH. Before the HKMG process, natural oxide was removed by buffered-oxide-etch (BOE), and the thin oxide interlayer was grown by ozone-treatment. Then HfO_2 was grown by atomic layer deposition, and undergoes a post annealing at 450℃ in ambient nitrogen. In the following, TiN/TaN/TiN/W stacks were deposited as metal gates, in which the 1-nm TiN/1-nm TaN layers were used to tune gate work function to achieve acceptable threshold voltage. Lastly, electrical connections to device terminals were completed. The final structure of a $Si_{0.73}Ge_{0.27}$ pMOSFET with 30-nm gate length is shown by transmission electron microscopy (TEM) image in Fig. 1. For comparison, the control silicon pMOSFETs were also fabricated by almost the same process except $Si_{0.73}Ge_{0.27}$ epitaxy. The device characteristics were analyzed with Agilent b1500 and Keithley 4200 semiconductor parameter analyzers.

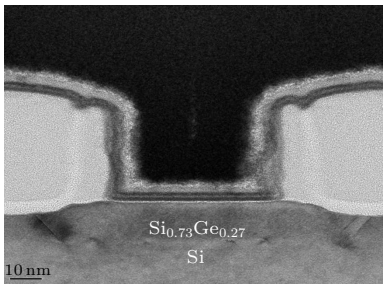

Fig. 1. Cross-sectional TEM image of a $Si_{0.73}Ge_{0.27}$ pMOSFET with HfO_2/TiN/TaN/TiN/W gate stacks. Here $Si_{0.73}Ge_{0.27}$ is capped with a thin silicon layer. The gate length of the device is 30 nm.

Typical transfer and output characteristics of a $Si_{0.73}Ge_{0.27}$ pMOSFET with gate length (L_G) of 30 nm and gate width (W_G) of 3 μm are shown in Figs. 2(a) and 2(b). In our measurements, source and substrate are set to 0 V or grounded, and the bias on gate and drain (V_{GS} and V_{DS}) are referred to source. It is seen in Fig. 2(a) that the $Si_{0.73}Ge_{0.27}$ device exhibits high ON/OFF ratio of 1.76×10^5 with saturation current (I_{SAT}) of 428 μA/μm and off-current (I_{OFF}) of 2.43 nA/μm, where I_{SAT} is extracted at $V_{GS} = V_{DS} = -1$ V and I_{OFF} is extracted at $V_{GS} = 0$ V and $V_{DS} = -1$ V. The short-channel effects are also analyzed. In our evaluation, the drain-induced barrier lowering (DIBL) is defined as $|V_{TLIN} - V_{TSAT}|$, where V_{TLIN} and V_{TSAT} are the threshold voltages at drain voltage $|V_{DS}| = 0.05$ and 1.0 V, respectively. The threshold voltages at the linear and saturated region (V_{TLIN} and V_{TSAT}) are −0.30 V and −0.22 V, which are extracted with the constant current (to be $W_G/L_G \times 100$ nA) method. Thus the DIBL of device is found to be about 77 mV/V, and it verifies good electrostatic control of gate over channel. In addition, the subthreshold swing (SS) is extracted to be 90 mV/decade for the linear transfer curve. It should be noted that the small values of DIBL and SS are mainly due to the thin equivalent oxide thickness (EOT) by using high-κ/metal gates. The output curves as seen in Fig. 2(b) show remarkable saturation when V_{DS} is less than −0.6 V.

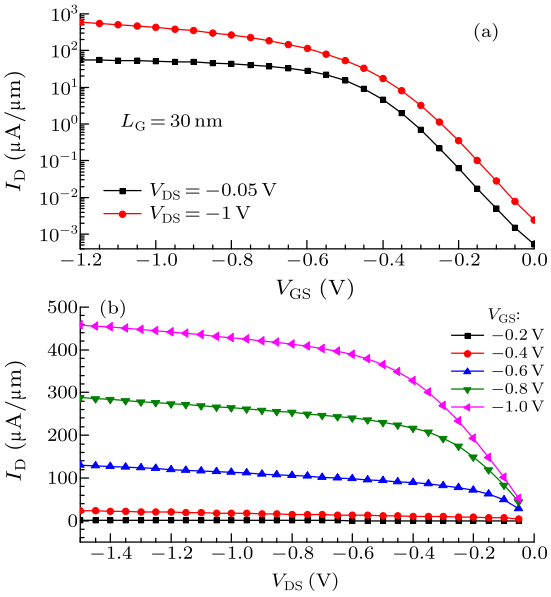

Fig. 2. Typical I_{DS}–V_{GS} (a) and I_{DS}–V_{DS} (b) characteristics of a $Si_{0.73}Ge_{0.27}$ pMOSFET with gate length of 30 nm.

To investigate the mobility enhancement of strained $Si_{0.73}Ge_{0.27}$ pMOSFETs, a large device with gate length of 16 μm and gate width of 8 μm was analyzed. The split C–V technique was used to measure the gate-to-channel capacitance (C_{GC}). The C_{GC}–V_{GS} curves of both $Si_{0.73}Ge_{0.27}$ and control silicon pMOSFETs are shown in Fig. 3(a), where the capacitance is measured at 100 kHz. The EOT of gate dielectric is estimated to be 0.9 nm. It is seen that C_{GC} increases as V_{GS} decreases in both pMOSFETs, while an extra plateau is uniquely shown over some range of V_{GS} (from −0.2 V to −0.5 V) in the $Si_{0.73}Ge_{0.27}$ device.

This can be explained by dual silicon and $Si_{0.73}Ge_{0.27}$ channels in $Si_{0.73}Ge_{0.27}$ pMOSFETs. Because the top of $Si_{0.73}Ge_{0.27}$ valence band is slightly lower than that of silicon, the inversion layer is first established in $Si_{0.73}Ge_{0.27}$ near Si-cap/$Si_{0.73}Ge_{0.27}$ interface as gate bias increases absolutely, and the measured capacitance forms the plateau as observed. Under this condition, since the effective thickness of gate dielectric is increased by the residual silicon cap, the corresponding capacitance saturates around a low value of 1.6 pF. When the gate bias increases further, high electric field will gradually overcome the small band offset, and consequently the portion of carriers in the silicon cap layer increases correspondingly. Therefore the measured capacitances under small alternative voltages in both the devices are almost equal when the gate bias is high enough. The inset of Fig. 3(a) shows the I_{DS}–V_{GS} curves of the same two devices at $V_{DS} = -0.05$ V. It is found that drain current in the $Si_{0.73}Ge_{0.27}$ pMOSFET is about two times that of the silicon transistor.

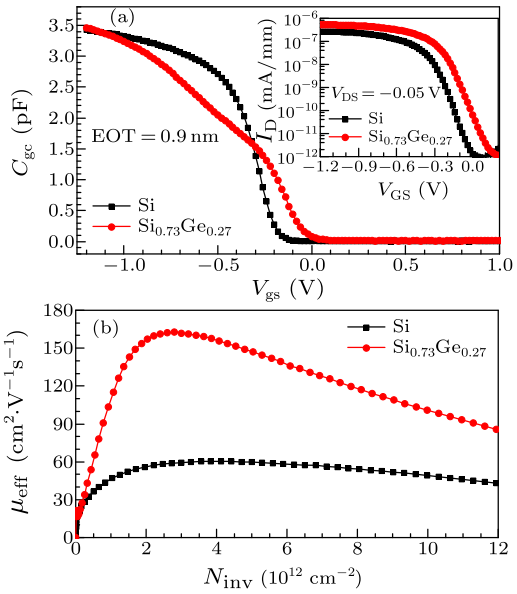

Fig. 3. (a) Split C–V and (b) effective hole mobility (μ_{eff}) in $Si_{0.73}Ge_{0.27}$ and Si pMOSFETs with gate length and width of 16 μm and 8 μm, respectively. Inset in (a) shows the I_D–V_{GS} curves at $V_{DS} = -0.05$ V of the same two devices.

The effective hole mobilities (μ_{eff}) as a function of carrier concentration (N_{inv}) in $Si_{0.73}Ge_{0.27}$ and silicon pMOSFETs are extracted from the data in Fig. 3(a), as shown in Fig. 3(b). It is obvious that much higher mobility is achieved in the $Si_{0.73}Ge_{0.27}$ transistor than the silicon device. The enhancement of hole mobility is primarily due to the reduced effective hole mass in the strained $Si_{0.73}Ge_{0.27}$ epitaxy layer.[3] The mobility increases with N_{inv} at first, and the highest μ_{eff} in the $Si_{0.73}Ge_{0.27}$ pMOSFET is up to 160 $cm^2V^{-1}s^{-1}$ at 2.2×10^{12} cm^{-2}. However, the mobility in $Si_{0.73}Ge_{0.27}$ pMOSFET drops more greatly than the silicon transistor for high N_{inv}. It is known from the above analysis that the inversion layer moves from $Si_{0.73}Ge_{0.27}$ to silicon as gate bias increases. The degraded mobility for high N_{inv} in $Si_{0.73}Ge_{0.27}$ device compared with the silicon device is partially due to larger effective mass in silicon than $Si_{0.73}Ge_{0.27}$. Another reason can be that the interface scattering in $Si_{0.73}Ge_{0.27}$ device increases more severely, since the location of the whole inversion layer shifts a longer distance towards the interface as the absolute gate bias increases from 0 V to high voltage.

It is known that layout has a strong influence on the strain relaxation in Si_xGe_{1-x}, and therefore affects the improvement of device performance.[23] Figure 4 shows the linear I_{DS}–V_{GS} curves of two $Si_{0.73}Ge_{0.27}$ and silicon pMOSFETs with gate length of 30 nm and gate width of 3 μm. It is seen that the drive current at $V_{DS} = -1$ V is improved by 26 % in the $Si_{0.73}Ge_{0.27}$ device. The improvement for this short-channel device is significantly reduced compared with the long-channel device as discussed above, which can be attributed to the increasing strain relaxation especially in the channel direction as the channel length decreases. It should be noted that all these $Si_{0.73}Ge_{0.27}$ devices can be optimized by selecting a more suitable thickness of silicon cap. The performance improvement as reported in short-channel devices can be further improved by more deliberate layout design.

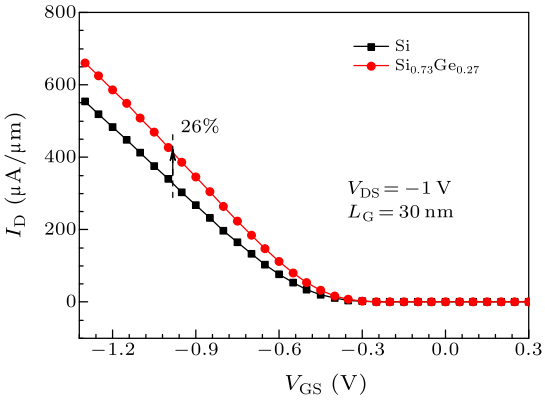

Fig. 4. Drive current comparison between Si and $Si_{0.73}Ge_{0.27}$ channel pMOSFETs with the gate length of 30 nm. The gate length of the transistors is 30 nm. The 26% current increase is shown at $V_{DS} = -1$ V.

In summary, the strained-$Si_{0.73}Ge_{0.27}$ channels have been successfully integrated with high-κ/metal gates in pMOSFETs by using the replacement post-gate process. It is found that the improvement of hole mobility is more than 100% by using $Si_{0.73}Ge_{0.27}$ channels in long-gate-length pMOSFETs. The fabricated $Si_{0.73}Ge_{0.27}$ pMOSFETs with gate length of 30 nm show well suppressed short-channel effects (DIBL~77 mV/V and SS~90 mV/decade) and good electrical performance (I_{SAT} ~428 μA/μm and I_{SAT}/I_{OFF} ~1.76×10^5 at $V_{DD} = 1$ V). Although the

enhancement of device performance is reduced as the gate length decreases due to strain relaxation, 26% increase of drive current is still achieved for 30-nm-gate-length $Si_{0.73}Ge_{0.27}$ devices. Device performance can be further improved by optimizing the thickness of the silicon cap layer and/or layout.

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