Comparison of GaN/AlGaN/AlN/GaN HEMTs Grown on Sapphire with Fe-Modulation-Doped and Unintentionally Doped GaN Buffer: Material Growth and Device Fabrication *

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AlGaN/GaN high electron mobility transistors (HEMTs) grown on Fe-modulation-doped (MD) and unintentionally doped (UID) GaN buffer layers are investigated and compared. Highly resistive GaN buffers ($10^9\,\Omega\cdot$cm) are induced by individual mechanisms for the electron traps' formation: the Fe MD buffer (sample A) and the UID buffer with high density of edge-type dislocations ($7.24\times10^9\,cm^{-2}$, sample B). The 300 K Hall test indicates that the mobility of sample A with Fe doping ($2503\,cm^2V^{-1}s^{-1}$) is much higher than sample B ($1926\,cm^2V^{-1}s^{-1}$) due to the decreased scattering effect on the two-dimensional electron gas. HEMT devices are fabricated on the two samples and pulsed I–V measurements are conducted. Device A shows better gate pinch-off characteristics and a higher threshold voltage (−2.63 V) compared with device B (−3.71 V). Lower gate leakage current $|I_{GS}|$ of device A (3.32×10^{-7} A) is present compared with that of device B (8.29×10^{-7} A). When the off-state quiescent points Q_2 ($V_{GQ2}=-8$ V, $V_{DQ2}=0$ V) are on, V_{th} hardly shifts for device A while device B shows +0.21 V positive threshold voltage shift, resulting from the existence of electron traps associated with the dislocations in the UID-GaN buffer layer under the gate. Under pulsed I–V and transconductance G_m–V_{GS} measurement, the device with the Fe MD-doped buffer shows more potential in improving reliability upon off-state stress.

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Due to the intrinsic strong spontaneous and piezoelectric polarization, AlGaN/GaN high electron mobility transistors (HEMTs) can obtain high speed, large current, and high breakdown voltage characteristics.[1,2] Meanwhile, the growth of the highly resistive (HR) GaN buffer layer is required to prevent the buffer leakage current, and to provide insulation and carrier confinement.[3,4] However, for the growth of Ⅲ-nitride-based HEMT structures on the foreign substrate (SiC, Al_2O_3, Si), the UID-GaN buffer is normally known to be n-type by impurity auto-doping of O and Si which originate from the substrates by thermal etching, recapture and diffusion.[5,6] In addition, the interface between the epitaxial layer and the substrate is a critical region of the device where impurities such as Si and O gather and induce a thin, degenerate conductive n-type region.[7,8] These two factors will deteriorate the reverse-bias (RB) buffer leakage. Previously, the HR-GaN buffer could be obtained through UID-GaN with high density of edge-type threading dislocations (ETDs) because ETDs in the GaN buffer behave as electron traps and compensate for the background electrons.[9,10] However, a high amount of threading dislocation densities (TDDs) may result in increased RB gate leakage current[11,12] and the traps associated with high TDDs deteriorate the reliability of the AlGaN/GaN HEMTs.[13] Therefore, a more reliable method to obtain HR-GaN should be developed without degrading devices' performance so much.

The Fe-doped GaN buffer layer in GaN HEMTs has also shown to be effective in forming isolation property.[5,6] Modulation-doped GaN buffer near the GaN/sapphire substrate was proposed for compensation of the n-type region near the GaN/Al_2O_3 interface. However, there is a lack of a systematic comparison between the as-grown HEMT structures and HEMT devices on UID and the Fe-MD GaN buffer layer.

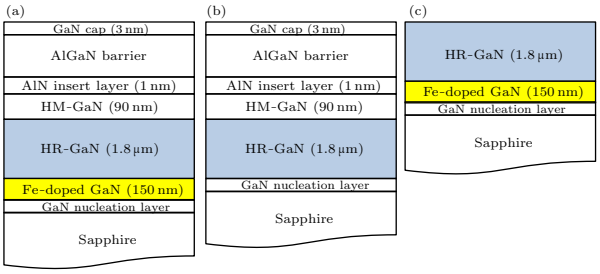

Fig. 1. Schematic diagrams of the HEMT structures investigated: (a) the HEMT structure with the Fe-doped buffer (sample A), (b) the HEMT structure without the Fe-doped buffer layer (sample B), (c) the HR Fe-doped GaN buffer structure (sample C).

In this Letter, we focus on the growth and characterization of GaN HEMTs on sapphire with and without Fe-doped buffer layers. Chemical, structural, and electrical properties of these structures are investigated and compared. Secondary mass ion mass spectroscopy (SIMS, by EAGLABS® PCOR-

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SIMS®) depth profiles, high resolution x-ray diffraction (HRXRD, by PANalytical X'Pert^3 MRD), x-ray reflectivity (XRR), atom force microscopy (AFM) are performed to study the structural properties and crystalline quality, while electrical properties were obtained by the room temperature Hall measurements. GaN HEMT devices were also fabricated and characterized.

The epitaxial HEMT structures investigated are schematically shown in Fig. 1. Fe-doped epitaxial (Al) GaN-layer systems (samples A and C) are grown on the *c*-plane sapphire substrate by metal-organic chemical vapor deposition (MOCVD). The growth of the HEMT structures began with a thin low temperature GaN nucleation layer. Modulation doping of Fe was adopted and about 10^{19} atom/cm^3 is introduced in this lattice during the early stage of epitaxy. Indeed, a 150-nm Fe-doped GaN buffer was followed up to growth. Then the ferrocene source is switched off and a 1.8-μm HR-GaN buffer layer was grown. On this buffer layer, a 90-nm high mobility (HM) GaN channel layer was deposited. Afterwards, the growth was completed by deposition of a 1-nm AlN insert layer, an undoped AlGaN barrier layer and a 3-nm GaN cap layer. The HM-GaN channel layer and the AlN interlayer were simultaneously employed to further improve the two-dimensional electron gas (2DEG) transport properties.[14] The detailed material growth method could be found in Refs. [14,15]. To study the impact of the Fe-doped buffer layer, sample B with a UID-GaN buffer (without Fe doped) buffer was also grown for comparison. The HR Fe-doped GaN buffer was grown as sample C for characterization.

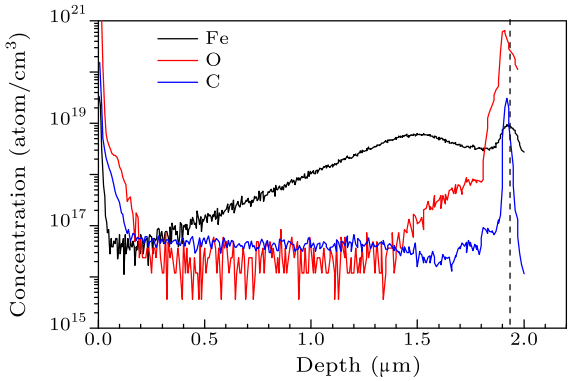

Fig. 2. SIMS depth profiles concerning Fe, O, C elements for as-grown sample C. The dotted line indicates the GaN/sapphire interface.

The HR-GaN buffer is very critical for HEMTs to avoid the reverse-biased parallel conduction path.[16] The resistivity was measured to be higher than $10^9\,\Omega$·cm for both buffers.

HEMT devices were fabricated on samples A and B. Ohmic contact metal was first formed. Mesa isolation was conducted by ICP dry etching. Schottky gate was sputtered and lifted off. Afterwards, PECVD-Si_3N_4 was deposited as the passivation layer. The measured devices have a gate length $L_g = 3\,\mu$m, a gate width $W = 100\,\mu$m, a gate-to-source distance $L_{gs} = 5\,\mu$m, and a gate-to-drain distance $L_{gd} = 20\,\mu$m.

To understand the diffusion and incorporation of Fe into the layer structure of sample C, SIMS depth profiles are shown in Fig. 2. For clarity, the profiles are limited to the upper 2 μm of the sample. It is found that O impurities with a concentration of 8×10^{20} cm^{-3} are incorporated at the GaN/sapphire interface, which may be caused by the diffusion of O from the sapphire substrate (Al_2O_3). This thin layer may induce additional charge near the interface, causing the leakage through the buffer layer. As shown in Fig. 2, the high Fe concentration ($\sim 1 \times 10^{19}$ cm^{-3}) necessary to compensate for the residual conductivity in GaN is responsible for a significant roughening of the growth front (Fe morphactant effect reported elsewhere[6]) and cannot be maintained for thick layers. Indeed, the ferrocene source is only used for 150 nm and then is switched off to allow the smoothing of the surface during the growth of the remaining part of the GaN template. The profiles for other contaminants like C and O remain unchanged through the upper 1.3 μm, probably because they are not far from the detection limit.

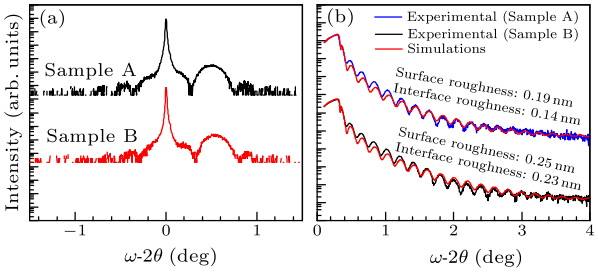

Fig. 3. (a) Measured HRXRD near the (004) reflections plane in TA mode of samples A and B with simulation curves, and (b) XRR curves of samples A and B.

Figure 3(a) shows the triple-axis (TA) HRXRD scan (ω–2θ) of samples A and B. The Al content and the AlGaN thicknesses are calculated to be 0.23, 22.5 nm (sample A), and 0.25, 23 nm (sample B), respectively. Figure 3(b) gives the XRR curves. Strong periodical oscillations (nearly 20 Kiessing fringes) can be observed for both the samples. The surface and interface roughness for sample A (AlGaN/GaN structure established for simulations as a simplification) show as 0.19 and 0.14 nm, while they are 0.25 and 0.23 nm for sample B. This indicates that sharp interfaces in both samples have been formed during the material growth, providing fine platforms for the 2DEG formation. The measured RMS surface roughnesses for samples A and B by AFM are 0.23 and 0.26 nm, respectively, showing good consistency with our simulations.

X-ray rocking curves (XRC) were measured and the peak full width at half maximum (FWHM) is presented in Fig. 4. As we know, the FWHM for the (0002) plane is sensitive to screw dislocation densities (SDDs) and the $(10\bar{1}2)$ plane is sensitive to both SDDs and edge dislocation densities (ETDs). SDDs and ETDs are calculated by using models in Ref. [17]. SDDs in samples A and B are calculated

to be 7.87×10^7 and $1.46 \times 10^8\,\mathrm{cm}^{-2}$, respectively. The ETDs in samples A and B are calculated to be 9.90×10^8 and $7.78 \times 10^9\,\mathrm{cm}^{-2}$. Compared with GaN HEMTs grown on the UID-GaN buffer, nearly an order magnitude lower TDDs is observed in GaN HEMTs grown on the Fe-doped GaN buffer. Thus better material quality has been obtained in the Fe-doped GaN buffer without degrading the HR property.

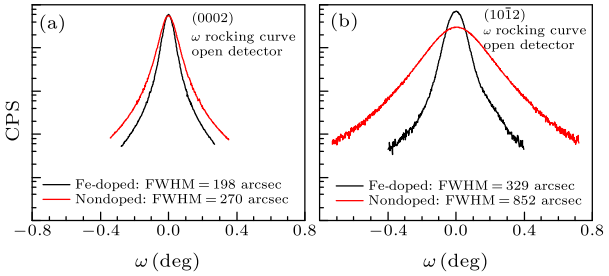

Fig. 4. (a) Symmetric (0002) diffraction plane and (b) screw diffraction (10$\bar{1}$2) XRC of the GaN buffer for wafer A (black) and wafer B (red).

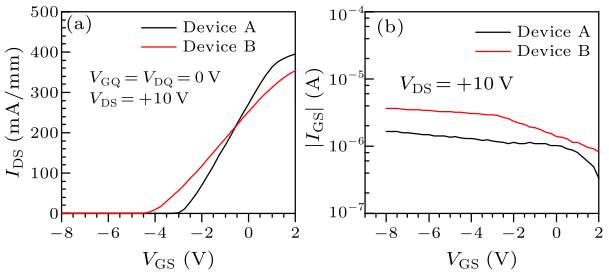

Fig. 5. (a) Transfer characteristics I_{DS}–V_{GS} of both devices and (b) measured gate leakage $|I_{GS}|$–V_{GS} characteristics ($V_{DS} = +10$ V).

Room temperature Hall tests are measured. The measured 2DEG sheet density n_S of sample A ($8.07 \times 10^{12}\,\mathrm{cm}^{-2}$) is slightly lower than sample B ($8.15 \times 10^{12}\,\mathrm{cm}^{-2}$). The lower 2DEG sheet density may be related to the smaller Al content and thinner AlGaN barrier thickness in sample A (0.23, 22.5 nm) compared with sample B (0.25, 23 nm). The 300 K Hall 2DEG mobilities (μ_{2DEG}) for the two samples are 2503 and $1926\,\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$. The improved electron mobility of sample A can be explained by the combination of the reduced scattering of dislocation,[14,18] interface roughness, alloy disorder, polar optical phonons and acoustic phonons.[19] We have also conducted theoretical investigations and found that the decrease of TDDs can improve 2DEG mobility effectively.[14] Further, the sheet resistances R_{sh} were measured to be $348\,\Omega$/square and $373\,\Omega$/square for samples A and B, respectively.

The I_{DS}–V_{GS} transfer characteristics of both devices are presented in Fig. 5(a). Measurements were conducted in the pulsed mode and the self-heating effect can be ignored.[20] Each test pulse period consists of a 300 μs on-state pulse, followed by a 99.7 ms off-state pulse (0.3% duty cycle) at the quiescent bias point Q (V_{GQ}, V_{DQ}). Here Q_0 (V_{GQ0}, V_{DQ0}) is set at (0 V, 0 V). The maximum current densities I_{DSmax} of the two devices are 395 and 354 mA/mm for devices A and B, respectively. Larger I_{DSmax} of device A results from lower R_{sh} for sample A. The threshold voltage V_{th} is also extracted to be −2.63 V and −3.71 V for devices A and B, respectively.[21] While in device A, Fe doping in GaN buffer works as electron traps,[22] showing as a back barrier under the 2DEG channel. As shown in Fig. 5(a), the transfer characteristics of device A show a sharper pinch-off performance compared with device B. This means that the electron distribution in the 2DEG channel of device B is more dispersed and harder for the gate to pinch off. Thus the mean 2DEG/gate distance for device B shall be larger than device A. Therefore, the measured $|V_{thB}|$ (3.71 V) is higher than $|V_{thA}|$ (2.63 V). Figure 5(b) shows the measured gate leakage current $|I_{GS}|$ during the dc transfer characteristics. Here $|I_{GS}|$ of device A is 3.32×10^{-7} A while $|I_{GS}|$ of device B is 8.29×10^{-7} A ($V_{GS} = -8$ V). Higher gate leakage in device B is caused by the increased TDDs which work as the leakage paths.[12,23] Thus, device B with the UID-GaN buffer shows degraded pinch-off characteristics, along with lower I_{DSmax} and higher $|I_{GS}|$, compared with device A with the Fe MD-doped buffer. This indicates that it is more practical to fabricate high-power GaN HEMTs on the Fe-doped GaN buffer with high performance for power switching applications.

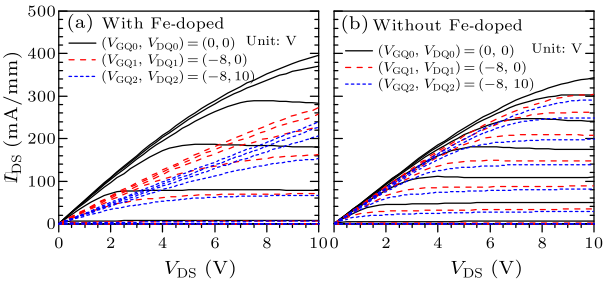

Fig. 6. Pulsed I_{DS} versus V_{DS} characteristics of devices (a) A and (b) B. Measurements are taken under different quiescent bias points (V_{GQ}, V_{DQ}), as indicated in the graph. Each test pulse period consists of a 300 μs on-state pulse, followed by a 99.7 ms off-state pulse (0.3% duty cycle). Here V_{GS} is taken from −8.0 V to +2.0 V in steps of 1.0 V.

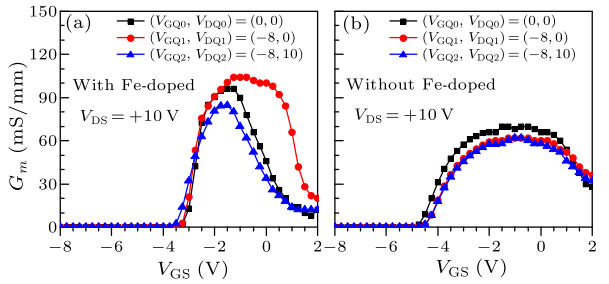

Fig. 7. Pulsed G_m–V_{GS} characteristics for devices (a) A and (b) B.

The trapping phenomenon of devices were characterized by using pulsed I_{DS}–V_{DS} and transconductance G_m–V_{GS} measurements, as shown in Figs. 6 and 7.[24] The same pulse method in Fig. 5 is used

here while three quiescent points are adopted. (1) Q_0: (V_{GQ0}, V_{DQ0})=(0 V, 0 V) characterized by negligible electron trapping; (2) Q_1: gate lag with (V_{GQ1}, V_{DQ1})=(−8 V, 0 V); and (3) Q_2: drain lag with (V_{GQ2}, V_{DQ2})=(−8 V, 10 V). The extracted on-state resistance change $\Delta R_{on}/R_{on}$ (%) from Fig. 6, the threshold voltage shift ΔV_{th} and the peak transconductance change $\Delta G_m/G_m$ (%) from Fig. 7 are all summarized in Table 1. The subscriptions 1 and 2 stand for the data measured under Q_1 and Q_2, respectively. All data are compared with the data measured at Q_0.

As indicated in Ref. [24], the traps associated with the high density of defects located below the gate region causes predominantly threshold voltage (V_{th}) dynamical shift, while the traps in the gate-drain access region results in a dynamic increase of the peak transconductance (G_m) with no V_{th} shift. As shown in Fig. 7(a), nearly zero shift of V_{thA} (−0.03 V) is observed when (V_{GQ1}, V_{DQ1})=(−8 V, 0 V) is applied for device A, meaning that almost no traps are present under the gate region (including the dislocation and point defect related traps). The Fe concentration in HM-GaN is low (Fig. 2) due to the MD method and thus, the trapping phenomenon is hardly observable. This shows more advantage compared with the continuously doped Fe buffer.[25] For device B, there exists a +0.21 V change for V_{thB} (Fig. 7(b)). When the gate is biased at the off state (V_{GS} = −8 V), electrons will fill in the traps related to the high density of dislocations in the UID-GaN region under the gate, increasing the net negative charge. As a result, n_S decreases and V_{th1} for device B meets a positive shift.[24] As for the dynamic G_m, both devices show certain decreases due to the trapping of electrons in the region between gate and drain.[26] Higher $\Delta G_{m1}/G_{m0}$ of device B (11.4%) is present compared with device A (7.50%), which seems to mean that the gate-drain surface traps of device B show more severe effect on the conductance. Then the gate-drain access region shall meet a relatively higher resistance rise for device B. However, the increase of the on-state resistance $\Delta R_{on1}/R_{on0}$ is relatively lower for device B (8.84%) than device A (40.5%). The possible explanation for this discrepancy should be that the Fe-doping has changed the surface states of device A and the deposition condition of the PECVD-Si_3N_4 passivation layer is not optimized to totally eliminate the surface traps. The surface traps may come from the dangling bond at surface[27] or the iron-related traps[22] due to the doping diffusion. Previous researchers have used natural oxide removal, nitridation and ALD-Al_2O_3 to passivate the dangling bond at the GaN surface to decrease the interface trap density.[27] As for device B, although the gate-channel resistance increases due to the partially 2DEG depletion by the dislocation-traps under the gate, the PECVD-Si_3N_4 layer is already enough to passivate the surface traps and the gate-drain resistance will not rise so much as device A. As a result, the total resistance R_{on} consisting of both gate-channel resistance and the gate-drain access region resistance[28] will increase relatively higher for device A (40.5%) when the off-state quiescent bias point Q_1 is on (V_{GQ1} = −8 V, V_{DQ1} = 0 V).

Table 1. Extracted threshold voltage shift ΔV_{th}, the peak transconductance change $\Delta G_m/G_m$ (%) and the on-state resistance change $\Delta R_{on}/R_{on}$ (%). The subscriptions 1 and 2 stand for the data measured under the quiescent points Q_1 and Q_2, respectively. Furthermore, all data are compared with the data measured at Q_0 (V_{GQ0}, V_{DQ0}) = (0 V, 0 V).

Devices	ΔV_{th1} (V)	$\Delta G_{m1}/G_{m0}$ (%)	$\Delta R_{on1}/R_{on0}$ (%)	ΔV_{th2} (V)	$\Delta G_{m2}/G_{m0}$ (%)	$\Delta R_{on2}/R_{on0}$ (%)
Device A	−0.03	7.50	40.5	−0.17	18.7	127
Device B	+0.21	11.4	8.84	+0.3	11.4	13.0

Our thought is further confirmed when Q_2 (V_{GQ2} = −8 V, V_{DQ2} = 10 V) is applied. For device B, the pulsed G_{m2}–V_{GS} curve does not change that much from the G_{m1}–V_{GS} curve, meaning that the trapping status of surface states in device B keeps passivated or saturated. Here $\Delta R_{on2}/R_{on0}$ also does not change that much in device B (13.0% for Q_2 and 8.84% for Q_1). However, for device A, an obvious decrease in $\Delta G_{m2}/G_{m0}$ (18.7%) indicates that the surface trapping becomes more active when a large drain-gate voltage (+18 V) is applied. Meanwhile, $\Delta R_{on2}/R_{on0}$ meets a significant rise to 127% for device A due to the higher gate-drain resistance. It should be noted that with proper optimization of the growing conditions for the PECVD-Si_3N_4 layer on device A, the surface traps can be passivated just as device B.[29] Further study for dielectric passivation on HEMTs with the Fe-doped buffer is on-going in our group. Therefore, the current collapse in device A is mainly due to the surface traps, while buffer traps contribute more in device B. Unlike the inherent traps in the UID-GaN buffer layer, the surface traps related to the Fe MD-doped buffer can be removed through external processing steps such as the Si_3N_4 passivation layer. Therefore, the Fe MD-doped buffer is shown to be more advantageous in fabricating GaN HEMTs with high reliability.

In summary, AlGaN/GaN HEMTs grown on GaN buffer layers with/without Fe-MD have been fabricated. Both buffers show high resistivities ($10^9\,\Omega\cdot$cm) induced by individual mechanisms: high density of dislocations for conventional buffer ($7.24\times10^9\,cm^{-2}$) and Fe-doped electron traps in the Fe-doped buffer. The 300 K Hall mobility of sample A ($2503\,cm^2V^{-1}s^{-1}$) is much higher than sample B ($1926\,cm^2V^{-1}s^{-1}$) due to the decreased scattering effect on 2DEG. The maximum output current density is improved from 354 (device B) to 395 mA/mm (device A), and device A shows better gate pinch-off characteristics and a higher threshold voltage (−2.63 V). Moreover, device A shows merely no V_{th} shift when the off-state quiescent point Q_2 (V_{GQ2} = −8 V, V_{DQ2} = 0 V) is on while device B shows +0.21 V positive

threshold voltage shift, resulting from the existence of traps associated with high density of dislocations in the GaN buffer layer under the gate. Therefore, devices with the Fe MD-doped buffer can have more potential in improving reliability under the off-state stress. The obtained insight provides a key design scheme of GaN HEMTs with high reliability.

References

[1] Ikeda N, Niiyama Y, Kambayashi H, Sato Y, Nomura T, Kato S and Yoshida S 2010 *Proc. IEEE* **98** 1151
[2] Mishra U K, Shen L, Kazior T E and Wu Y F 2008 *Proc. IEEE* **96** 287
[3] Cao Y, Zimmermann T, Xing H L and Jena D 2010 *Appl. Phys. Lett.* **96** 042102
[4] Poblenz C, Waltereit P, Rajan S, Heikman S, Mishra U K and Speck J S 2004 *J. Vac. Sci. Technol.* B **22** 1145
[5] Lee W, Ryou J H, Yoo D, Limb J, Dupuis R D, Hanser D, Preble E, Williams N M and Evans K 2007 *Appl. Phys. Lett.* **90** 093509
[6] Bougrioua Z, Azize M, Lorenzini P, Laügt M and Haas H 2005 *Phys. Status Solidi* A **202** 536
[7] Look D C and Molnar R J 1997 *Appl. Phys. Lett.* **70** 3377
[8] Cheong M G, Kim K S, Oh C S, Namgung N W, Yang G M, Hong C H, Lim K Y, Suh E K, Nahm K S, Lee H J, Lim D H and Yoshikawa A 2000 *Appl. Phys. Lett.* **77** 2557
[9] Xu F J, Xu J, Shen B, Miao Z L, Huang S, Lu L, Yang Z J, Qin Z X and Zhang G Y 2008 *Thin Solid Films* **517** 588
[10] Wang X L, Chen T S, Xiao H L, Wang C M, Hu G X, Luo W J, Tang J, Guo L C and Li J M 2008 *Solid-State Electron.* **52** 926
[11] Hsu J W P, Manfra M J, Molnar R J, Heying B and Speck J S 2002 *Appl. Phys. Lett.* **81** 79
[12] Ganguly S, Konar A, Hu Z Y, Xing H L and Jena D 2012 *Appl. Phys. Lett.* **101** 253519
[13] Ťapajna M, Kaun S W, Wong M H, Gao F, Palacios T, Mishra U K, Speck J S and Kuball M 2011 *Appl. Phys. Lett.* **99** 223501
[14] Peng E C, Wang X L, Xiao H L, Wang C M, Yin H B, Chen H, Feng C, Jiang L J, Hou X and Wang Z G 2013 *J. Cryst. Growth* **383** 25
[15] Wang X L, Hu G X, Ma Z Y, Ran J X, Wang C M, Xiao H L, Tang J, Li J P, Wang J X, Zeng Y P, Li J M and Wang Z G 2007 *J. Cryst. Growth* **298** 835
[16] Selvaraj S L, Suzue T and Egawa T 2009 *IEEE Electron Device Lett.* **30** 587
[17] Srikant V, Speck J S and Clarke D R 1997 *J. Appl. Phys.* **82** 4286
[18] Jena D, Gossard A C and Mishra U K 2000 *Appl. Phys. Lett.* **76** 1707
[19] Lisesivdin S B, Yildiz A, Balkan N, Kasap M, Ozcelik S and Ozbay E 2010 *J. Appl. Phys.* **108** 013712
[20] Chini A, Soci F, Meneghini M, Meneghesso G and Zanoni E 2013 *IEEE Trans. Electron Devices* **60** 3176
[21] Chen W J, Wong K Y, Huang W and Chen K J 2008 *Appl. Phys. Lett.* **92** 253501
[22] Silvestri M, Uren M J and Kuball M 2013 *Appl. Phys. Lett.* **102** 073501
[23] Yan D W, Lu H, Cao D, Chen D S, Zhang R and Zheng Y D 2010 *Appl. Phys. Lett.* **97** 153503
[24] Meneghini M, Ronchi N, Stocco A, Meneghesso G, Mishra U K, Pei Y and Zanoni E 2011 *IEEE Trans. Electron Devices* **58** 2996
[25] Cardwell D W, Sasikumar A, Arehart A R, Kaun S W, Lu J, Keller S, Speck J S, Mishra U K, Ringel S A and Pelz J P 2013 *Appl. Phys. Lett.* **102** 193509
[26] Vetury R, Zhang N Q, Keller S and Mishra U K 2001 *IEEE Trans. Electron Devices* **48** 560
[27] Liu S, Yang S, Tang Z K, Jiang Q M, Liu C, Wang M J, Shen B and Chen K J 2015 *Appl. Phys. Lett.* **106** 051605
[28] Lu B and Palacios T 2010 *IEEE Electron Device Lett.* **31** 951
[29] Mizutani T, Ohno Y, Akita M, Kishimoto S and Maezawa K 2003 *IEEE Trans. Electron Devices* **50** 2015