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Selective Area Growth of GaAs in V-Grooved Trenches on Si(001) Substrates by Aspect-Ratio Trapping *

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A high quality of GaAs crystal growth in nanoscale V-shape trenches on Si(001) substrates is achieved by using the aspect-ratio trapping method. GaAs thin films are deposited via metal-organic chemical vapor deposition by using a two-step growth process. Threading dislocations arising from lattice mismatch are trapped by laterally confining sidewalls, and antiphase domains boundaries are completely restricted by V-groove trenches with Si {111} facets. Material quality is confirmed by scanning electron microscopy (SEM), transmission electron microscopy (TEM) and high resolution X-ray diffraction. Low temperature photoluminescence (PL) measurement is used to analyze the thermal strain relaxation in GaAs layers. This approach shows great promise for the realization of high mobility devices or optoelectronic integrated circuits on Si substrates.

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The Ⅲ–Ⅴ compound semiconductors are excellent materials of the optoelectronic devices due to their outstanding optical characteristics. Epitaxial growth of Ⅲ–Ⅴ compound semiconductors on Si substrates has attracted significant attention for many years due to the potential for monolithic integration of Ⅲ–Ⅴ optoelectronic devices with Si integrated circuits.[1] In recent years, the dimensions scale of metal oxide semiconductor field-effect transistor devices has reached its limits due to the increased device leakage and processing complexity. The interest of integrating GaAs and other high electron-mobility materials such as InGaAs on Si substrates is increasing dramatically. These materials can act as high mobility channels in complementary metal oxide semiconductor (CMOS) devices, offering the possibility to further increase the performance of future CMOS generations.[2,3] However, there are three major challenges for the direct epitaxial growth of GaAs on Si: the large lattice mismatch, the difference in the thermal expansion coefficient and the growth of a polar material on a nonpolar substrate. These lead to the high density of threading dislocations and antiphase domain boundaries (APBs) in GaAs layers.[4,5] Various epitaxial schemes have been used to try to reduce GaAs dislocation density, such as graded SiGe buffer layers, thermal cycles annealing (TCA), and strained-layer superlattices as dislocation filters.[6–8] However, to date, the disadvantage of these methods mean GaAs may not be acceptable for the co-integration of the CMOS process. For instance, the SiGe buffer will lead to the Ge diffusion to GaAs layers as an impurity. The TCA requires high annealing temperatures and the strained-layer superlattices make the process complex and difficult in practical applications.

Approaches involving selective area growth of Ⅲ–Ⅴ materials in the trenches with a high aspect ratio have shown some promise.[9–11] The defects arising from lattice mismatch (∼4%) are trapped by SiO_2 sidewalls. In the present study, a high-quality GaAs crystal was deposited in nanoscale V-shape trenches on Si (001) substrates by using the aspect-ratio trapping method. We contrast the crystal quality growth in plane bottom trenches with the growth in the V-shape trenches. The strain relaxation effect in the selective growth GaAs in V-shape trenches was studied by photoluminescence (PL) measurement.

Using photolithography and inductively coupled plasma etching (ICP), the trenches with 400 nm period were etched through 500-nm-thick PECVD-grown SiO_2 on 150 mm on-axis Si (001) substrates along the [110] direction. The GaAs layer was selectively deposited by using low-pressure metal organic chemical vapor phase deposition (MOCVD, AIXTRON 200), by using triethylgallium, trimethylgallium and arsine (AsH_3) as precursors. We compare the crystal quality of GaAs selectively grown in plane bottom trenches with V-groove trenches. Prior to epitaxy, the substrate of sample S1 was cleaned in 5% hydrogen fluoride (HF) solution to remove the native oxide. The Si wafers of samples S2 and S3 were etched in KOH solution for a sufficient time to produce the required V-shape trenches with {111} facets.[12] After rinsing with deionized water, the wafer of sample S2 was cleaned in 5% HF solution and the wafer of sample S3 was immersed in 10% HCl solution and 5% HF. As a final

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component to the pre-epitaxy cleaning process, the Si substrates of all the samples were thermally cleaned in a H_2 ambient at 720℃ for 20 min. When the wafers were being cooled from the H_2 baking temperature, AsH_3 was introduced into the reactor to terminate the Si {111} surfaces with As atoms. After this step, the GaAs epitaxy was initiated with the well-known two-step procedure. Low-temperature GaAs layers were selectively grown in V-groove trenches of Si (001) substrates at 400℃, as a nuclei layer. High temperature GaAs layers were then also selectively grown at 630℃. The GaAs crystal morphology imaging was obtained by a scanning electron microscope (SEM) and a transmission electron microscope (TEM). The crystalline quality of GaAs layers selectively grown in V-grooved trenches have also been characterized by high resolution X-ray diffraction (HRXRD) and low-temperature PL measurement at 80 K.

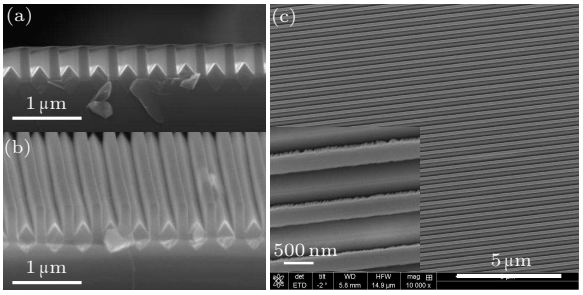


Fig. 1. SEM images of GaAs selective heteroepitaxial growth on patterned V-shape trenches Si(001) substrate: (a) the cross-sectional image taken on the [110] axis; (b) the cross-sectional image taken with a tilt around the [110] axis; (c) plan view taken in perpendicular to the (001) plane of the Si substrate. The inset in (c) shows a partial enlarge of plane view.

Figure 1 shows the SEM images of GaAs crystals obtained by selective growth in V-groove trenches on Si (001) substrates. Fig. 1(a) shows a cross-sectional image taken on the [110] axis, Fig. 1(b) was taken with a tilt around the [110] axis, and Fig. 1(c) was taken perpendicular to the (001) plane of the Si substrate. It is well known that APBs are characterized by pyramid-shaped pits or wedge-shaped surface defects which affect the surface morphology of selectively grown GaAs layers.[13,14] From SEM images, we can observe that all GaAs layers were grown in the V-shape trenches, form a perfect wedge with {111} surfaces between the SiO_2 lateral sidewalls, and the crystal morphology is uniform with a nearly flawless surface. This result demonstrates that an aspect-ratio trapping (ART) method with a V-shape trench can completely annihilate the APBs. In a V-shape trench, the surface of Si is {111} facets, and the single step on the Si {111} surface is equal to the interplanar spacing of Si {111} planes.[15,16] When the GaAs are deposited on Si {111} surfaces, unlike the single atom steps of {001} planes, such steps may not lead to the APBs in the GaAs material.

To accurately study the defect reduction in GaAs layers grown in V-shape trenches, TEM was taken on [001] (Fig. 2(a)), [110] (Fig. 2(b)) and [1$\bar{1}$0] (Fig. 2(c)) directions to sample S3, respectively. Dislocations originated at the GaAs/Si interface are completely trapped in the V-grooved trenches. As a result, a defect-free region was achieved on the above part of GaAs materials. Fig. 2(d) is a high-resolution TEM image taken on the [1$\bar{1}$0] axis of the sample S1. Comparing the crystal quality with sample S3, it is evident that the V-shape trenches have distinct advantages for GaAs selective epitaxy growth. We can explain this result by the fact that in the process of the V-shape trenches produced, the residual oxide, near-surface damage of the Si crystal resulting from the ICP etching process can be thoroughly removed by KOH etching, and it can also increase the aspect ratio of trenches on the Si substrate.

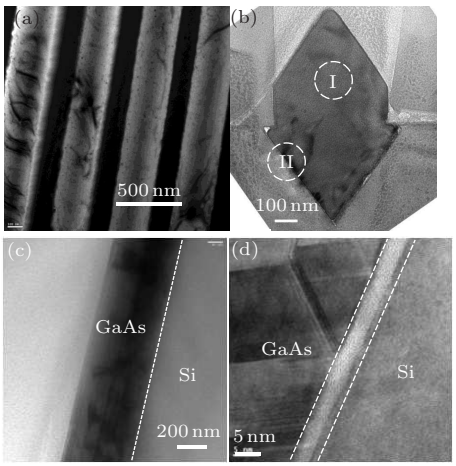


Fig. 2. TEM images of selective-area-growth GaAs on Si: (a) plane view TEM image of GaAs grown in V-shape trenches; (b, c) cross-sectional TEM images taken on [110] and [1$\bar{1}$0] directions of GaAs grown in V-shape trenches, respectively; (d) the cross-sectional TEM image taken on [1$\bar{1}$0] direction of GaAs grown in plane bottom trenches.

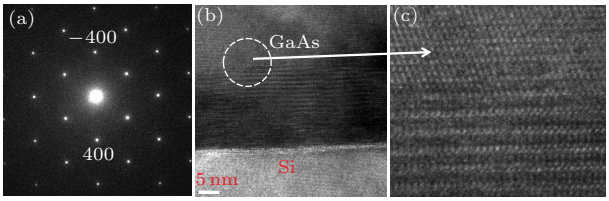


Fig. 3. (a) The diffraction pattern of region I; (b) the HRTEM image of GaAs/Si {111} interface of region Ⅱ; (c) the enlarged area marked in (b).

According to the diffraction patterns (Fig. 3(a)) taken at the GaAs top layer region, we can observe a face-centered cubic structure diffraction pattern of the ⟨110⟩ zone. This result indicates that the GaAs crystal has grown epitaxially in the V-groove trenches with a zinc blende structure. The high resolution TEM image of the Si and GaAs{111} interface in the bottom of the

trenches is given in Figs. 3(b) and 3(c) (a partial enlarged view). From Figs. 3(b) and 3(c), a series of microtwins and stacking faults parallel with the GaAs/Si interface can be observed. These twins/stacking faults will relieve misfit strain between GaAs and Si, which is caused by a/6 ⟨112⟩ type partial dislocation.[17,18] These defects cannot propagate to the top region of the GaAs layers.

XRD characterization was performed to further investigate the crystal quality of GaAs grown in different trenches. Figure 4 shows XRD $\omega - 2\theta$ scans recorded around (004) Bragg reflection of the Si substrate to samples S1 (red line), S2 (black line) and S3 (brilliant blue line). The GaAs XRD full width at half maximum (FWHM) and peak intensity are relisted in Table 1. The XRD peak positions suggest that the GaAs lattice has fully relaxed (4% lattice mismatch) with respect to Si. The FWHM of the rocking curve of the sample S3 (004) diffraction peak is 217 arcsec. A significant improvement in FWHM and intensity (recorded in Table 1) of XRD scans was shown from S1 to S3, which reflects a more obvious improvement of GaAs crystal quality in V-grooved trenches than the plane bottom trenches, and these results are identical with the TEM images. It is evident that a HCl solution cleaned process is indispensable to remove KOH etching reactions that might be attached in the bottom of the trenches.

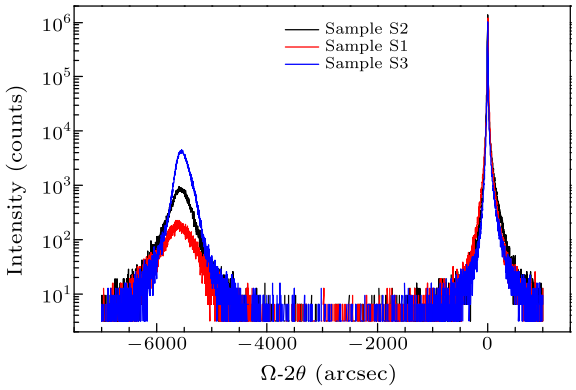


Fig. 4. HRXRD diffraction curves of the GaAs grown on ART patterned Si(001) substrates.

Table 1 The results of XRD of FWHM, intensity I and PL about FWHM, energy band (EB)

Sample	HRXRD		Photoluminescence	
	FWHM (arcsec)	I	FWHM (meV)	EB (eV)
S1	266	225		
S2	262	943	39.7	1.490
S3	217	4503	24.2	1.501
S4			9.4	1.472

The PL measurement is an effective means to characterize the strain existing in GaAs crystals.[19] Figure 5 shows the result of low-temperature PL measurement at 80 K of samples S2 (black line), S3 (blue line) and S4 (red line, GaAs grown on unpatterned Si substrate with Ge buffer layers). The FWHM and peak intensity are relisted in Table 1. The vertical dashed line at 1.509 eV is the energy band gap of intrinsic GaAs at 80 K (theoretical calculation[20]). A redshift of PL intense peak was observed in our samples, which is due to the residual biaxial tensile strain induced by the thermal expansion mismatch between Si and GaAs.[21] By comparing the results of samples S3 and S4, the GaAs selective growth in V-shape trenches shows a more significant shortage in redshift distance than growth on unpatterned Si substrates with Ge buffer layers: the sample S3 with only shift 8 meV and the sample S4 with a large 36 meV redshift. This result proves that the method of selective area growth of GaAs in V-grooved trenches can efficiently relax the strain of GaAs crystals grown on Si substrates.

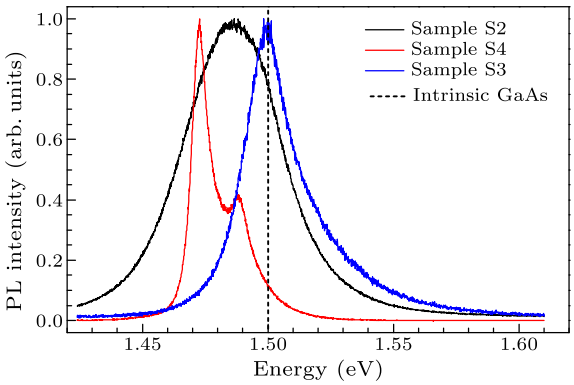


Fig. 5. PL spectra at $T = 80$ K of the GaAs grown on Si substrates.

In summary, we have demonstrated a high-quality GaAs film in V-shape trenches on Si(001) on-axis substrates, and we have performed a two-step growth approach by combining a low temperature nucleation layer to promote the GaAs growth onto the Si surface with a high temperature main layer to enhance the crystalline quality of the epitaxy layer inside the SiO_2 trenches. Dislocations originated at the GaAs/Si interface are completely trapped on the SiO_2 sidewalls and APBs were eliminated very well by the V-shape trenches. This method can also efficiently relax the strain induced by the thermal expansion mismatch of GaAs and Si. A comparison of crystal quality was made to the GaAs growth in V-shape trenches with in-plane bottom trenches. Those results are promising for realization of optoelectronic integration circuits and high-mobility devices on Si substrates.

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