The Distinguished Charge-Trapping Capability of the Memory Device with Al_2O_3-Cu_2O Composite as the Charge Storage Layer *

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A memory device $Si/Al_2O_3/Al_2O_3$-$Cu_2O/Al_2O_3/Pt$ is fabricated by using atomic layer deposition and rf-magnetron sputtering techniques. The memory device including the composite of Al_2O_3 and Cu_2O as the charge storage layer shows a distinguished charge trapping capability. At a working voltage of ±11 V a memory window of 9.22 V is obtained. The x-ray photoelectron spectroscopic study shows a shoulder from Cu^{2+} ions around the peak of Cu^{1+} ions. It is suggested that the charge-trapping mechanism should be attributed to the defect states formed by the inter-diffusion at the interface of two oxides.

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The charge-trapping memory (CTM) devices, such as the poly-silicon-oxide-nitride-oxide-silicon-type (SONOS) structure memories including nitride memories and nanocrystals (NCs) memories, have received much attention for the application in the next-generation non-volatile memories due to their low operating voltage, fast program/erase speed, good endurance and retention characteristics.[1−6] In an SONOS-structure device, the thickness of the tunneling oxide is reduced to improve the program/erase (P/E) speed and operation.[7] The thinner tunneling oxide may cause poor stability and reliability of such devices. Recently, Al_2O_3 has been proposed for the tunneling and blocking layers and some high-k oxides and NCs, such as HfO_2, TiO_2, ZrO_2, have also been employed to replace Si_3N_4 layers for faster P/E speed and better retention property than the conventional SONOS devices.[8−11] However, these improvements especially in the charge trapping capability are still not enough to meet the requirements of high density and low working voltage.

In this Letter, we report a memory device with the structure $Si/Al_2O_3/Al_2O_3$-$Cu_2O/Al_2O_3/Pt$, in which the charge-trapping layer, a composite of two oxides, shows a distinguished charge trapping capability.

The p-type (100) silicon wafer with a resistivity of 1–10 Ωcm was used as the substrate. Before the deposition, the wafer was ultrasonically cleaned in the alcohol for 3 min, and then in deionized water for 3 min. After ultrasonic cleaning, the wafer was immersed in HF diluted solution ($HF:H_2O$=1:10) for 30 s to remove the native oxide, then the wafer was cleaned by the deionized water to remove the HF, and was dried by a nitrogen gas gun.

The cleaned silicon wafer was transferred to the atomic-layer-deposition (ALD) reactor chamber and an Al_2O_3 layer with a thickness of 3 nm was deposited as the tunneling layer at 200℃. The $(Cu_2O)_5(Al_2O_3)_5$ (CAO) charge-trapping layer was deposited by using rf-magnetron sputtering technique with a mixed ceramic target in a mole ratio of Cu_2O:Al_2O_3=5:5. The reactor chamber was under a mixed ambience of argon and oxygen (3:1) at 4 Pa, and the rf power was 100 W. The Al_2O_3 blocking layer with a thickness of 15 nm was deposited by the ALD technique. Finally, Pt top electrodes with an area of 1.77×10^{-4} cm^2 were deposited by using the magnetron sputtering technique at room temperature. Ag silver paste was spread on the back side of the silicon wafer as the bottom electrode. The structure of CAO charge trapping memory device was schematically shown in Fig. 1. Before depositing the Pt electrode on the Al_2O_3 blocking-layer, the device undergoes a rapid annealing treatment (RTA) at 200℃ in N_2 for 40 s.

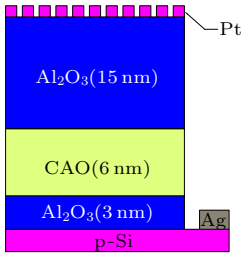

Fig. 1. Schematic of the structure of the CAO charge-trapping memory device.

Keithley 4200 semiconductor characterization system (Keithley 4200 SCS) was used to characterize the electric properties of the CAO charge trapping memory device at CasCade Summit 12000B-M platform. The cross-sectional morphology of the memory device was characterized by using the high resolution transmission electron microscopy (HRTEM) (Tecnai F20).

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The chemical valences of atoms contained in CAO film were characterized by using x-ray photoelectron spectroscopy (XPS) with the Thermo ESCALAB 250 system.

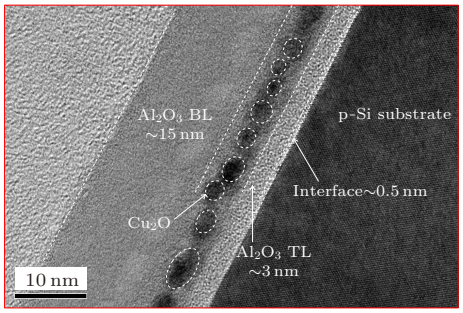

Fig. 2. The cross-sectional HRTEM image of the CAO charge-trapping memory device.

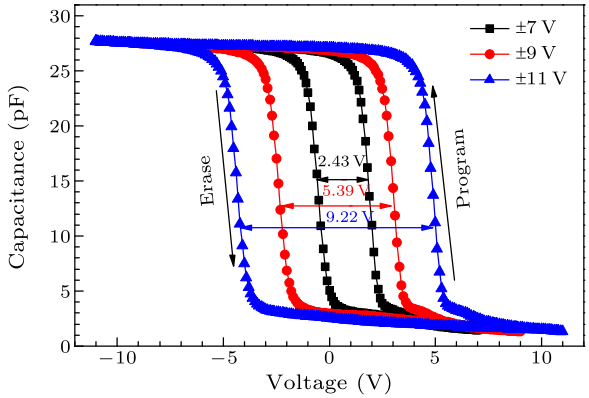

Fig. 3. The C–V curves of the CAO memory device at 1 MHz.

The cross-sectional HRTEM morphology of the CAO charge-trapping memory device is shown in Fig. 2. The figure presents the structure of Si substrate/Al_2O_3 tunneling oxide/CAO charge-trapping layer/Al_2O_3 blocking oxide. From Fig. 2, thicknesses of the Al_2O_3 tunneling layer, CAO charge-trapping layer and Al_2O_3 blocking layer are about 3 nm, 6 nm and 15 nm, respectively, well in accordance with our design. The interface between the Si substrate and the Al_2O_3 tunneling layer is quite sharp, and only 0.5 nm thickness of interface could be observed, indicating slight inter-diffusion at the interface. In addition, some egg-shaped black regions can be observed in the charge-trapping layer, in which no clear lattice image could be observed. Considering the fact that Al_2O_3 is amorphous at the annealing temperature, the black region should be the quasi-crystallized Cu_2O due to the high concentration of Cu_2O in the target.

Figure 3 shows the high-frequency (1 MHz) capacitance-voltage (C–V) curves of the CAO charge-trapping memory devices. The C–V curves were first measured by sweeping the gate voltage from +7 V to −7 V and then back to +7 V at a rate of 0.5 V/s, in steps of 0.1 V. A holding time of 120 s was applied before the measurement of C–V, which ensured that the charging and discharging processes in the devices have reached a steady state.[12] As shown in Fig. 3, at an applied voltage of ±7 V the memory window is about 2.43 V, here the memory window in the C–V curve is defined as the difference of the flat band voltages ($\Delta V_{\rm FB}$) between the program and erase states. The density of the trapped charges per unit area ($N_{\rm t}$) can be estimated by using the formula[13,14]

$$N_{\rm t} = \frac{C_{\rm ox}\Delta V_{\rm FB}}{qA}, \tag{1}$$

where $C_{\rm ox}$ is the capacitance of the memory device in the accumulation region; q is the electron charge; A represents the effective area of the Pt electrode, in this case $A = 1.77 \times 10^{-4}\,{\rm cm}^2$. The density of the trapped charges in the CAO charge trapping memory device was determined to be $2.47 \times 10^{12}/{\rm cm}^2$. As the voltage scanning program was set as $+9\,{\rm V} \rightarrow -9\,{\rm V} \rightarrow +9\,{\rm V}$, a larger memory window of 5.39 V was obtained for the CAO charge trapping memory device, the corresponding density of the trapped charged was about $5.48 \times 10^{12}/{\rm cm}^2$. When the applied voltage was increased to ±11 V, a much larger memory window of 9.22 V was observed, and the density of the trapped charges reached $9.37 \times 10^{12}\,{\rm cm}^{-2}$. No saturation tendency in the increase of the density of the trapped charges could be observed.

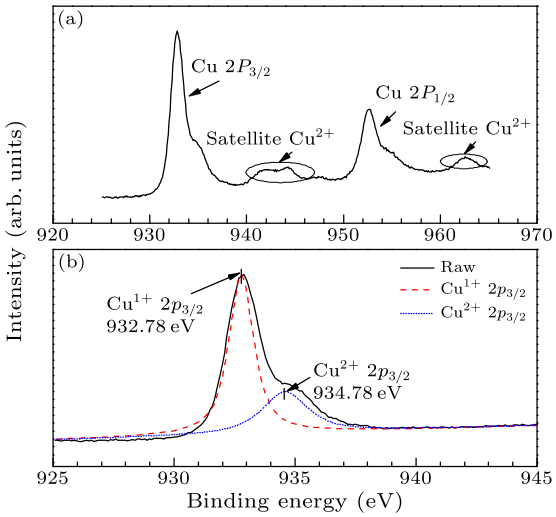

Fig. 4. (a) Cu 2p XPS spectrum of CAO film, (b) the fitted Cu $2p_{3/2}$ XPS peak by resolving Cu $2p_{3/2}$ peak into two individual peaks with a Gaussian function.

In order to investigate the charge-trapping mechanism in CAO memory devices, an additional CAO film with a thickness of 100 nm was also deposited by using the rf-magnetron sputtering technique and thermally treated under the same experimental conditions as that used for the fabrication of CAO charge trapping memory devices. The chemical valences of all atoms contained in CAO film were investigated by using XPS. The XPS binding energy has been calibrated by centering the C 1s spectrum at 284.6 eV. Figure 4(a) shows the Cu 2p XPS spectrum of the CAO film, in which the satellites of Cu $2p_{3/2}$ and Cu $2p_{1/2}$ as the finger print of Cu ions can be observed. It is obvious that as the sub-spectrums of Cu 2p spectra, the

Cu $2p_{3/2}$ peak and the Cu $2p_{1/2}$ peak both contain a shoulder with a weaker intensity in the high energy side, as shown in Fig. 4(a). With a Gaussian function, the Cu $2p_{3/2}$ peak in CAO film was resolved into two individual peaks, i.e., 932.78 eV and 934.78 eV, as shown in Fig. 4(b) by using the dotted lines. The former peak corresponds to the Cu^{1+}–O bond and the latter is related to the Cu^{2+}–O bond. This means that there are two chemical states for Cu atoms in CAO film. An *ab initio* study by Wallin *et al.*[15] showed that some transition-metal (such as Cr and Cu) doping in Al_2O_3 causes additional states in the band-gap of Al_2O_3. The lattice surroundings in Al_2O_3 by the substitution of Al^{3+} with Cu^{1+} may result in the occurrence of Cu^{2+}. Similarly, the trap states due to the inter-diffusion at the interface HfO_2/Al_2O_3 has been investigated by many researchers,[16–18] and the enhancement of the charging-trapping capability due to the inter-diffusion at the interface HfO_2/Al_2O_3 was also observed.[19] On the other hand, the oxidation by the sputtering gas of O_2 may also contribute slightly to the defect states. Thus, it is reasonably suggested that the remarkable charge-trapping capability of CAO film in CAO charge-trapping memory device should be mainly attributed to the defect states formed at the interfaces due to the combination of two oxides, Al_2O_3 and Cu_2O.

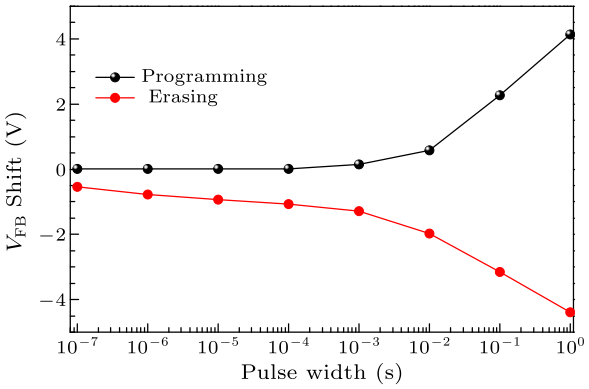

Fig. 5. The P/E characteristics of CAO memory device.

The P/E characteristics of our memory device is shown in Fig. 5, where the applied voltages are the pulsed signals with different pulse widths, and the amplitudes of the pulsed voltage are ±10 V. When the pulse width is shorter than 10^{-3} s, the programming and erasing speeds are low. The P/E speeds increase significantly at an applied voltage with larger pulse width.

To investigate the endurance characteristics of the CAO memory device, the flat-band shift of the device was measured by applying the pulses bias with an amplitude of ±10 V and a pulse width of 10 ms for the P/E operations, as shown in Fig. 6. The P/E memory windows of our device shifted from 7.1 V to 9.23 V after applied 10^5 P/E cycles. This means that about 30% deviation of the memory window was observed for our memory window. The good endurance property of the CAO charge-trapping memory device should be attributed to the good intrinsic stability of Al_2O_3.

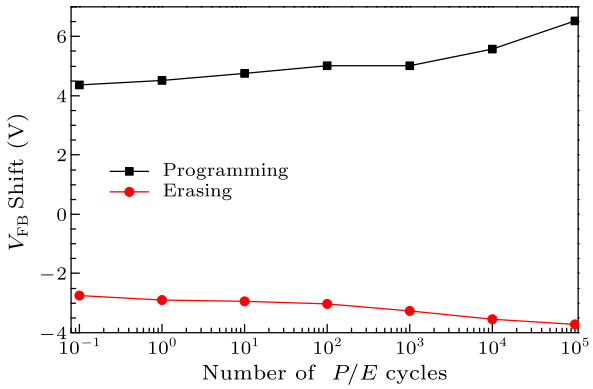

Fig. 6. The endurance characteristics of the CAO memory device.

In conclusion, the $Si/Al_2O_3/Al_2O_3$-$Cu_2O/Al_2O_3/Pt$ memory device has been fabricated. The combination of two high-k oxides in the charge-trapping layer results in a distinguished charge-trapping capability of the memory device. The charge-trapping mechanism is attributed to the defect states formed by the inter-diffusion at the interface of two oxides. With the remarkable charge-trapping efficiency and the simple structure, the charge-trapping memory device with different high-k dielectric composites as the charge-trapping layer should be one of the possible choices for the non-volatile memory devices in the future.

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