# A Silicon Tunnel Field-Effect Transistor with an *In Situ* Doped Single Crystalline Ge Source for Achieving Sub-60 mV/decade Subthreshold Swing *

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*We report the demonstration of an n-channel lateral Si tunnel field-effect transistor (TFET) with a single crystalline Ge source fabricated using the gate-last process. The $p^+$ Ge source was in situ doped and grown at 320°C. An abrupt interface between Ge source and Si channel with type-Ⅱ band alignment and a steep source doping profile (∼1.5 nm/decade) formed the tunneling junction. This allows the realization of a TFET with a steep subthreshold swing of 49 mV/decade at room temperature and an $I_{ON}/I_{OFF}$ ratio of $10^7$.*

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Tunneling field effect transistors (TFETs) can achieve a subthreshold swing $S$ steeper than 60 mV/decade at room temperature, and could be attractive for enabling aggressive supply voltage $V_{DD}$ reduction well into the sub-0.5 V regime.[1−9] The TFET device operation is based on gate-controlled band-to-band tunneling (BTBT), and allows the realization of high ON-state current $I_{ON}$ to OFF-state current $I_{OFF}$ ratio at a low $V_{DD}$. To reduce the effective tunneling barrier for high BTBT rate, semiconductors with narrow energy bandgap $E_G$ like GeSn,[6,8] InGaAs[9] and InAs[10] have been investigated. TFETs made of narrow bandgap materials, however, may suffer from high $I_{OFF}$ due to drain side tunneling. Different materials may be used for the source and channel in a TFET which employs a source-channel heterostructure junction. The BTBT rate in such a TFET also depends on the band alignment of the materials through which the tunneling occurs. Heterostructures with a type-Ⅱ staggered band alignment at the interface have been investigated as a TFET performance booster, which can enhance $I_{ON}$ by using narrow bandgap materials in source region and while $I_{OFF}$ is limited by a large bandgap material in the drain region.[11,12]

In this study, n-channel lateral Si TFETs with single crystalline Ge source using gate-last process were fabricated. A Ge-source/Si-channel tunneling junction with a steep doping profile was formed, as confirmed using a secondary ion mass spectrometry (SIMS). A steep $S$ of 49 mV/decade is achieved.

TFET fabrication was performed on a bulk Si(100) substrate using a gate-last process. The key process steps are shown in Fig. 1. A 400-nm-thick $SiO_2$ layer was thermally grown and patterned using a reverse isolation mask. The $n^+$ drain was formed by a masked arsenic ion ($As^+$) implantation (40 keV and a dose of $1 \times 10^{15}$ cm$^{-2}$) and a 1000℃ 60 s anneal [Fig. 1(a)]. A 60-nm-thick $SiO_2$ layer was deposited and patterned as a mask for a source recess etch using $Cl_2$-based plasma [Fig. 1(b)].

The samples were then cleaned and loaded into an ultra-high vacuum chemical vapor deposition (UHVCVD) apparatus for epitaxial growth of *in situ* boron (B) doped Ge source at 320℃ [Fig. 1(c)]. 4.6 nm of $HfO_2$ gate dielectric and 200 nm of TaN were subsequently deposited and etched in $Cl_2$-based plasma to form the gate stack [Fig. 1(d)]. Due to the low thermal budget of gate stack formation, the growth of the interfacial layer between $HfO_2$ and the Si channel was effectively suppressed and a small equivalent oxide thickness (EOT) of 1.35 nm was obtained.

Figure 2(a) shows the top-view SEM image of the ring-type Ge-source TFET with a gate length of 10 μm and a gate width of 400 μm. The transmission electron microscopy (TEM) image of the tunneling region for the $p^+$ Ge source-Si channel region under the TaN/$HfO_2$ gate stack is depicted in Fig. 2(b). Simulated band diagram near surface along source to channel direction in the TFET is shown in Fig. 2(c).

Figure 3 shows the vertical profiles of B, Ge and Si in the source region. A steep B profile of 1.5 nm/decade is achieved. The hole concentration in the source is about $4 \times 10^{19}$ cm$^{-3}$ which was obtained by Hall measurement on a separate blanket sample. Due to the very low growth temperature of the Ge source, inter-diffusion between Ge and Si and the formation of Ge islands were effectively suppressed. Meanwhile, a single crystalline Ge source having an abrupt Ge/Si interface could be achieved, which can be seen from the TEM image in Fig. 2(b). The steep doping profile and compositionally abrupt interface lead to an abrupt tunneling junction with

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high BTBT rate at the Ge source/Si channel interface.

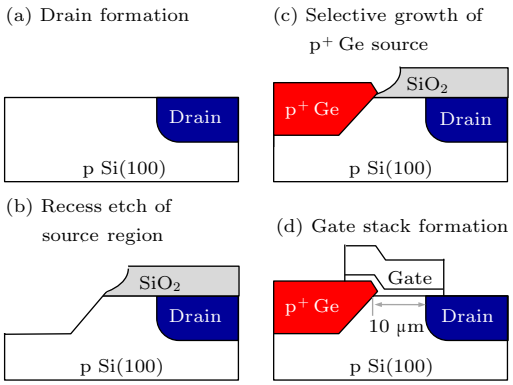


**Fig. 1.** Key process steps for fabricating a TFET with a single crystalline Ge source, including (a) drain implant and anneal, (b) source recess etch, (c) selective epitaxy of *in situ* B-doped Ge source, and (d) gate stack formation.

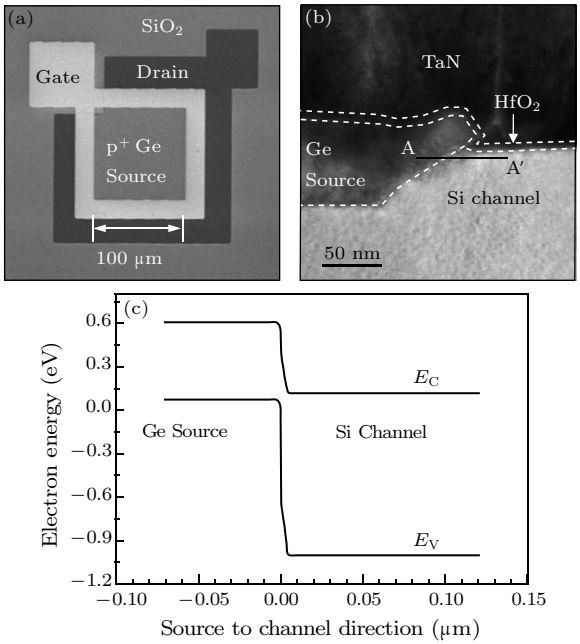


**Fig. 2.** (a) Top-view SEM image of the ring-type Ge-source Si TFET. (b) TEM image of the tunneling region featuring the $p^+$ Ge source-Si channel junction, TaN metal gate, and $HfO_2$ gate dielectric. (c) Simulated band diagram near surface along source to channel direction [denoted by the A–A′ line in Fig. 2(b)] at $V_{GS} = V_{DS} = 0$ V.

Figure 4(a) shows the $I_{DS}$–$V_{GS}$ transfer characteristics of an n-channel lateral Ge-source TFET, and the $I_{DS}$–$V_{DS}$ output characteristics of the same device is depicted in Fig. 4(b). The TFET demonstrates the steep $S$ below 60 mV/decade over 2 orders of $I_{DS}$ magnitude at $V_{DS} = 0.1$ V. This is contributed by the staggered type-Ⅱ band alignment at the abrupt Ge source/Si channel junction. The leakage current at $V_{GS} = 0$ V and $V_{DS} = 1.0$ V is due to the tunneling current of $p/n^+$ Si junction at drain side. We can see that the leakage current at $V_{DS} = 1.0$ V decreases from $V_{GS} = 0$ V to 0.25 V. This is because the tunneling barrier of the $p/n^+$ Si junction at drain side increases with $V_{GS}$.

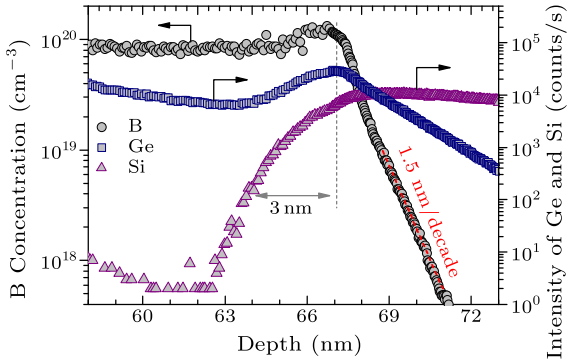


**Fig. 3.** SIMS profiles for B, Ge and Si along the vertical direction in the Ge source region of TFET, showing the steep doping profile.

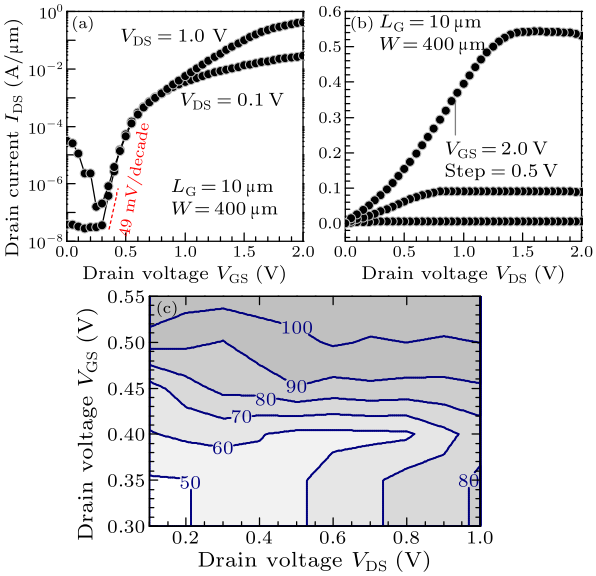


**Fig. 4.** (a) $I_{DS}$–$V_{GS}$ of TFET with single crystalline Ge source, showing a steep subthreshold swing of 49 mV/decade. (b) $I_{DS}$–$V_{DS}$ curves of the same device in (a). (c) Contour lines for $S$ of the TFET obtained at each bias ($V_{GS}$, $V_{DS}$) point at room temperature. Sub-60 mV/decade swing is achieved for $V_{DS}$ ranging from 0.1 V to 0.5 V and for $V_{GS}$ ranging from 0.3 V to 0.4 V.

The value of $S$ was computed at each $V_{GS}$ and $V_{DS}$, as $S$ is generally a function of $V_{GS}$ and $V_{DS}$. Figure 4(c) shows the contour lines for the $S$ obtained from measured data. The smallest $S$ is 49 mV/decade. $S$ below 60 mV/decade is achieved in the $V_{DS}$ range from 0.1 V to 0.5 V and in the $V_{GS}$ range from 0.3 V to 0.4 V. For sub-0.5 V $V_{DD}$ operation, $S$ has to as steep as possible in the bias regime in which $V_{GS}$ and $V_{DS}$ are less than 0.5 V. At higher $V_{DS}$, $S$ degrades due to the increase in $I_{OFF}$. The leakage floor of $I_{DS}$ is below 0.1 pA/μm at $V_{DS} = 0.1$ V and the $I_{ON}/I_{OFF}$ ratio is about $10^7$ at $V_{DS} = 1.0$ V.

From the TEM image of the source region

[Fig. 2(b)], the Ge/Si interface under the gate inclines to the source side. Experiment and simulation have demonstrated that an extended source structure, i.e., the source/channel interface inclining to the channel, would lead to the establishing of more tunneling paths with shorter length, which increases the tunneling current and reduces the $S$.[13,14] Therefore, the $I_{\rm ON}$ and $S$ characteristics of the TFETs can be further enhanced by optimizing the design of the Ge source geometry.

In summary, a steep $S$ of 49 mV/decade and an $I_{\rm ON}/I_{\rm OFF}$ ratio of $10^7$ are achieved in an n-channel lateral TFET with an *in situ* doped Ge source. This is attributed to the steep doping profile and abrupt composition interface at the Ge source/Si channel tunneling junction. Further enhancement in TFET performance may be achieved through optimization of the source geometry.

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