CHIN. PHYS. LETT. Vol. 30, No. 3 (2013) 037303

A High Performance $In_{0.7}Ga_{0.3}As$ MOSFET with an InP Barrier Layer for Radio-Frequency Application *

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(Received 30 September 2012)

We demonstrate a high performance implant-free n-type $In_{0.7}Ga_{0.3}As$ channel MOSFET with a 4-nm InP barrier layer fabricated on a semi-insulating substrate employing a 10-nm Al_2O_3 as gate dielectric. The maximum effective channel mobility is 1862 $cm^2/V{\cdot}s$ extracted by the split C–V method. Devices with 0.8 μm gate length exhibit a peak extrinsic transconductance of 85 mS/mm and a drive current of more than 200 mA/mm. A short-circuit current gain cutoff frequency f_T of 24.5 GHz and a maximum oscillation frequency f_{max} of 54 GHz are achieved for the 0.8 μm gate-length device. The research is helpful to obtain higher performance $In_{0.7}Ga_{0.3}As$ MOSFETs for radio-frequency applications.

PACS: 73.40.Qv, 71.61.Ey, 77.84.Bw DOI: 10.1088/0256-307X/30/3/037303

It is well known that Ⅲ–V compound semiconductors are considered as the most promising candidates to replace mainstream Si-based CMOS technology beyond the 22 nm nodes.[1–6] $In_xGa_{1-x}As$ has been used as a channel material for high-speed electronic devices because of its high electronic mobility.[2] Recently, a high performance $In_xGa_{1-x}As$ NMOSFET with Al_2O_3 deposited by atomic layer deposition (ALD) technology was reported by Xuan *et al.*,[3] molecular beam epitaxy (MBE) reported by Lin *et al.*,[7] InAlP oxide by Xiu *et al.*,[8] HfO_2 with a-Si passivating layer[9] by ALD technology.

Due to the density of interface traps, the effective channel mobility of a surface channel MOSFET is much smaller than the intrinsic materials. The radio-frequency (rf) performance of a surface $In_xGa_{1-x}As$ MOSFET is relatively lower: an inversion channel InGaAs MOSFET with 0.75 μm gate length exhibits an short-circuit current gain cut-off frequency f_T = 7 GHz and an maximum oscillation frequency f_{max} = 10 GHz.[10] An InGaAs-channel MOSFET with 0.8 μm gate length demonstrated f_T = 14 GHz and f_{max} = 40 GHz.[11] However, buried channel MOSFETs with an InP or InP/InAlAs barrier layer and MOSHEMTs show a higher effective channel mobility than surface channel MOSFETs,[12–14] and show a lower gate leakage current than HEMTs.[14,15] There has been no report on the rf performance of buried InGaAs MOSFETs with an InP barrier layer.

In this Letter, we report an implant-free buried $In_{0.7}Ga_{0.3}As$ channel MOSFET using 4 nm InP as a barrier layer and 10 nm Al_2O_3 as gate dielectric. A 0.8 μm gate-length depletion-mode *n*-channel $In_{0.7}Ga_{0.3}As$ MOSFET device with a drain current of 200 mA/mm and with a peak transconductance of 85 mS/mm is obtained. The measured f_T and f_{max} are 24.5 GHz and 54 GHz, respectively. High rf performance is expected due to its high effective channel mobility which peaks at 1862 $cm^2/V{\cdot}s$, exhibiting its promising applications to millimeter-wave integrated circuit designs.

The device structure of the fabricated buried $In_{0.7}Ga_{0.3}As$ channel MOSFET is shown in Fig. 1. The epitaxial wafers were provided by the Institute of Physics, Chinese Academy of Sciences. A 300-nm InAlAs buffer layer, a 10-nm $In_{0.7}Ga_{0.3}As$ channel, a 4-nm InP barrier layer and a 20-nm n-doping 2×10^{19} cm^{-3} $In_{0.53}Ga_{0.47}As$ cap layer were sequentially grown on semi-insulting InP substrates by molecular beam epitaxy (MBE) technology.

In the device fabrication process, the mesa isolation process was carried out by phosphoric acid-base (H_3PO_4:H_2O_2:H_2O = 3:1:50) and hydrochloric acid (HCl:H_2O = 3:1) wet solution, the $In_{0.53}Ga_{0.47}As$ contact layer in the channel region was etched from the InP barrier layer by the H_3PO_4:H_2O_2:H_2O (3:1:50). Then a two-step pre-gate cleaning process was carried out. Firstly, the native oxide was removed by HF, and then excess elemental arsenic was removed by NH_4OH at room temperature for 5 min, finally the InP barrier layer was passivated by conventional $(NH_4)_2S$ solution. After the above processes, the wafer was quickly transferred ex-situ to a Beneq TF300 ALD module, a 10-nm thick Al_2O_3 gate insulator was deposited at a substrate temperature of 300℃, using alternately pulsed chemical precursors of $Al(CH_3)_3$ (the Al precursor) and H_2O (the oxygen precursor) in a carrier N_2 gas flow. After post-deposition annealing at 400℃ for 30 s in a nitrogen ambience, conventional Ni/Au metal was e-beam evaporated, followed by lift-off pro-

*Supported by the National Basic Research Program of China under Grant Nos 2011CBA00605 and 2010CB327501, the National Science & Technology Major Project under Grant No 2011ZX02708-003, One Hundred Talents Program of Chinese Academy of Sciences, and the Scientific Research Foundation for the Returned Overseas Chinese Scholars, the Ministry of Education of China.
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cess to form the gate electrodes. The post metal annealing (PMA) was performed at 300℃ for 30 s in a nitrogen ambience. After selectively etching the gate insulator Al_2O_3 using BOE, the source drain electrodes were formed by electron beam evaporation of Ni/Ge/Au/Ge/Ni/Au metal and patterned by using lift-off processes, followed by a 270℃ annealing for 3 min. The contact resistance R_C was extracted to be 0.15 Ω·mm by the transmission line method, which is much smaller than 1.5 Ω·mm presented in Ref. [3].

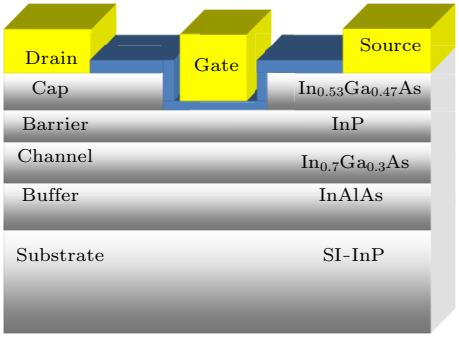

Fig. 1. The schematic cross section of the $In_{0.7}Ga_{0.3}As$ MOSFET with a 4-nm InP barrier layer and 10-nm Al_2O_3.

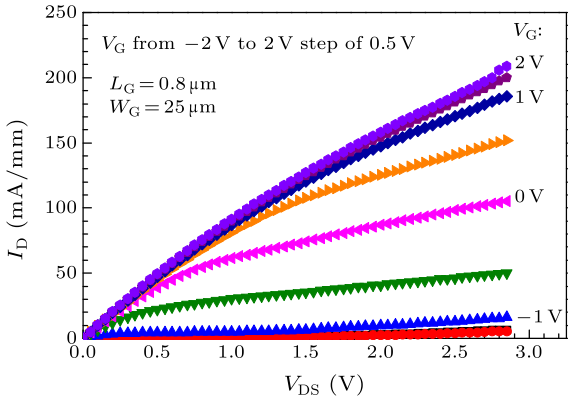

Fig. 2. *I–V* characteristics of the $In_{0.7}Ga_{0.3}As$ MOSFET with 4 nm InP barrier layer and 10 nm Al_2O_3.

Figure 2 shows the *I–V* characteristics for a 0.8-μm gate length MOSFET with a gate bias from −2 to 2 V in steps of 0.5 V. The maximum drain current is 200 mA/mm at $V_G = 2$ V and $V_{DS} = 3$ V. The transfer characteristics and the drain current versus gate voltage of the MOSFET are shown in Fig. 3. A maximum extrinsic transconductance G_{max} of 85 mS/mm was achieved at $V_G = -0.4$ V and $V_{DS} = 3$ V. Although the thick barrier layer (4 nm InP) increases the source and drain resistance, the effective channel mobility for InGaAs MOSFETs with an InP barrier layer is much larger than surface channel MOSFETs.[9] As shown in Fig. 4, the peak effective channel mobility for $In_{0.7}Ga_{0.3}As$ MOSFETs with the InP barrier layer is 1862 cm^2/V·s. The effective channel mobility of $In_{0.7}Ga_{0.3}As$ MOSFET (20 μm gate length) was extracted by using the I_D–V_G characteristics at low V_{DS} of 50 mV and the total inversion charge N_{inv} in the channel. The inset shows the split *C–V* method of measurement on MOSFETs fabricated on the SI substrate. The G_{max} versus C_{OX} and μ_n is the theoretical relation of $G_{max} = Z \cdot C_{OX} \cdot \mu_n (V_G - V_T)^2 / L$, where Z and L are the gate wide and length, C_{OX} is the gate oxide capacity, and μ_n is the effect channel mobility. If the InP barrier layer reduces to 1 nm, The device in this work would show about 5% smaller gate oxide capacity and around 30% larger effective channel mobility than those presented in Ref. [3]. These result in the G_{max} of the device with 1 nm InP barrier layer to be about 24% larger than that presented in Ref. [3].

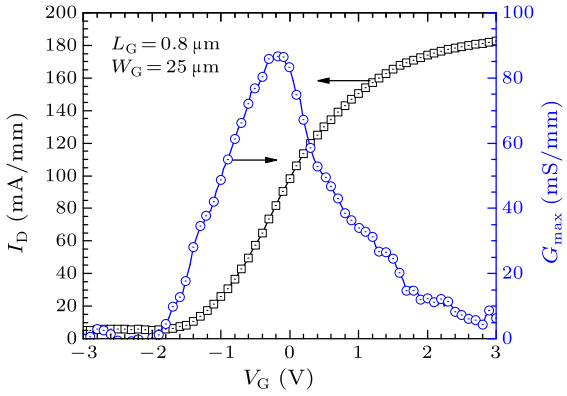

Fig. 3. The drain current and extrinsic transconductance vs gate bias for $In_{0.7}Ga_{0.3}As$ MOSFETs with the 4-nm InP barrier layer and 10-nm Al_2O_3 at $V_{DS} = 3$ V.

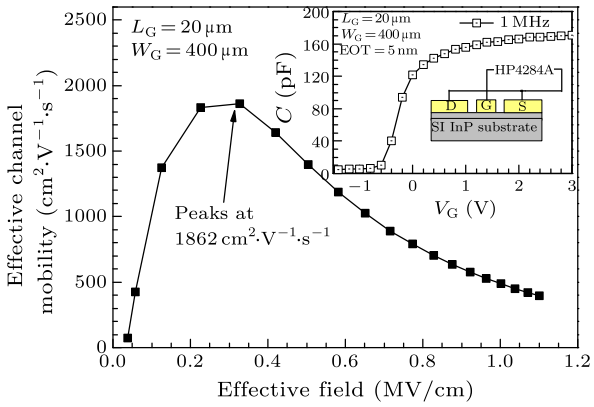

Fig. 4. Effective channel mobility vs effective electric field for $In_{0.7}Ga_{0.3}As$ MOSFETs with the 4-nm InP barrier layer and 10 nm Al_2O_3. The inset shows the split *C–V* characteristics of $In_{0.7}Ga_{0.3}As$ MOSFET at 1 MHz frequency.

Biasing the devices at $V_{DS} = 3$ V and $V_G = 0$ V, the On-wafer *S*-parameters were measured up to 40 GHz for both 25 μm gate width MOSFET and probe pads. The device under test was de-embedded using on-chip open and short pad structures. As shown in Fig. 5, the 0.8-μm gate length device shows $f_T = 24.5$ GHz and $f_{max} = 54$ GHz. These values were obtained by extrapolating the curves of the short circuit current gain H_{21} and the unilateral power gain U_{max}, respectively, using −20 dB/decade slopes.

To further study the characteristics of the

$In_{0.7}Ga_{0.3}As$ MOSFET device, a small-signal equivalent circuit model of a two-finger $In_{0.7}Ga_{0.3}As$ MOSFET is illustrated in Fig. 6. The extrinsic and intrinsic small signal parameters were firstly extracted from the measured S-parameters by using the conventional method,[16] and the error function was defined as the difference between measured and simulated S parameters as follows:

$$|\varepsilon| = \sum_{i,j=1}^{2} \sum_{k=1}^{N_f} \frac{|S_{ij}^{\mathrm{m}}(f_k) - S_{ij}^{\mathrm{s}}(f_k)|}{|S_{ij}^{\mathrm{m}}(f_k)|}, \qquad (1)$$

where N_{f} is the number of measurements at different frequency points, $S_{ij}^{\mathrm{m}}(f_k)$ and $S_{ij}^{\mathrm{s}}(f_k)$ $(i,j=1,2)$ are the measured and simulated S-parameters, respectively.

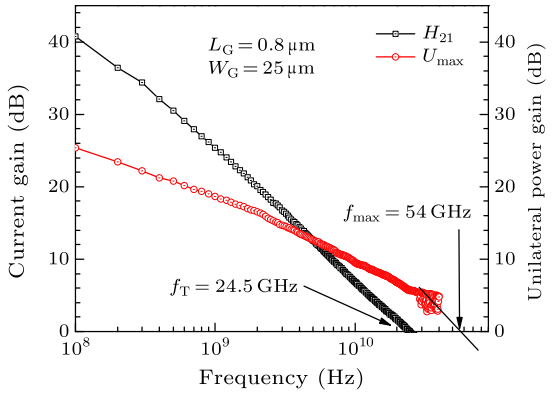

Fig. 5. Short-circuit current gain and unilateral power gain of the gate length of 0.8 μm $In_{0.7}Ga_{0.3}As$ MOSFET.

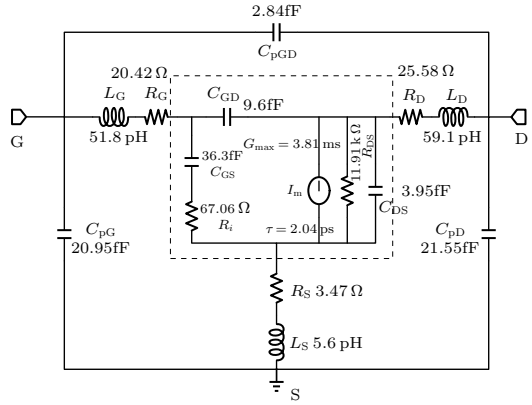

Fig. 6. The small signal equivalent circuit model of the $In_{0.7}Ga_{0.3}As$ MOSFET.

Then all the small signal parameters were achieved by minimizing the error function (see Eq. (1)) using a genetic algorithm optimizer (GA),[17] which could be easily implemented in Agilent's Advanced Design System software. In the parameters, the R_{DS} is much larger but the $G_{\max}$ is much smaller than the HEMT's.[18] The result may be caused by the lower density of channel electrons and the 4-nm-thick intrinsic InP barrier layer. This illustrates that the performance of the device can be enhanced by optimizing the device structure, such as adding bottom δ doping and decreasing the thickness of the InP barrier layer.

In summary, the dc and rf characteristics of an $In_{0.7}Ga_{0.3}As$ channel NMOSFET with a 4-nm-thick InP barrier layer and 10 nm Al_2O_3 gate dielectric have been reported. Due to the effective channel mobility and unpinned Al_2O_3/InP interface, the 0.8 μm gate length device exhibits a maximum transconductance of 85 mS/mm, a drain current of more than 200 mA/mm, f_{T} of 24.5 GHz, and $f_{\max}$ of 54 GHz. The InP barrier layer and gate oxide thickness should be decreased to enhance $In_{0.7}Ga_{0.3}As$ MOSFET dc and rf performance in our future works.

References

[1] Feng Q, Hao Y, Yue Y Z 2008 *Acta Phys. Sin.* **57** 1886 (in Chinese)
[2] Lin T D, Chiu H C, Chang P, Chang Y H, Wu Y D, Hong M and Kwo J 2010 *Solid-State Electron.* **54** 919
[3] Xuan Y, Wu Y Q and Ye P D 2008 *IEEE Electron Device Lett.* **29** 294
[4] Xiang W F, Lu H B, Chen Z H, He M, Lu X B, Liu L F, Guo H Z and Zhou Y L 2005 *Chin. Phys. Lett.* **22** 182
[5] Yang Y, Li G P, Gao Y and Liu J 2009 *Chin. Phys. Lett.* **26** 027801
[6] Mao W, Zhang J C, Xue J S, Hao Y, Ma X H, Wang C, Liu H X, Xu S R, Yang L A, Bi Z W, Liang X Z, Zhang J F and Kuang X W 2010 *Chin. Phys. Lett.* **27** 128501
[7] Lin T D, Chang P, Chiu H C, Hong M, Kwo Y, Lin Y S and Shawn S H 2010 *J. Vac. Sci. Technol.* B **28** C3H14
[8] Xiu X and Patrick F 2010 *CS MANTECH Conference* (Portland, USA 17–20 May 2010) p 207
[9] Ok I, Kim H, Zhang M, Zhu F, Zhao H, Park S, Yum J, Garcia D, Majhi P, Goel N, Tsai W, Gaspe C K, Santos M B and Lee J C 2008 *Appl. Phys. Lett.* **92** 202903
[10] Ren F, Kuo J M, Hong M, Hobson W S, Lothian J R, Lin J, Tsai H S, Mannaerts J P, Kwo J, Chu S N G, Chen Y K and Cho A Y 1998 *IEEE Electron Device Lett.* **19** 309
[11] Passlack M, Zurcher P, Rajagopalan K, Droopad R, Abrokwah J, Tutt M, Park Y B, Johnson E, Hartin O, Zlotnicka A, Fejes P, Hill R J W, Moran D A J, Li X, Zhou H, Macintyre D, Thoms S, Asenov A, Kalna K and Thayne I G 2007 *IEDM Tech. Dig.* P 621
[12] Zhao H, Chen Y T, Yum J H, Wang Y Z, Goel N and Lee J C 2009 *Appl. Phys. Lett.* **94** 193502
[13] Xue F, Jiang A, Zhao H, Chen Y T, Wang Y Z, Zhou F and Lee J 2012 *IEEE Electron Device Lett.* **33** 1255
[14] Lin H C, Yang T, Sharfi H, Kim S K, Xuan Y, Shen T, Mohammadi S and Ye P D 2007 *Appl. Phys. Lett.* **91** 212101
[15] Kazzi M E, Czornomaz L, Rossel C, Rossel C, Gerl C, Caimi D, Siegwart H, Fompeyrine J and Marchiori C 2012 *Appl. Phys. Lett.* **100** 063505
[16] Taking S, MacFlane D and Wasige E 2011 *IEEE Trans. Electron Devices* **58** 1418
[17] Menozzi R, Piazzi A and Contini F 1996 *IEEE Trans. Circuits Syst.* I **43** 839
[18] Matsuzaki H, Maruyama T, Koasugi T, Takahashi H, Tokumitsu M and Enoki T 2007 *IEEE Trans. Electron Devices* **54** 378