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Direct Experimental Evidence of Hole Trapping in Negative Bias Temperature Instability

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Negative bias temperature instability (NBTI) in ultrathin-plasma-nitrided-oxide (PNO) based p-type metal-oxide-semiconductor field effect transistors (pMOSFETs) is investigated at temperatures ranging from 220 K to 470 K. It is found that the threshold voltage V_T degradation below 290 K is dominated by the hole trapping process. Further studies unambiguously show that this process is unnecessarily related to nitrogen but the incorporation of nitrogen in the gate dielectric increases the probability of hole trapping in the NBTI process as it introduces extra trap states located in the upper half of the Si band gap. The possible hole trapping mechanism in NBTI stressed PNO pMOSFETs is suggested by taking account of oxygen and nitrogen related trap centers.

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Negative bias temperature instability (NBTI) is one of the most important reliability research topics in modern CMOS technologies. Although it has been known for forty years, the degradation mechanism is still under debate and is of great interest. The negative bias temperature (NBT) degradation has been largely attributed to two different traps. One is the interface states due to Pb centers, resulting from the dissociation of Si-H bonds.[1,2] The other is the hole traps generated in the gate oxide, such as oxide vacancy related E' centers or nitride-incorporated defects.[3] Recent studies[4–6] suggested that both interface state and hole traps play very important roles in NBTI. The former exhibits a power-law time dependence and a high activation energy, while the latter shows a relative small activation energy and total recovery. In most cases, both contributions are mixed in the NBTI process. It is of great importance to separate them in order to understand their roles and generation mechanisms. Charge pumping (CP) is the one widely used technique to identify the interface trap properties. By comparing CP data with NBTI results, Huard and Denais[3] concluded that a significant fraction of threshold voltage shift is due to the trapped holes. To study the hole trapping mechanism in NBTI, computing techniques are usually used to separate the contribution of hole traps from the interface states based on their different electrical performance, such as temperature and voltage dependence.[3,5,6] In this study, we use the low temperature NBTI measurement technique to assess the hole trapping in the NBTI process. Our experimental results show that the $|\Delta V_T|$ at relative low temperature is dominated by hole trapping process in both SiO_2 and plasma-nitrided-oxide (PNO) based p-type metal-oxide-semiconductor field effect transistors (pMOSFETs), with V_T being the threshold voltage. The incorporation of nitrogen in the gate dielectric induces the extra trap states in energy levels above the Si mid-gap, which induces the stronger hole trapping phenomena in PNO devices than in SiO_2 devices.

PNO pMOSFETs used in this study are fabricated in 65-nm CMOS process technology. The device is in the gate width $W = 10\,\mu m$ and the gate length $L = 0.13\,\mu m$. SiON film thickness is 2.6 nm evaluated by C–V technique.

The measurements are conducted using a Keithley 4200 semiconductor characterization system in a Cascade Summit 12000 probe station with a built-in temperature controller. The temperature of the sample holder can be turned from 220 K to 470 K continuously with an error less than 0.1 K. For V_T degradation measurement, an electrical stress of V_{GS} was first applied on the gate while the source, drain and substrate are grounded. After the stress, I_{DLIN} at $|V_{DS}| = 50\,mV$ was measured by directly switching stress voltage to measure voltage V_{GM} with 50 ms delay in each measurement. The stress induced ΔV_T is calculated with the equation[7]

$$\Delta V_T = \frac{\Delta I_{DLIN}}{I_{DLIN0}} \times (V_{GM} - V_{T0}), \tag{1}$$

where I_{DLIN0} and V_{T0} are pre-stress drain current and threshold voltage, respectively, ΔI_{DLIN} is I_{DLIN} shift after stress. The technique is used to study the V_T shift in both the degradation and recovery phase in

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the NBTI process.

In order to characterize fast $V_{\rm T}$ shifts as a function of recovery bias $V_{\rm GR}$ between the inversion and accumulation state, we independently stress the device for 4600 s, then switch the gate bias from the stress level to $V_{\rm T}$ and remain there for enough long time to guarantee that the time dependent recovery is negligible during the subsequent ramping procedure. After the first recovery, $V_{\rm GR}$ is ramping from inversion state to accumulation state with a stepwise of 0.24 V and $\Delta V_{\rm T}$ is recorded at each $V_{\rm GR}$.

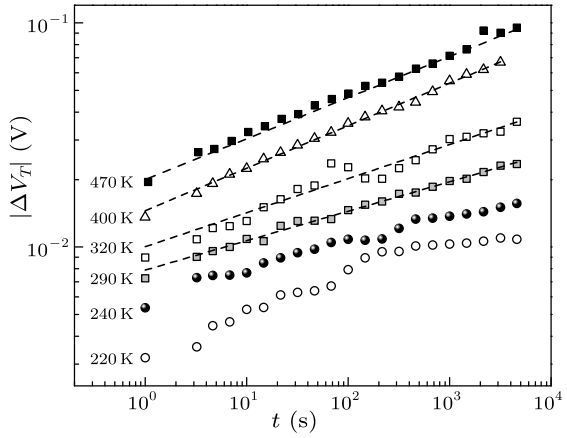

Fig. 1. The time behavior of $|\Delta V_{\rm T}|$ for PNO pMOSFETs under NBTI stress ($V_{GS} = -2$ V) at temperatures ranging from 220 K to 470 K. The dashed line is the power-law fitting line ($\sim t^n$).

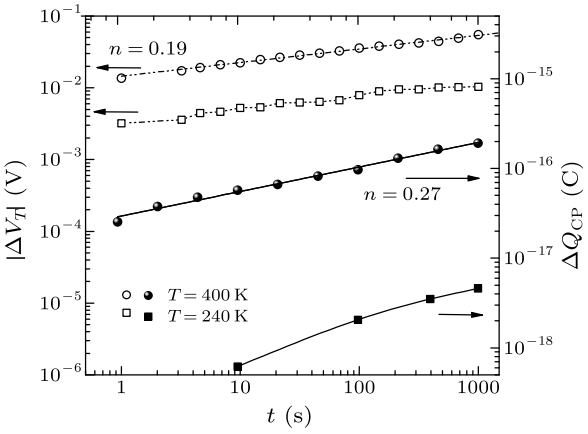

Fig. 2. The time behavior of $|\Delta V_{\rm T}|$ (solid) and interface charges $\Delta Q_{\rm cp}$ (open) for PNO pMOSFETs under NBTI stress ($V_{\rm GS} = -2$ V) at $T = 400$ K and 240 K. The interface charges $\Delta Q_{\rm cp}$ are measured by charge pumping technique, where the frequency is set as 1 MHz and the gate voltage is typically ranged from 1 V$to+$1 V.

Figure 1 shows the time behaviors of $|\Delta V_{\rm T}|$ in PNO devices at temperatures varying from 220 K to 470 K. It could be observed that at a relative high temperature, $|\Delta V_{\rm T}|$ follows power-law time dependence. As shown in Fig. 2, the $|\Delta V_{\rm T}|$ at 400 K exhibits a power law time exponent $n = 0.19$. This value is far smaller than the n value ($\sim$0.27) of the interface charges $\Delta Q_{\rm cp}$'s time dependence measured by charge pumping technique. The difference between the two exponents indicates that other degradation origins could be involved in NBT degradation besides the interface state generation

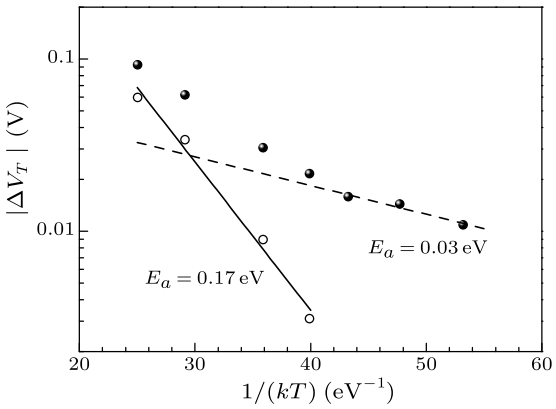

Fig. 3. ΔV_T (at $t = 2154$ s) as a function of $1/kT$. The filled circles are the measured $|\Delta V_{\rm T}|$ and the open circles are the calculated $|\Delta V_{\rm T}|$ at high temperature by subtracting $|\Delta V_{\rm T}|$ extrapolated from low temperature data (dashed line) from high temperature measured $|\Delta V_{\rm T}|$.

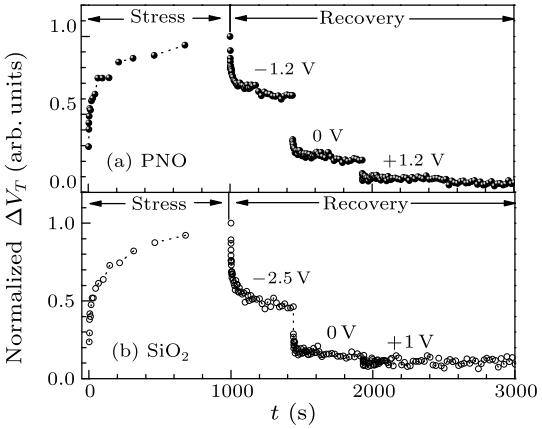

Fig. 4. The time behavior of $|\Delta V_{\rm T}|$ in the stress and the recovery phase at $T = 240$ K in (a) PNO devices. It is stressed at $V_{\rm GS} = -2$ V and recovered at $V_{\rm GR} = -1.2$, 0, $+1.2$ V, respectively; (b) 5.6-nm SiO_2 devices. It is stressed at $V_{\rm GS} = -4$ V and recovered at $V_{\rm GR} = -2.5$, 0, $+1$ V, respectively, in order to achieve similar oxide fields as those applied for PNO devices.

As the temperature falls below 290 K, $V_{\rm T}$ degradation is still significant. For example, at least 10 mV of $V_{\rm T}$ shift occurs at $T = 240$ K at stress time $t = 1000$ s. On the other hand, the generated interface charges decrease dramatically when the temperature changes from 400 K to 240 K. Using $\Delta Q_{\rm cp}/C_{\rm ox}$, here $C_{\rm ox}$ is oxide capacitance measured by C–V technique, the estimated $|\Delta V_{\rm T}|$ due to the interface charges is about 1 mV at 240 K at stress time $t = 1000$ s. This result clearly shows that the large $|\Delta V_{\rm T}|$ at the low temperature is not due to the contribution from the interface

state generation.

To further understand the NBTI process, the activation energy E_a in the whole temperature range has been extracted, as shown in Fig. 3. In the range of 220–270 K, the degradation exhibits weak T dependence with E_a∼0.03 eV. As the stress temperature increases, an additional degradation with large temperature excitation dominates, indicating that there are two mechanisms in NBT degradation. To obtain the high-temperature activation energy, the contribution of small E_a component at high temperatures has been calculated (the dashed line) and subtracted from the measured $|\Delta V_{\rm T}|$ at high temperatures. The corresponding E_a value due to the additional high temperature activation is 0.17 eV. This value is in good agreement with the E_a value (0.16 eV) reported in Ref. [3], which is believed to be associated with the interface Si-H dissociation energy in PNO pMOSFETs.

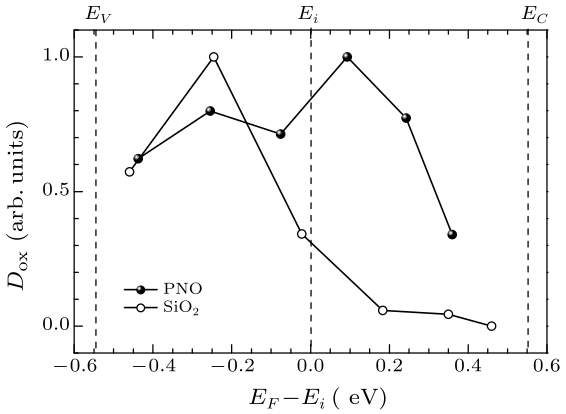

Fig. 5. The normalized density of recoverable oxide trap states in the Si band gap, extracted from the $|\Delta V_T|$ measurements when V_{GR} is ramping from the inversion state to accumulation state. The Fermi level position $E_{\rm F}$ corresponding to V_{GR} is obtained from the C–V measurements.

The degradation with E_a∼0.03 eV occurs in the whole measured temperature range and dominates the low temperature NBTI process. The same results were reported in Ref. [8]. To understand the possible origin of this part, we performed recovery measurements of $|\Delta V_{\rm T}|$ at a low temperature. Figure 4(a) shows the recovery behavior of $|\Delta V_{\rm T}|$ at $T = 240$ K in the PNO device. It is found that the $|\Delta V_{\rm T}|$ recovery progresses with increasing the gate bias, recovered by 38%, 80% and 94% at $V_G = -1.2$, 0, +1.2 V, respectively. Almost fully recovery under positive gate bias indicates that the $V_{\rm T}$ degradation at low temperatures is dominated by the transient hole trapping process. The hole trapping mechanism in NBTI is often suggested that a channel holes tunnel into oxide and are trapped into the oxide traps by elastic or inelastic process. The gradual increase of $|\Delta V_{\rm T}|$ with time at low temperature (in Fig. 4(a)) indicates that hole traps are being continually generated under NBT stress. The presence of temperature activation energy (E_a∼0.03 eV) may be due to the structure relaxation participating in the hole trapping process.[4,9] The similar hole trapping and detrapping behavior is also detected in SiO_2 devices at low temperature (Fig. 4(b)), indicating that the hole trapping is unnecessarily related to nitrogen

It is noteworthy that about 14% charges are detrapped at positive gate voltage in PNO-based devices. Positive bias recovery behavior has been reported in NBTI stressed decoupled-plasma-nitridation (DPN) and rapid-thermal-nitridation (RTN) pMOSFETs.[5] However, as shown in Fig. 4(b), no such positive bias recovery is detected in pure SiO_2 devices at low temperature in spite of the similar charge trapping and detrapping behaviors observed. In order to estimate the energetic profiling of recoverable oxide traps for two devices, we measured $|\Delta V_{\rm T}|$ as a function of recovery gate bias $V_{\rm GR}$ between the inversion and accumulation state. By assuming the location of the recoverable oxide traps close to the gate oxide-substrate interface, the density of recoverable trap states $D_{\rm ox}$ can be calculated by[15]

$$D_{\rm ox}\left(\frac{E_{\rm F}^{i}+E_{\rm F}^{i-1}}{2}\right)=\frac{C_{\rm ox}}{q}\frac{\Delta V_{\rm th}(E_{\rm F}^{i})-\Delta V_{\rm th}(E_{\rm F}^{i}-1)}{E_{\rm F}^{i}+E_{\rm F}^{i-1}}, \tag{2}$$

where $C_{\rm ox}$ is the oxide capacitance and $E_{\rm F}^{i}$ is the Fermi level position at the bias level $V_{\rm GR}^{i}$. Figure 5 shows the normalized density of recoverable oxide trap states in the Si band gap. For SiO_2 devices, we observe one significant peak which locates below the Si mid-gap, while for PNO devices two peaks are observed; one is located below the Si mid-gap which is quite similar to that in Si devices, the other is located in the upper half of the silicon band. This extra trap state could be related to the substantial NBTI enhancement for PNO devices comparing to that for SiO_2 devices.

In SiO_2 devices, trap states E' centers ($O_3 \equiv$Si·) have been identified under the NBT stressing conditions,[11] and the NBTI model with inelastic hole trapping at E' center prosecutors is employed by Grasser *et al.*[4] The substitution of nitrogen on the oxygen site produces large numbers of nitrogen vacancy defects in the device. Campbell *et al.* recently measured NBTI-induced defects in 2.3-nm PNO pMOSFET by using the spin-dependent recombination method and identified that new trap states, K centers, are introduced under NBT stress.[12] K centers are silicon atoms back-bonded to nitrogen atoms ($N_3 \equiv$Si·), generated by capturing a hole in a neutral nitrogen vacancy defect ($N_3 \equiv$Si–Si$\equiv N_3$). Trapping mechanism at K center persecutors is believed to be common with that of E' centers by many authors ac-

cording to their similar structural features.[10,13] The nitrogen related deep level states detected in the recovery in PNO devices are probably associated with these K centers. Both energy levels are near the conduction band of Si substrates.[14] Further study is now ongoing.

In summary, we have experimentally investigated NBTI phenomena in PNO pMOSFETs at temperatures ranging from 220 K to 470 K. The results show that the $V_{\rm T}$ degradation has different activation energies above and below 290 K, indicating the existence of two mechanisms in NBT degradation, one is the generation of classic interface traps, the other is the generation of hole traps. $V_{\rm T}$ degradation below 290 K is dominated by the hole trapping process. The similar trapping and detrapping behaviors are also found in SiO_2 devices, indicating that this hole trapping process is unnecessarily related to nitrogen. However, the incorporation of nitrogen in gate oxides increases the probability of hole trapping in PNO pMOSFETs as it introduces extra trap states in energy levels near conduction band of substrate Si. The possible hole trapping mechanism in NBTI stressed PNO pMOSFETs is suggested by taking into account of oxygen and nitrogen related trap centers.

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