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Low-Voltage Depletion-Mode Indium-Tin-Oxide Thin-Film Transistors Gated by $Ba_{0.4}Sr_{0.6}TiO_3$ Dielectric *

WANG Li-Ping(王丽萍), LU Ai-Xia(陆爱霞), DOU Wei(窦威), WAN Qing(万青)**

[1]*Key Laboratory for Micro-Nano Optoelectronic Devices of Ministry of Education, and State Key Laboratory of Chemo/Biosensing and Chemometrics, Hunan University, Changsha 410082*

[2]*Ningbo Institute of Material Technology and Engineering. Chinese Academy of Sciences, Ningbo 315201*

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We report on the fabrication and characterization of low-voltage indium-tin-oxide (ITO) thin-film transistors (TFTs) gated by $Ba_{0.4}Sr_{0.6}TiO_3$ (BST) gate dielectric deposited at room temperature. The 400-nm-thick BST film shows a low leakage current density of 6×10^{-8} A/cm^2 and a high specific capacitance of 83 nF/cm^2 (corresponding $\varepsilon_r = 37$). The ITO TFTs gated by such BST dielectric operate in a depletion mode with an operation voltage of 5.0 V. The device exhibits a threshold voltage of −3.7 V, a subthreshold swing of 0.5 V/decade, a field effect mobility of 3.2 cm^2/Vs and a current on/off ratio of 1.4×10^4.

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Oxide-based thin-film transistors (TFTs) capable of low-voltage operation have been intensively investigated for their applications in low power consumption electronic devices.[1] Several methods have been proposed for reducing operation voltage: (1) reducing the thickness of the gate dielectrics,[2,3] (2) developing high-k gate dielectrics with low leakage currents,[4−9] Both (1) and (2) can result in large capacitive coupling between gate electrode and channel, and reduce the gate and drain voltage. However, using a very thin gate dielectric is not a suitable approach given that the surface roughness of the substrate may be on the order of the thickness of the insulator leading to a pinhole in the insulator, and high resultant leakage currents.[10] The use of high-k gate insulators is therefore the optimum approach for reducing the operating voltage. A potential candidate for gate insulators is barium strontium titanate (BST).[11] Recently, $InGaZnO_4$ TFT gated by 170-nm-thick amorphous $Ba_{0.5}Sr_{0.5}TiO_3$ ($\varepsilon_r = 28$) with an operation voltage of 3.0 V was reported.[6] However, the BST film of thickness less than 200 nm suffers from relatively high leakage current densities,[10] and further reduction in the leakage current should be required.

Up to now, extensive consideration has been given to the enhancement-mode TFTs, little attention has been paid to the depletion mode devices. In fact, depletion-mode TFTs are widely used as load elements in accumulation-depletion logic circuits.[12] Lee *et al.*[13] and Huang *et al.*[14] fabricated unipolar inverters, composed of two organic field-effective transistors (OFETs), using an enhancement-mode driver and a depletion-mode load to implement full-swing organic logic circuits. A depletion-mode inorganic oxide semiconductor TFT can be achieved by using a conductive indium tin oxide (ITO) channel[15] since current can flows from the source to the drain at zero gate voltage. Figure 1 shows a schematic picture of the ITO-based TFTs operating in depletion mode. Figure 1(a) displays the normal ON state, showing the conduction channel at zero bias. By applying a negative bias to the gate electrode, a depletion region is formed. Figure 1(b) indicates the formation of the depletion region throughout the whole thickness near the source. Then, the drain current drops significantly, and thus, the TFT becomes OFF-state.[16] In this Letter, low-voltage depletion-mode ITO TFTs gated by high-k amorphous $Ba_{0.4}Sr_{0.6}TiO_3$ gate dielectric are reported. The threshold voltage, field effect mobility, current on/off ratio and subthreshold swing are estimated to be −3.7 V, 3.2 cm^2/Vs, 1.4×10^4 and 0.5 V/decade, respectively.

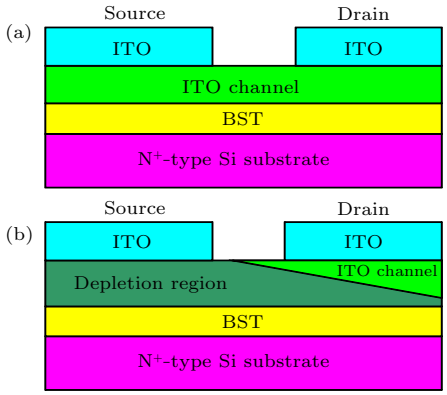

Fig. 1. Schematic picture of an ITO-based TFT with depletion mode: (a) the normal ON state when applied voltage is 0 V, and (b) the OFF state when a negative gate voltage is applied.

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**To whom correspondence should be addressed. Email: wanqing7686@hotmail.com

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ITO-based TFTs were fabricated on n^+-type (100) Si substrates with bottom-gate and top-contact source/drain electrodes. First, the BST film with a thickness of 400 nm was deposited by rf magnetron sputtering at room temperature using a $Ba_{0.4}Sr_{0.6}TiO_3$ ceramic (Ba : Sr = 4 : 6) as the sputtering target. The sputtering power, pressure and Ar/O_2 ratio are 100 W, 0.5 Pa and 2/10 SCCM (SCCM denotes cubic centimeters per minute at STP), respectively. Next, a 50-nm-thick ITO channel layer was deposited on the BST dielectric by rf magnetron sputtering in Ar/O_2 mixed ambient at 0.5 Pa. Then, highly conductive ITO source and drain electrodes with a thickness of 100 nm were deposited by dc magnetron sputtering and patterned using nickel shadow masks in pure argon ambient at 1.0 Pa. The channel length and width of the TFTs were 80 μm and 1000 μm, respectively. The entire process of device fabrication was performed at room temperature. The structural characterizations of the BST film were performed by x-ray diffraction (XRD) and field emission scanning electron microscopy (SEM, Hitachi 4800). The electrical characterizations of the BST film and ITO-based TFT were measured by a Keithley 4200 semiconductor parameter analyzer.

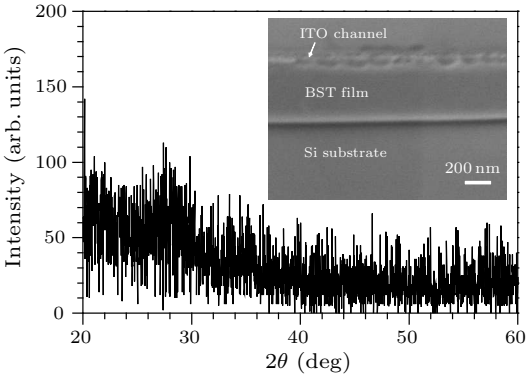

Fig. 2. The x-ray diffraction (XRD) pattern of the 400-nm-thick BST film deposited at room temperature. Inset: a cross-sectional SEM image of the BST and ITO channel layer.

Figure 2 shows the XRD pattern of the BST film, and no diffraction peak is observed, indicating the amorphous nature of the BST film deposited at room temperature. The insert in Fig. 2 shows a cross-sectional SEM image of the ITO/BST film deposited on a Si substrate at room temperature. The BST dielectric layer and the ITO active layer form a regular compact arrangement, with thicknesses of around 400 nm and 50 nm, respectively.

Figure 3 shows the leakage current curve of the BST film deposited at room temperature as a function of applied bias voltage. The leakage current density is estimated to be about 6×10^{-8} A/cm^2 at −5 V, which is much smaller than that of the BST film reported in Refs. [6,10] ($\sim 10^{-5}$ A/cm^2 at 5.0 V). It remains on the order of 1×10^{-8} A/cm^2 in the positive bias voltage, indicating that the leakage current is sufficiently small even in the ON region of the depletion TFT, which ensures that the field-effect device performance will not be affected by the gate leakage. The inset in Fig. 3 shows the capacitance-voltage ($C-V$) characteristics of the n^+ Si/BST (400 nm)/ITO channel/ITO electrode structure. The maximum specific capacitance of the BST film is 83 nF/cm^2 and the dielectric constant of the BST dielectric is estimated to be about 37. A clockwise hysteresis is observed in the $C-V$ curves. We can calculate the magnitude of the trapped charge density from the hysteresis window (about 1.3 V) using the relation

$$N_t \sim [\sim C_i(\Delta V_G)/e]\,. \tag{1}$$

The calculated value of trap density $N_t \sim 7.7 \times 10^{11}$ cm^{-2}, which indicates that the BST/ITO interface has a relatively low trap density.[17]

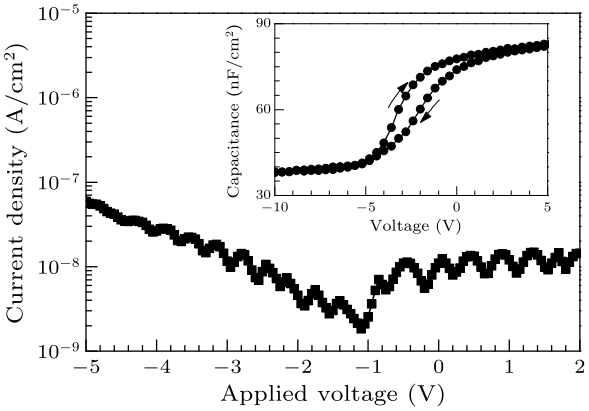

Fig. 3. The leakage current density of the BST film deposited at room temperature as a function of applied bias voltage. Inset: the capacitance-voltage characteristics measured in the n^+-Si/BST (400 nm)/ITO channel/ITO electrode structure.

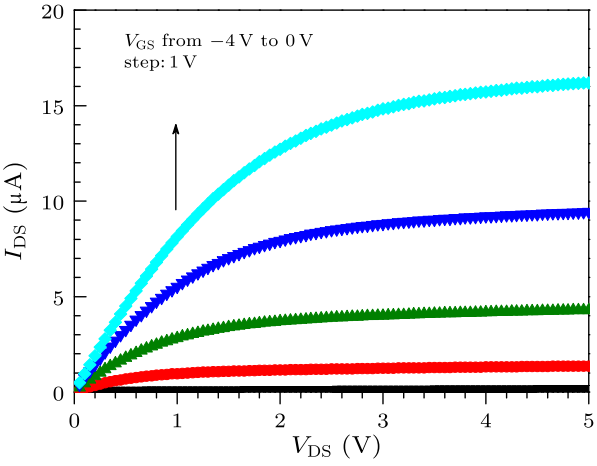

Fig. 4. Output characteristics of ITO TFT gated by BST gate dielectric. V_{DS} is swept from 0 to 5.0 V at each V_{GS} varied from −4.0 to 0 V in steps of 1 V.

Figure 4 illustrates the output characteristics ($I_{DS} - V_{DS}$ curves at V_{GS} from −4.0 to 0 V) for the

ITO TFT gated by BST gate dielectric, and the operation voltage is reduced to 5.0 V. As shown in Fig. 4, the TFT exhibited excellent saturation and pinch-off characteristics, indicating that the entire channel region under the gate bias can be depleted of electrons. Moreover, drain current I_{DS} increases quickly as the gate voltage V_{GS} continuously increases from −4.0 V to 0 V. The output curves display good Ohm contacts, and a saturation current of 16 μA at the bias condition $V_{GS} = 0$ V and $V_{DS} = 5.0$ V.

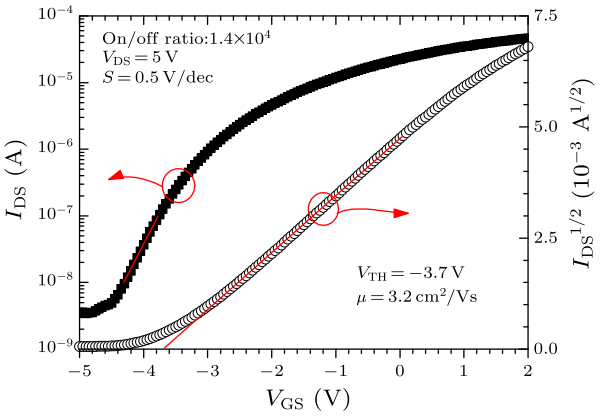

Fig. 5. Transfer characteristics (drain-to-source current I_{DS} vs gate voltage V_{GS} and square root of I_{DS} vs V_{GS} at $V_{DS} = 5.0$ V) of the same ITO TFT gated by BST gate dielectric.

The corresponding transfer characteristics of $\log(I_{DS}) - V_{GS}$ and $\sqrt{I_{DS}} - V_{DS}$ for $V_{DS} = 5.0$ V are shown in Fig. 5. The curves indicate a low off state current of 3.4×10^{-9} A, and a drain current on/off ratio of 1.4×10^4 is calculated from the drain current at the maximum and minimum. The subthreshold gate voltage swing S is given by the relation

$$S = dV_{GS}/d\left(\log|I_{DS}|\right), \tag{2}$$

where S is determined to be 0.5 V/decade. From S we can infer the maximum density of surface states at the semiconductor/dielectric interface via the equation

$$N_{max}^{S} = \left[\frac{S\log e}{kT/q}\right]\frac{C_i}{q}, \tag{3}$$

where $N_{max}^{S} = 3.8 \times 10^{12}\,\mathrm{cm}^{-2}$ is obtained for the insulator/ITO interface. The threshold voltage V_{TH} is calculated from the x-axis intercept of the $\sqrt{I_{DS}} - V_{GS}$ plot. The field-effect mobility μ_{FE} can be calculated from the equation

$$I_{DS} = \frac{WC_i\mu_{FE}}{2L}\left(V_{GS} - V_{TH}\right)^2, \tag{4}$$

where L is the channel length, W is the channel width, C_i is the capacitance density, V_{TH} is the threshold voltage. The extracted V_{TH} and μ_{FE} are −3.7 V and 3.2 cm^2/Vs.

In conclusion, a 400 nm-thick BST film deposited at room temperature shows a small leakage current of 6×10^{-8} A/cm^2 at a bias voltage of −5.0 V, and a large relative permittivity of 37. ITO-based TFTs with depletion mode exhibit a low operation voltage of 5.0 V. The field-effect mobility, on/off-current ratio, threshold voltage, and subthreshold swing are estimated to be 3.2 cm^2/Vs, 1.4×10^4, −3.7 V and 0.5 V/decade, respectively. Given that the entire processing of the TFTs is at room temperature, such TFTs have the advantage of compatibility with flexible polymeric substrates or paper substrates.

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