CHIN. PHYS. LETT. Vol. 27, No. 1 (2010) 018503

Nonvolatile Memory Effect in Organic Thin-Film Transistor Based on Aluminum Nanoparticle Floating Gate *

WANG Wei(王伟)[1,2,3], MA Dong-Ge(马东阁)[1**]

[1]*State Key Laboratory of Polymer Physics and Chemistry, Changchun Institute of Applied Chemistry, Chinese Academy of Sciences, Changchun 130022*

[2]*State Key Laboratory of Integrated Optoelectronics, College of Electronic Science and Engineering, Jilin University, Changchun 130012*

[3]*Graduate School of Chinese Academy of Sciences, Beijing 100049*

(Received 17 August 2009)

A nonvolatile memory effect was observed in an organic thin-film transistor by introducing a floating gate structure. The floating gate was composed of an Al film in a thickness of nanometers, which was thermally deposited on a SiO_2 insulator and exposed to air to spontaneously oxidize. It can be seen that the transistors exhibit significant hysteresis behaviors and storage circles in current-voltage characteristics in the dark and under illumination, indicating that the transistors may act as a nonvolatile memory element. The operational mechanism is discussed in the cases of dark and illumination via charge trapping by the Al floating gate.

PACS: 85.30.Tv, 72.80.Le, 85.25.Hv DOI: 10.1088/0256-307X/27/1/018503

In the past two decades, organic electronics have attracted considerable attention due to their flexibility, low cost and large area process for potential applications: flat-panel displays,[1] logical circuit,[2] solar cells,[3] sensors.[4] Recently, much attention is paid to organic memory devices[5−17] for applications like organic circuits in a radio-frequency identification tag or a smart card. One interesting option is to make a memory cell based on an organic thin-film transistor (OTFT) due to its non-destructive readout and single-transistor application.[18] Up to now, several methods have been used to fabricate OTFT memory devices. One way is to use ferroelectric materials, such as $PbZrTiO_3$,[8] poly (vinylidenefluoridetrifluoroethylene) (PVDF/TrFE),[9−13] nylon poly (m-xylylene adipamide) (MXD6),[14] or electret polyvinyl alcohol (PVA),[15] as the gate insulating layer. The direction of the polarization of the gate dielectric layer modulates the channel conductance, resulting in the memory characteristics of the OFTFs. Another way to make a TFT memory is by using a floating gate structure, where a floating gate is generally introduced into the gate dielectric. This approach has seen dramatic progresses in the field of silicon-based nonvolatile memory. However, the attempt of the floating gate TFT memory based on organic semiconductors is rarely reported.[16,17]

In this Letter, we report an OTFT-based memory device with the floating gate structure. The floated gate is formed by oxide a thin Al film in air. Clearly, a remarkable hysteresis loop can be observed in the drain-source current I_{DS} via drain-source voltage V_{DS} characteristics when sweeping the gate-source voltage V_{GS} between +80 V to −80 V, and there exists a clear difference in the characteristics in dark and under illumination.

A heavily doped n-type silicon (n^+-Si) with a 900 nm thermally growth SiO_2 as the gate insulator was used as the substrate and gate. After routine cleaned, the substrates were put into the vacuum chamber. A 3-nm-thick Al film was first thermally evaporated onto the surface of SiO_2 at a rate of about 0.6 Å/s under a pressure of 10^{-4} Pa. Next, the substrate was exposed to the cleaned dry air at room temperature for two minutes. Then the Al thin film was partially oxidized and finally many separated nanoparticle islands are formed, which could act as the floating gate. After exposed in air, the substrates were put in the vacuum chamber again. With the vacuum pressure of 10^{-4} Pa, a 30-nm-thick pentacene film was thermally deposited acting as the active layer at a rate of about 0.5 Å/s, and a 10 nm molybdenum oxidation (MoO_3) and 100 nm Al as source-drain electrode were deposited by a shadow mask to finish the device. The utilization of MoO_3 may improve the injection of holes.[19] The result channel width W and length L are 2000 μm and 30 μm, respectively. During the deposition, the substrates were held at room temperature. A cross-section schematic diagram of the result devices is shown in the inset of Fig. 1(a). The electrical characteristics of the devices were measured using two Keithley 2400 source-measure units in the dark or

*Supported by the Hundred-Talents Program of Chinese Academy of Sciences, the National Natural Science Foundation of China (50573075 and 60707015), the National Science Fund for Distinguished Young Scholars of China (50325312), and Science Fund for Creative Research Groups of the National Natural Science Foundation of China (20621401), and the Youth Scientific Research Foundation of Jilin Province (20080173).

**Email: mdg1014@ciac.jl.cn

© 2010 Chinese Physical Society and IOP Publishing Ltd

under illumination at room temperature within ambient air. The used light source is a fluorescent lamp with major spectral peaks in the 400–700 nm range and with an intensity of 1.8 mW/cm^2.

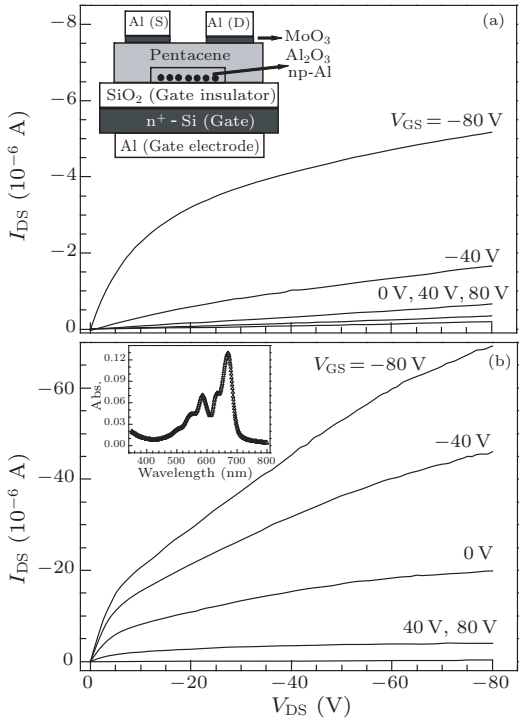


Fig. 1. Output characteristic curves of present transistor in dark (a) and under illumination (b). The inset in (a) shows the cross section schematic diagram of present transistor, and the inset in (b) presents the spectral response curve of the 30-nm-thick pentacene film.

Figure 1(a) shows the output characteristic I_{DS}–V_{DS} of a typical transistor in dark. The device features a p-channel field effect transistor. Furthermore, a clear hole accumulation mode and a slight hole depletion mode features can be observed, which means that some holes can accumulate in the channel at $V_{GS} = 0$ V. This hole depletion mode should be related to the memory effect of the transistor. When the device was illuminated by the fluorescent lamp, it is found that the operation current ($I_{DS,\,illumination}$) shows a large increase compared with that ($I_{DS,\,dark}$) in dark, and the feature of hole depletion mode becomes more notable (as shown in Fig. 1(b)). The inset of Fig. 1(b) shows the spectral response curve of the pentacene film, in which two main absorb peaks are observed at 585 nm and 670 nm, respectively. Obviously, under illumination, the energy of some photons is absorbed by pentacene and electrons-holes (e-h) pairs are generated in the channel, which should be attributed to the additional current in the role of the electrical field.

Figures 2(a) and 2(b) show the transfer characteristic I_{DS}– V_{GS} of the result transistor in dark and under illumination, respectively. It is clearly seen that significant hysteresis loops, in clockwise direction, are observed when cycling V_{GS} is applied. Except for the first time sweeping, the hysteresis loops have a good repeatability. The memory ratio is defined as the ratio of I_{DS} in different sweeping directions at the same V_{GS}. The largest values of memory ratio, 2.1 (in dark) and 11 (under illumination), can be obtained at $V_{GS} \sim -55$ V and +25 V, respectively, in the case of constant $V_{DS} = -10$ V. For the sweeping forward or backward, different threshold voltages V_T can be extracted, which can be defined as the reading state "0" or "1", respectively. The high negative (−80 V) or positive (80 V) V_{GS} can be defined as the programming/erasing (P/E) voltage. The memory window voltages, defined as the difference of V_T in both sweeping directions, with the value of 18 V for in dark and 58 V under illumination, respectively, can be obtained. It is clearly seen that the magnitude of $I_{DS,\,illumination}/I_{DS,\,dark}$ depends not only on the V_{GS} value, but also on the sweeping direction of V_{GS}, as shown in the inset of Fig. 2(b). The ratio value reaches the maximum value of 102 at $V_{GS} = -3$ V in forward sweeping. The increase of I_{DS} under illumination should be related to photo-induced hole accumulation at electric field.

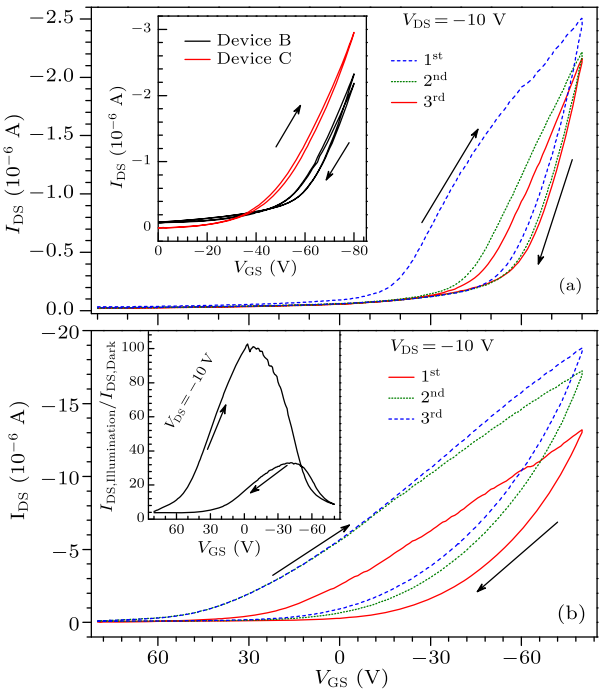


Fig. 2. Transfer characteristic I_{DS}–V_{GS} in linear regime ($V_{DS} = -10$ V) measured in dark (a) and under illumination (b). The inset in (a) shows the transfer characteristics in linear regime of devices B and C. The inset in (b) shows the magnification of $I_{DS,\,illumination}/I_{DS,\,dark}$ as a function of V_{GS}.

Figure 3 shows typical storage cycles of present device at $V_{DS} = -10$ V in dark and illumination. The P/E voltages are chosen to be $V_{GS} = -80$ V and 80 V, respectively. The reading state of the memory

for 0/1 can also be carried out by monitoring I_{DS} at $V_{GS} = -50$ V (in dark) or $V_{GS} = 0$ V (under illumination). High I_{DS} denotes the 0 state of the memory unit and low I_{DS} denotes the 1 state of the memory unit. It can be seen that the present OTFT shows better storage performance. The memory properties can be yet kept after 100 cycles. The data retention time of present transistor memory devices in dark and under illumination is illustrated in Fig. 4. The 0/1 state is obtained by P/E voltages of -80 V and 80 V for 20 s, respectively. In the measurement of I_{DS} versus time, the reading voltage is fixed to be -50 V and 0 V in dark and under illumination, respectively, with $V_{DS} = -10$ V. The data retention time, with I_0/I_1 droping to 50% of its initial value, is about 200 s for the average result of dozen same devices, which can be compared with Ref. [16].

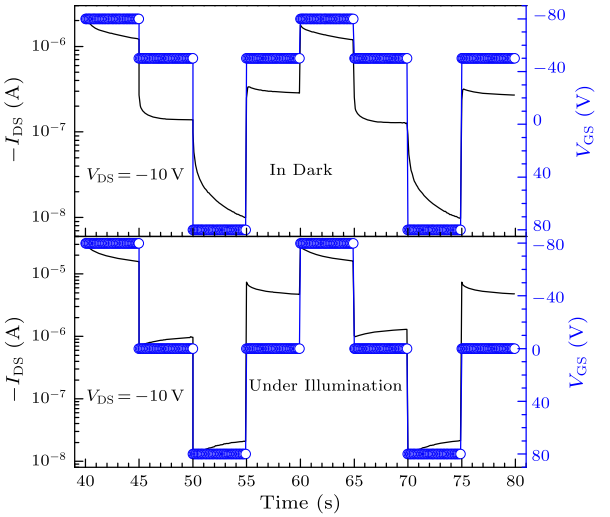


Fig. 3. Two typical storage cycles at $V_{DS} = -10$ V, with $V_{GS} = -80$ V/80 V for programming/erasing, and $V_{GS} = -50$ V or 0 V for reading with the memory operated in dark or under illumination, respectively.

One possible explanation is the repeatable hysteresis and memory properties should be attributed to the utilization of the Al nanoparticle islands acting as the floating gate in dielectric. To demonstrate the role of Al nanoparticle islands, different thickness Al thin films are thermally grown as the floating gate. When the Al film is thicker than 3 nm, the hysteresis phenomenon of device transfer characteristics is more prominent, only with a slight decrease of I_{DS}. When the Al film is thinner than 2 nm (such as device B), the hysteresis is small, which indicates that the oxidation depth of the Al film is about 2 nm. For the reference structure transistors (device C) without any floating gate, only 900 nm SiO_2 acting as insulator, the hysteresis is near neglected. The transfer characteristics of devices B and C are shown in the inset of Fig. 2(a). The small hysteresis loops should be originated from the partial traps at inorganic/organic interface.

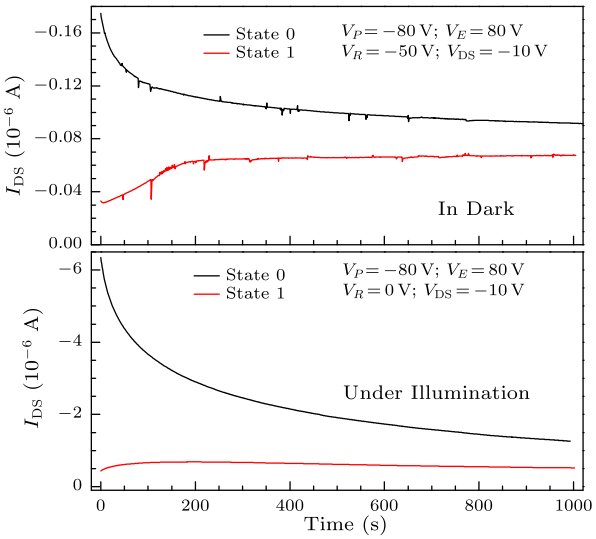


Fig. 4. Data retention of the present transistor memory device in dark (a) and under illumination (b).

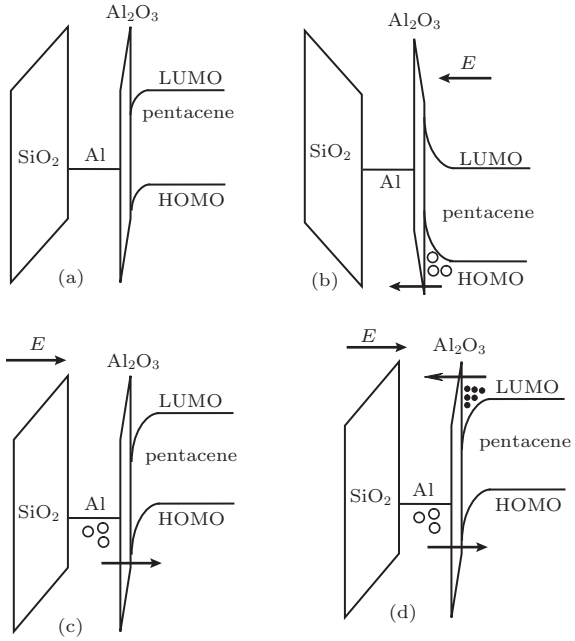


Fig. 5. Energy level diagrams of $SiO_2/Al/Al_2O_3$/pentacene without supplying V_{GS} (a), with supplying high negative V_{GS} in dark (b), with supplying high positive V_{GS} (c) in dark, and with supplying high positive V_{GS} under illumination (d).

Actually, the Al nanoparticle islands as floating gate can act as the charge capture centre. The hysterisis processes can be well explained by energy level diagrams. Figure 5(a) shows the energy level diagrams of $SiO_2/Al/Al_2O_3$/pentacene without supplying V_{GS}. The work function of Al is 4.2 eV. The lowest unoccupied molecular orbital (LUMO) and the highest occupied molecular orbitals (HOMO) of pentacene are 3.2 eV and 5.0 eV, respectively. The barrier heights for electron and hole are 1.0 eV and 0.8 eV, respectively. For the case of p-type semiconductor pentacene, as contacting with Al, the band of

pentacene bends downward as indicated in Fig. 5(a). The schematic energy-band structure variations corresponding to P/E processes in dark and under illumination are shown in Figs. 5(b), 5(c) and 5(d). Here a qualitative explanation is given to illustrate the P/E processes. As we know, the pentacene is p-type semiconductor, and then no electron can accumulate in the channel in dark. In the case of dark, as V_{GS} sweeps in both directions, the hysteresis loops are in the negative V_{GS} region, demonstrating that only holes play role in the storage operation. Before V_{GS} is applied, the Al nanoparticle island floating gate should be neutral. When a large positive V_{GS} is initially applied, the holes in Al nanoparticle islands diffused from the channel can be ejected back. In this case, it needs a small negative V_{GS} to turn the transistor on, and then the first sweeping I_{DS}–V_{GS} curve in forward (e.g. V_{GS} swept from 80 V to −80 V) locates in left. When a large negative V_{GS} is applied, the energy band of pentacene greatly bends upward, the holes may be injected to the Al nanoparticles floating gate from the channel by direct tunneling process and captured in the Al nanoparticle islands, as shown in Fig. 5(b), then the programming is performed. The captured holes generate an internal electric field E_i along the direction opposite to the applied V_{GS} and this E_i weakens the external applied electric field E_{GS} effects. Thus the I_{DS} swept backward is smaller than that swept forward at the same V_{GS}, and a more negative V_{GS} is needed to turn the device on; that is, a right shift of V_T occurs. When a high positive V_{GS} is applied again, that is, the 2nd I_{DS}–V_{GS} curve forward sweeping, the orbital energy level bends downward and the holes stored in the Al nanoparticles have chances to be ejected back into the pentacene channel by tunneling, as shown in Fig. 5(c). The erasing process is performed. However, there exists an additional FN tunnelling for holes through the space charge region at the pentacene surface near to Al_2O_3. As a result, the holes stored in the floating gate will be partly ejected into the channel, and others will remain in the floating gate. Affected by the E_i induced by these remained holes, the 2nd I_{DS}–V_{GS} curve swept forward shifts to left although it cannot return to the initial position. When the V_{GS} sweeps backward again, the I_{DS}–V_{GS} curve shifts to right. Thus a P/E cycle is performed as memory in dark. When illuminated, the electron-hole pairs generate in the channel. At a positive supplied V_{GS}, the orbital energy level bends downwards, as shown in Fig. 5(d). The photo-induced electrons have chances of being injected from the channel into the floating gate through the direct tunneling process. After combined with the remained holes, the redundant electrons are captured in the Al nanoparticles, and an E_i is generated, further weakening the external applied electric field effects. Taking into account the photo-induced holes, the transistor can turn on at a positive V_{GS}. Similarly, when a large negative V_{GS} is supplied, the stored electron have chances of being ejected from the floating gate into the channel through the FN tunneling process, and more holes are injected into the floating gate through the direct tunneling process. After combined with the stored electron, the redundant holes are captured in the Al nanoparticles, thus generating an E_i, also weakening the external applied electric field effects. Taking into account the photo-induced holes, the I_{DS}–V_{GS} curve shifts right remarkably, but be more left than that in dark. Thus a P/E cycle is performed under illumination.

In conclusion, a nonvolatile organic thin-film transistor memory has been demonstrated by introducing Al nanopartiles as a floating gate. The significant hysteresis behaviors and storage circles can be obtained in the dark and under illumination, respectively. It is hopeful that the memory ratio and the data retention time can be improved by optimizing the floating gate Al nanoparticle density and the interface of alumina/pentacene.

References

[1] Huitema H E A, Gelinck G H and Vander Puten J B P H 2001 *Nature* **414** 599
[2] Crone B, Dodabalapur A et al 2000 *Nature* **403** 521
[3] Bach U, Lupo D et al 1998 *Nature* **395** 583
[4] Zhu Z, Mason J T et al 2002 *Appl. Phys. Lett.* **81** 4643
[5] Ma L P, Liu J and Yang Y 2002 *Appl. Phys. Lett.* **80** 2997
[6] Bozano L D et al 2004 *Appl. Phys. Lett.* **84** 607
[7] Ouyang J Y, Chu C W, Szmanda C R and Yang Y 2004 *Nature Mater.* **3** 918
[8] Velu G, Legrand C, Tharaud O, Chapoton A, Remiens D and Horowitz G 2001 *Appl. Phys. Lett.* **79** 659
[9] Unni K N N, Bettignies R, Dabos-Seignon S and Nunzi J M 2004 *Appl. Phys. Lett.* **85** 1823
[10] Naber R C G, Tanase C et al 2004 *Nature Mater.* **4** 243
[11] Unni K N N, de Bettignies R, Dabos-Seignon S and Nunzi J M 2005 *Mater. Lett.* **59** 1165
[12] Naber R C G, de Boer B, Blom P W M and de Leeuw D M 2005 *Appl. Phys. Lett.* **87** 203509
[13] Yildirim F A, Ucurum C, Schliewe R R, Bauhofer W, Meixner R M, Goebel H and Krautschneider W 2004 *Appl. Phys. Lett.* **90** 083501
[14] Schroeder R, Majewski L A and Grell M 2004 *Adv. Mater.* **16** 633
[15] Singh Th B, Marjanovic N, Matt G J, Sariciffci N S, Schwodiauer R and Bauer S 2004 *Appl. Phys. Lett.* **85** 5409
[16] Liu Z, Xue F, Su Y, Lvov Y M and Varahramyan K 2006 *IEEE Trans. Nanotechnol.* **5** 379
[17] Zhen L, Guan W, Shang L, Liu M and Liu G 2008 *J. Phys. D: Appl. Phys.* **41** 135111
[18] Auciello O, Scott J F and Ramesh R 1998 *Phys. Today* **51** 22
[19] Chu C, Li S, Chen C, Shrotriya V and Yang Y 2005 *Appl. Phys. Lett.* **87** 193508