Characteristics Analysis of Vertical Double Gate Strained Channel Heterostructure Metal-Oxide-Semiconductor-Field-Effect-Transistor *

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(Received 10 September 2008)

Since device feature size shrinks continuously, there appears various short-channel effects on the fabrication and performance of devices and integrated circuits. We present a vertical double gate (VDG) strained channel heterostructure metal-oxide-semiconductor-field-effect-transistor (MOSFET). The electrical characteristics of the device with the effective gate length scaled down to 60nm are simulated. The results show that the drive current and transconductance are improved by 57.92% and 54.53% respectively, and grid swing is decreased by 36.83% over their unstrained counterparts. VDG MOSFETs exhibit a stronger capability to restrict short-channel-effects over traditional MOSFETs.

PACS: 78.40.Fy, 78.55.Ap, 78.30.Am

With the rapid development of integrated circuits, the existing silicon materials and processes are approaching their physical limits and facing severe challenges. As the device feature size shrinks continuously, various short-channel effects arise. The main adverse effects are the weakening of gate control capability and the significant increase of leakage current, which will bring serious influence to the fabrication and performance of devices and integrated circuits. Traditional bulk-Si metal-oxide- semiconductor-field-effect-transistor (MOSFET) devices are difficult to meet the further requirements of device performance. Silicon-on-insulator (SOI) complementary-metal-oxide-semiconductor (CMOS) technology with low power consumption, low noise, high input impedance, high integration, reliability and other advantages in the field of integrated circuits has occupied a dominant position and continuing to develop in accordance with Moore's law.[1] Multi-gate devices can effectively improve the problems existing in single-gate devices, considered the ideal candidate structure of the next generation of integrated circuits. A double gate device's current drive capability is superior to single-gate device's. The two gates provide much greater control of charges in the channel, leading to higher drive current and reduction of short channel effects.[2] Vertical double gate device can increase the transistor integration density resulting in low cost.[3] Intel corporation reported that a multi-bit NOR flash cell with sub-50nm body thickness T_{Si}, vertical channel (not FINFET) and double gate can be fabricated on a bulk-silicon substrate and can be electrically characterized, which is important for scalability, density and multi-bit operation.[4] SiGe technology has been used in energy band engineering and strain engineering in silicon devices and integrated circuits (ICs). Mandal *et al.*[5] reported a vertical double gate heterojunction p-MOSFET with a compressively strained SiGe channel and ultra-short length of 90 nm. The simulation results show that significant performance enhancements can be achieved in terms of higher saturation drain current, lower short channel effect, and lower drain-induced barrier lowering.

Combined with energy band engineering and vertical double gate structure, a novel vertical double gate strained channel full-depleted SiGe-on-insulator (SGOI) n-MOSFET with lower short channel effect, floating body effect and self-heating effect is presented in this Letter. The electrical properties of the novel structure n-MOSFET is simulated and analysed in comparison with the traditional silicon channel vertical double gate SGOI (VDG SGOI) n-MOSFET.

Table 1. Geometric and process parameters of the device.

Channel length(Vertical thickness of strained Si layer) (nm)	60
Lateral thickness of strained Si layer (nm)	40
Doping concentration of front gate (cm^{-3})	As 5×10^{19}
Doping concentration of back gate (cm^{-3})	As 5×10^{19}
Doping concentration of source and drain (cm^{-3})	As 1×10^{20}
Front gate oxide thickness (nm)	3
Back gate oxide thickness (nm)	3
Doping concentration of channel (cm^{-3})	B 1×10^{18}

*Supported by the Applied Material Research Foundation of Xi'an under Grant No XA-AM-200807, the Fund of Education Department of Shaanxi Province under Grant No 08JK384.

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Figure 1 shows the schematic cross section view of the present vertical double gate strained channel SGOI n-MOSFET. The relevant parameters of device structure and process parameters are listed in Table 1. In the structure, the strained Si channel grows in a virtual alloy SiGe substrate, which can enhance electron mobility, hence greater saturation drain current, higher transconductance and higher speed of the device could be obtained. Apart from that, as the vertical channel is adopted, the channel length is independent of lithographic accuracy, and it is of great advantage to improve the density of IC. Thus, the longer channel length can weaken all the second order effects induced by the miniaturization of devices, which would not affect the integration. In SOI devices, the unique SiO_2 buried layer plays an irreplaceable advantage in the reduction of parasitic capacitance, overcoming the latch-up effect. However, due to the fact that the thermal conductivity of SiO_2 buried layer (1.4 W/mK) is far below the thermal conductivity of silicon (145 W/mK), it leads to a very slow heat dissipation for SOI devices, and the heat generated in the active region is soon accumulated, inevitably resulting in the increase of lattice temperature and degeneration of the device, which is the so-called self-heating effects, while the SiGe layer between the SiO_2 layer and channel in the new structure of the device can apparently inhibit the self-heating effects.

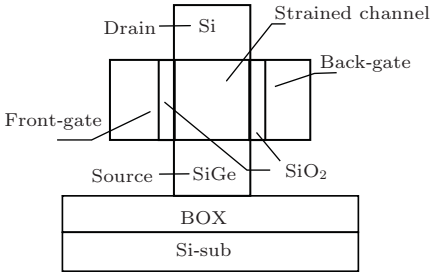

Fig. 1. Schematic cross section view of vertical double gate strained channel SGOI n-MOSFET.

A two-dimensional device simulation software ISE TCAD, taking into account the second order effects of the deep sub-micron devices and adopting a more precise hydrodynamic model and quantum mechanical model (e/h quantum potential), is used to simulate the electrical characteristics of the device. The mobility model uses the velocity saturation model (e/h highfield saturation) when the device channel is under high intensity electric field which includes mobility degradation induced by ionized impurity scattering (doping dep) and vertical electric field in channel (enormal). The recombination model contains band to band tunnelling, SRH (Shockley–Read–Hall) (tunnelling doping dep), Auger recombination and e/h avalanche, etc. The Poisson (poisson), Electronic (electron), hole (hole) and the electronic temperature (eTemperature) equations are calculated to lead the simulation results closer to the true situation.

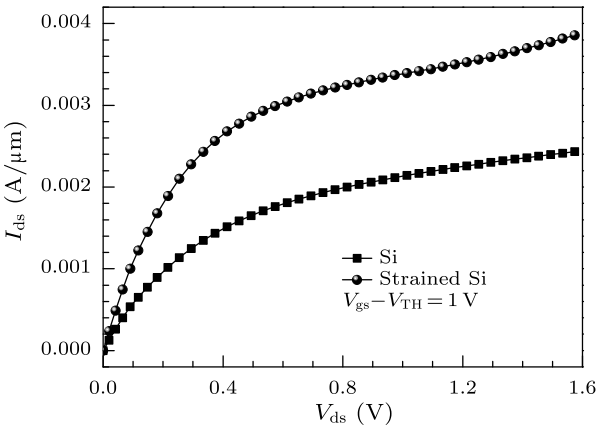

Fig. 2. Output characteristics of strained channel VDG SGOI n-MOSFET and conventional VDG SGOI n-MOSFET.

Figure 2 shows the output characteristic of strained channel VDG SGOI n-MOS and conventional VDG SGOI n-MOS when Ge component is 0.2, $V_{gs} - V_{TH}$ is equal to 1V and V_{ds} is biased at 1.5 V. From the figure we can see that the drive currents of the strained channel device and conventional VDG SGOI are 3.79 mA/μm and 2.40 mA/μm, respectively. That is to say, the drive capability enhancement of the strained channel device is 57.92% compared with the conventional VDG SGOI. For the strained channel Si n-MOS, the increment of carrier mobility chiefly comes from the reduction of the effective mass of carriers (electron mainly) and the decrement of scattering ratio of phonon in valley. Under the strain effect, the six-fold degeneracy energy valley of Si conduction band will split into two groups: one is two-fold degeneracy energy valley, and its energy is lower than the energy of the original valley, the other is four-fold degeneracy energy valley, and its energy is higher than the energy of the original valley. The two-fold degeneracy energy valley goes along the direction perpendicular to the interface, and four-fold degeneracy energy valley goes along the direction parallel with the interface. The empirical value of energy difference between the high energy valley and the low one is $0.6x$ eV, where x is the concentration of Ge. The tensile stress of upper strained Si layer will increase with the increasing Ge composition in the SiGe layer, and electron mobility will increase as well.[6]

Figure 3 illustrates the comparison of transfer characteristic between strained channel n-MOS and conventional n-MOS, when Ge component is 0.2, $V_{gs} - V_{TH}$ is equal to 1 V and V_{ds} is biased at 0.1 V. The simulation results suggest that the threshold voltage of strained channel VDG SGOI is 0.1922 V, and the threshold voltage of conventional n-MOS is 0.1907 V. The threshold voltage is defined as the voltage of a

point which is the crossing point of the horizontal axis and the tangent line of $I_{ds} - V_{gs}$ curve, which has achieved the maximum slope of the $I_{ds}-V_{gs}$ curve. Because the curve slope of strained n-MOS is larger than that of the traditional n-MOS, the threshold voltage of strained n-MOS is larger with this method. From the figure we can obviously see that the drive current of the strained channel VDG SGOI is larger than the traditional device, for instance, the drive current of the strained device is 0.562 mA/μm while the traditional one is 0.374 mA/μm when V_{gs} is biased at 0.8 V.

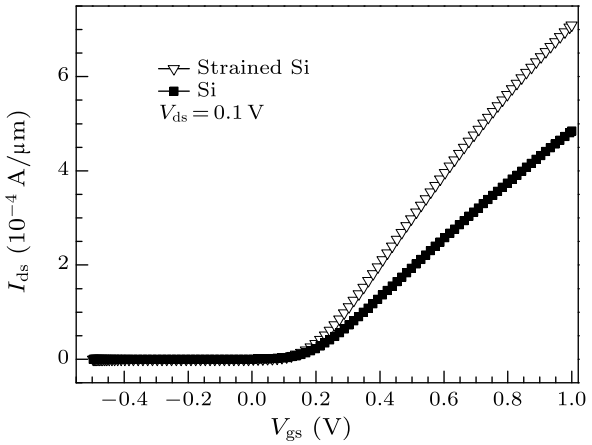

Fig. 3. Transfer characteristics of strained channel SOI MOSFET and conventional SOI MOSFET.

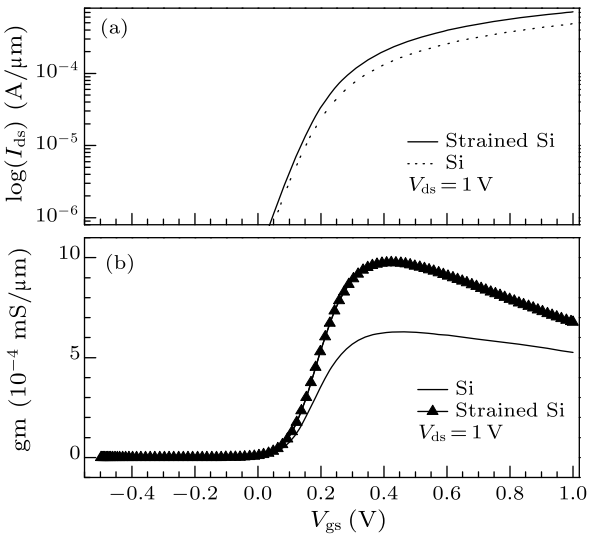

Fig. 4. Comparison of subthreshold characteristics (a) and transconductance (b) for strained channel n-MOS and conventional n-MOSFET.

Figures 4(a) and 4(b) display the comparison of subthreshold characteristics and the transconductance curves of the two devices, respectively. The grid swing S of the strained channel VDG SGOI is 19.128 mV/decade, while the traditional VDG SGOI is 26.172 mV/decade with 36.83% decrease compared with the former one, which means reduced short channel effects. Therefore it can be concluded that the novel structural n-MOS can achieve a better channel control capability compared with the traditional VDG SGOI device. Figure 3(b) demonstrates that the maximum transconductance of the strained VDG SGOI is 972 μS/μm, whereas the traditional one is 629 μS/μm, which means that the transconductance of the novel structure is 54.53% greater than that of the traditional one. Therefore, it is clear that the new structure has a better gate control capability.

The novel device structure presented here can be implemented under current semiconductor manufacture level. Figure 5 shows the complete process flow for the strained Si including bonding, SGOI substrate and regrowth steps.[7]

SGOI substrates can be fabricated via several approaches. The etch-back approach is selected. First of all, a 2.5-μm compositionally graded SiGe buffer (up to 25% Ge), capped with 2 μm of relaxed $Si_{0.75}Ge_{0.25}$ was deposited onto a Si donor wafer using an ultra-high-vacuum chemical vapour deposition (UHV-CVD) reactor [Fig. 5(a)]. The SiGe surface was polished using chemical mechanical polishing (CMP) to eliminate surface roughness. After a clean step, the donor wafer was bonded to a thermally oxidation handle wafer, and annealed at 850°C for 1.5 h. The bonded pair was ground to remove the donor wafer substrate, and then subjected to a tetramethyl ammonium hydroxide (TMAH) solution to etch away the SiGe grade layer until SiGe with 20% Ge exposed [Fig. 5(b)]. Then the relaxed SGOI substrate was put back to UHV-CVD reactor to regrow a relaxed SiGe (doping: p-type 10^{20} cm^{-3}), a strained-Si layer (60 nm) and Si layer[7] [Fig. 5(c)].

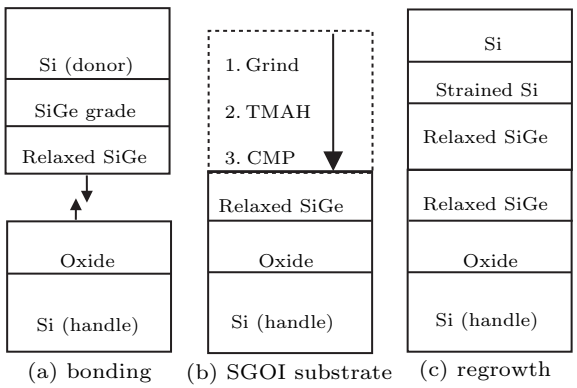

Fig. 5. Process flow for the strained Si.

We start with a 20-nm SiO_2 pad layer with dry oxidation. This thickness is chosen to keep in mind the SiO_2 etch selectivity to both polysilicon block and nitride spacer etch steps. Then the polysilicon block using deposition, which dictates the spacer height, is chosen to be three times its width. A two-step polysilicon block etch is used. The first step ensures near 90° sidewalls, while the second step yields an excel-

lent selectivity to underlying SiO_2. Different Si_3N_4 spacer thicknesses ranging from 5 to 50 nm were deposited and etched anisotropically. TMAH was used to remove the polysilicon block, leaving the nitride spacer behind. Subsequently, a Si fin is etched in a $Cl_2/HBr/O_2$ chemistry with the Si_3N_4 spacer as the hard mask. This is followed by the arsenic source implant step. Before the implant, a 45-nm-thick sacrificial LTO (low-temperature oxide) is deposited by low-pressure chemical vapour deposition (CVD) to protect the channel, whereas the original nitride spacer mask protects the drain. A 5-min 1000°C annealing is performed for dopant activation and diffusion after removing the nitride and oxide films. Next, a novel self-aligned process is accomplished for source explantation. Gate stack deposition is followed by gate definition, active area isolation (using a trench etch process), and dry oxidation to prevent leakage. Subsequently, preparations for the drain contact process are made. The first step is to deposit a compressive Si_3N_4 layer (slightly thicker than gate polysilicon), and then, spacer etch it. This layer serves several purposes in the VDG n-MOS structure. Its main purpose is to serve as an etch stop for the drain contact hole etch, and consequently, provide control over channel length and contact/series resistance of the VDG n-MOS.

The Si_3N_4 layer deposition and etch is followed by the drain implant (Arsenic, $5\times10^{20}\,\mathrm{cm}^{-2}$ dose, 30 keV energy), the PSG layer deposition, and the rapid thermal annealing RTA step (12 s at 1050°C) for dopant activation. Finally, aluminium is deposited and patterned, and a forming gas anneal (FGA) for 30 min at 400°C is performed.[8]

In summary, we have presented a novel full depleted strained channel VDG SGOI n-MOSFET, by using this device we can greatly improve the integration density and also reduce the short channel effect. The simulation results show that compared with the conventional VDG SGOI n-MOSFET, the drive capability of the novel structure device is improved up to 57.92%, the transconductance increases 54.53% and grid swing decreases 36.83%, which means more precipitous sub-threshold slope and better control capabilities for short channel effects. Therefore, applying the novel structure into integrated circuits can increase the integration density and circuit speed greatly.

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